T-52-13-90

OKI semiconductor

MSC7701 (Underdevelopment)

40-BIT GRID DRIVER

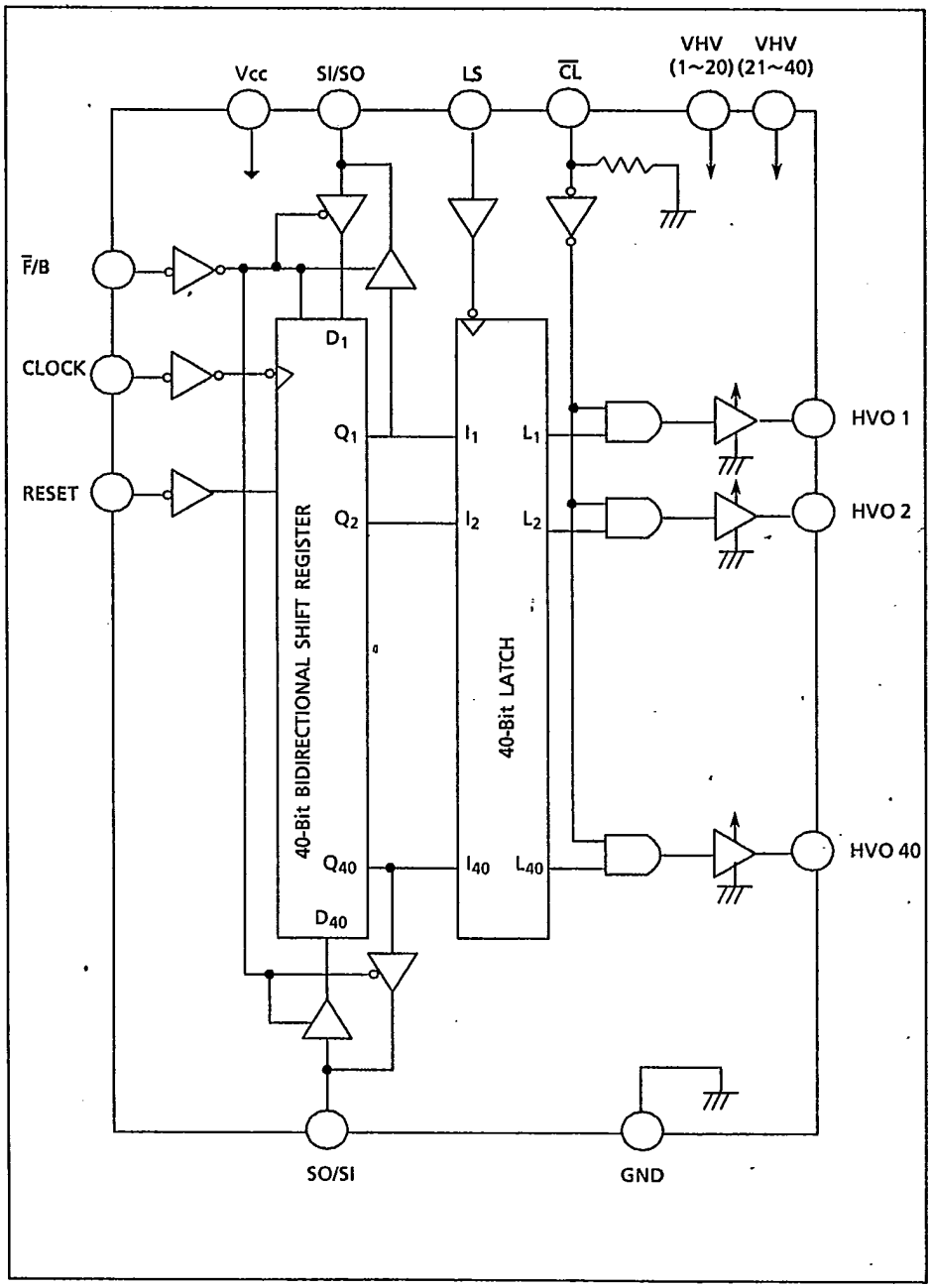
GENERAL DESCRIPTION

The MSC7701 is a monolithic IC using the high withstand voltage driver process for hybridizing CMOS and DMOS transistors on one chip.
The logic portion such as the input stage, shift register and latch is formed by CMOS, and the output driver requiring a high withstand voltage is formed by DMOS transistors.
Since the pin assigment allows single side pattern formation on the printed circuit board, the display unit size can be reduced.
The bidirectional shift register facilitates the pattern design when the devices are arranged symmetrically with the display at the center axis.

FEATURES

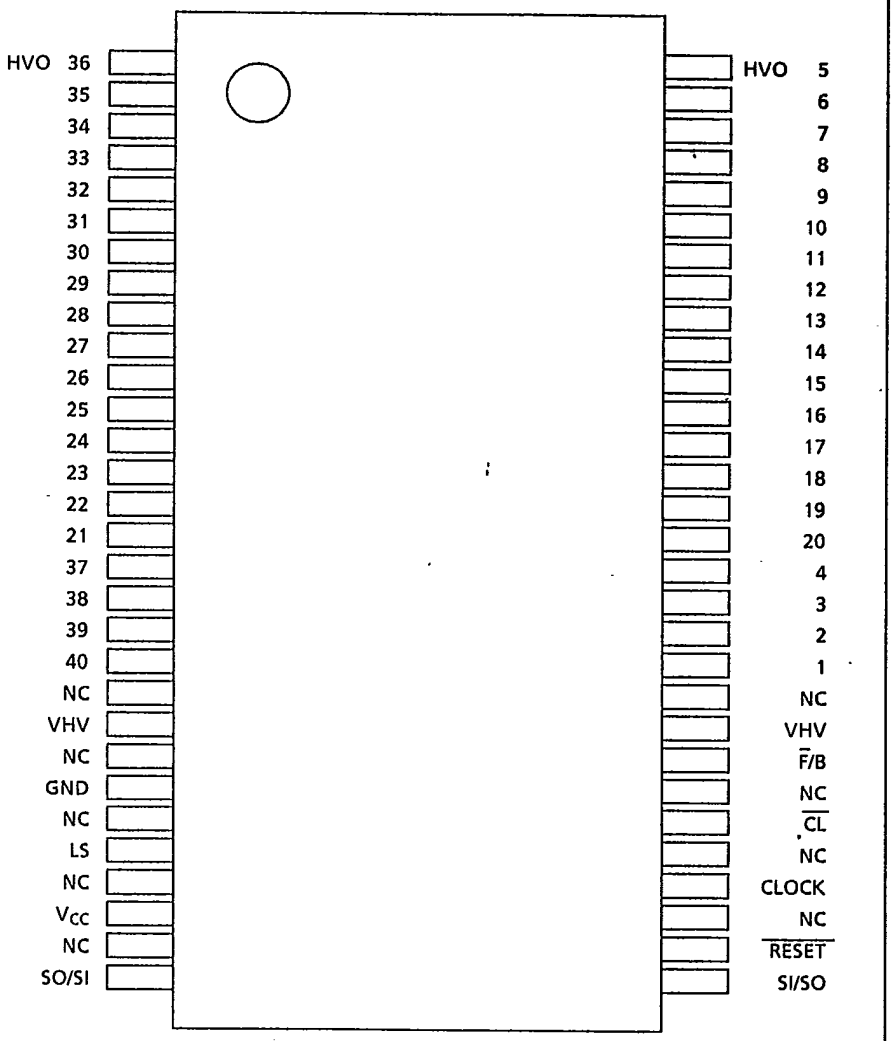
- Logic supply voltage (V_{CC}) : + 5 V
- VF driver supply voltage (V_{hv}) : + 130 V ;
- VF driver output current
  (I_{ohvh}) : – 40 mA (1 driver output high)
  (I_{ohvl}) : + 2 mA
- Clock frequency : 5.5 MHz
- Built-in 40-Bit latch
- Built-in 40-Bit bidirectional shift register
- 60 Pin FLAT Package

BLOCK DIAGRAM



PIN CONFDIGURATION

(Top View) 60 Lead Plastic Flat Package



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PIN DESCRIPTION

Pin No.	Symbol	Name	Description
1 ⋮ 20, 41 ⋮ 60	HVO 1 ⋮ HVO 40	Driver output	1. Each terminal is a high withstand voltage driver output terminal to drive the grid of the VF display tube, which corresponds to each bit of the shift register. 2. Each terminal can be directly connected to the grid terminal of the VF display tube.
22, 39	V_{HV}	Driver supply voltage	1. This is a power terminal of the high withstand voltage driver to drive the VF display tuve.
28	V_{CC}	Logic supply voltage	2. This is a power terminal of the logic portion.
36	$\overline{CL}$	Clear input	1. This is an input terminal containing a pull-down resistor. 2. The terminal is generally kept High. The driver output, High or Low, is driven by the output of the corresponding latch circuit. 3. When the terminal is Low, the driver outputs are fixed to "Low" regardless of the output of the latch circuit.
26	LS	Latch strobe input	1. When the terminal is High, the latch circuit is slewed, and the output of the shift register is read into the latch circuit. 2. When the terminal is Low, the latch circuit holds the output of the shift register immediately before the terminal is turned Low.
34	CLOCK	Clock input	1. This is a clock terminal of the shift register. The data of the shift register is shifted at the falling edge of a clock pulse.
32	$\overline{RESET}$	Reset input	1. When the terminal is Low; all the data of the shift register is Low. Generally and when not in use, connect the terminal to the V_{CC} terminal.
38	$\overline{F}$/B	Shift direction control input	1. When the terminal is Low, data is shifted from 1 to 40, and Pin 31 is a serial in terminal and Pin 30 is a serial out terminal. 2. When the terminal is High, data is shifted from 40 to 1, and Pin 30 is a serial in terminal and Pin 31 is a serial out terminal.
31	SI/SO	Serial input/serial output	1. When the $\overline{F}$/B terminal is Low, this terminal is a serial data input terminal. 2. When the $\overline{F}$/B terminal is High, this terminal is a serial data output terminal.
30	SO/SI	Serial output/serial input	1. When the $\overline{F}$/B terminal is Low, this terminal is a serial data output terminal. 2. When the $\overline{F}$/B terminal is High, this terminal is a serial data input terminal.
24	GND	GND	1. This is a grounding (GND) terminal.

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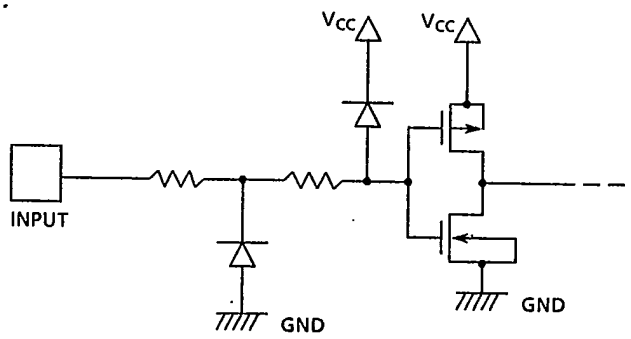
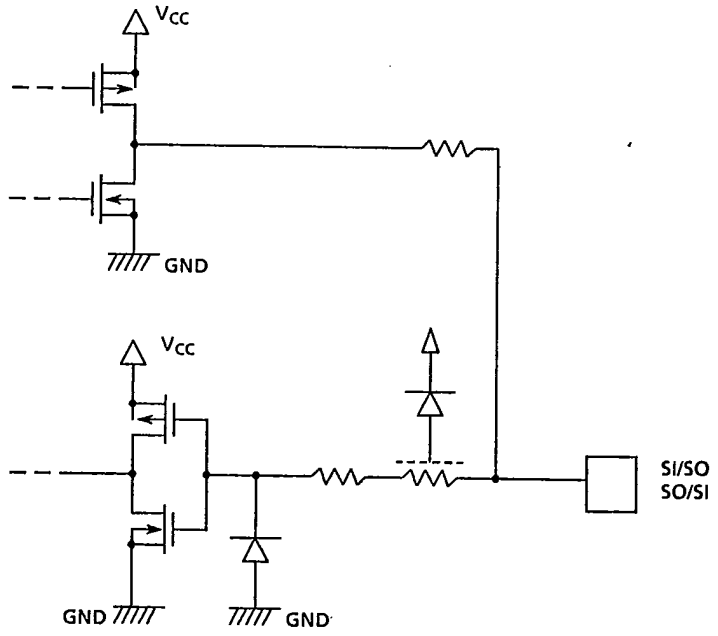
SCHEMATIC DIAGRAMS OF LOGIC PORTION INPUT AND OUTPUT TERMINAL CIRCUITS

Input terminal



Input-output terminal



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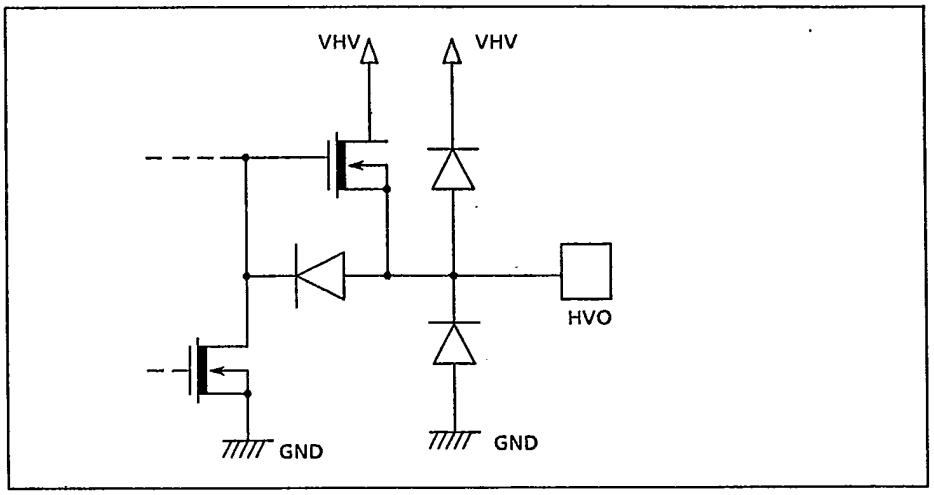
SCHEMATIC DIAGRAM OF DRIVER OUTPUT TERMINAL CIRCUIT



FUNCTION TABLE

$\overline{RESET}$	CLK	$\overline{F}$/B	SI/SO	Q1	Q2	Q3	----	Q39	Q40	SO/SI
L	X	L	X	L	L	L		L	L	L
L	X	H	L	L	L	L		L	L	X
H	↓	L	H	H	Q_{1n}	Q_{2n}		Q_{38n}	Q_{39n}	Q_{39n}
H	↓	L	L	L	Q_{1n}	Q_{2n}		Q_{38n}	Q_{39n}	Q_{39n}
H	↓	H	Q_{2n}	Q_{2n}	Q_{3n}	Q_{4n}		Q_{40n}	H	H
H	↓	H	Q_{2n}	Q_{2n}	Q_{3n}	Q_{4n}		Q_{40n}	L	L

$\overline{CL}$	LS	Qn	HVOn
L	X	X	L
H	H	H	H
H	H	L	L
H	L	X	NC

L : Low Level, H : High Level
X : Don't Care, NC : No Change

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ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Parameter	Symbol	Conditios	Limits	Unit	Note
Logic supply voltage	V_{CC}	Applicable to logic power terminal	−0.3~6.5	V	1
Driver supply voltage	V_{HV}	Applicable to driver power terminal	V_{CC}~150	V	1
Input voltage	V_{IN}	Applicable to all input teminals	−0.3~V_{CC} + 0.3	V	1
Data ouptput voltage	Vod	Applicable to data output terminal	−0.3~V_{CC} + 0.3	V	1
Driver output voltage	Vohv	Applicable to all driver terminals	−0.3~V_{CC} + 0.3	V	1
Power Dissipation	Pd	Ta≦25°C	860	mW	
Attenuation Rate	Rj-a	Ta>25°C	145	°C/W	2
Operating temperature	Top	VHV≦130V	−40~+85	°C	
Storage temperature	Tstg	———	−55~+150	°C	

Notes : 1. The maximum voltage which can be applied to the GND terminal.

2. Thermal resistance of the package (between junction and atmosphere).
The junction temperature (Tj) expressed by the equation indicated below should not exceed 150°C.
$Tj = P \times Rj - a + Ta$ (P : Maximum power consumption of IC)

- **Recommended Operating Conditions**

Parameter	Symbol	Conditions		MIN	MAX	Unit
Logic supply voltage	V_{CC}	Applicable to logic power terminal		4.5	5.5	V
Driver supply voltage	V_{HV}	Applicable to logic power terminal		10	130	V
High level input voltage	V_{IH}	Applicable to all input terminals	V_{CC} = 4.5V	3.6	—	V
			V_{CC} = 5.5V	4.4	—	
Low level input voltage	V_{IL}	Applicable to all input terminals	V_{CC} = 4.5V	—	0.9	V
			V_{CC} = 5.5V	—	1.1	
Driver high level output current	I_{OHVH}	1 driver output : High Other driver outputs : Low		—	− 40	mA
Driver low level output current	I_{OHVL}	Applicable to all driver output terminals		—	2	mA
Clock frequency	fØ	See timing chart.		—	5.5	MHz
Clock pulse width	t_{wclkl}	See timing chart.		70	—	nS
Data setup time	t_{ds}	See timing chart.		20	—	nS
Data hold time	t_{dh}	See timing chart.		45	—	nS
LS pulse width	t_{wls}	See timing chart.		80	—	nS
CLK-LS delay time	t_{dcl}	See timing chart.		45	—	nS
LS-CL delay time	t_{dlcl}	See timing chart.		0	—	nS
CL pulse width	t_{wcl}	See timing chart.		2	—	µS
Operating temperature	Top	See timing chart.		− 40	+ 85	°C

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• DC Characteristics

V_{CC} = 5V ± 10%, V_{HV} = 110V, Ta = −40°C~+85°C

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Logic supply current	I_{CC1}	No load V_{CC} = 5.5V	All inputs : Low	—	—	50	µA
	I_{CC2}		All inputs : High 1 driver output : High Other driver outputs : Low	—	—	200	
Driver supply current	I_{HV1}	No load V_{CC} = 5.5V	All driver outputs : Low	—	—	50	µA
	I_{HV2}		1 driver output : High	—	1.1	1.5	mA
High level input voltage	V_{IH}	V_{CC} = 4.5V	Applicable to all input terminals	3.15	—	—	V
		V_{CC} = 5.5V		3.85	—	—	V
Low level input voltage	V_{IL}	V_{CC} = 4.5V	Applicable to all input terminals	—	—	1.35	V
		V_{CC} = 5.5V		—	—	1.65	V
Input leak current	I_{ILEEK}	Ta = 25°C	Input terminals except $\overline{CL}$ terminal	—	—	±1	µA
High level input current	I_{IH}	V_{CC} = 4.5V	Applicable to $\overline{CL}$ terminal	20	50	100	µA
		V_{CC} = 5.5V		25	60	200	
Input capacitance	C_{IN}	Ta = 25°C		—	15	—	pF
High level data output voltage	V_{ODH}	I_O = −0.1mA	V_{CC} = 4.5V	3.5	—	—	V
			V_{CC} = 5.5V	4.5	—	—	
Low level data output voltage	V_{ODL}	I_O = −0.1mA	V_{CC} = 4.5V	—	—	0.9	V
			V_{CC} = 5.5V	—	—	1.1	
High level driver output voltae	V_{OHVH}	I_{OHV} = −40mA		106	—	—	V
Low level driver output voltae	V_{OHVL}	I_{OHV} = 2mA		—	—	4	V

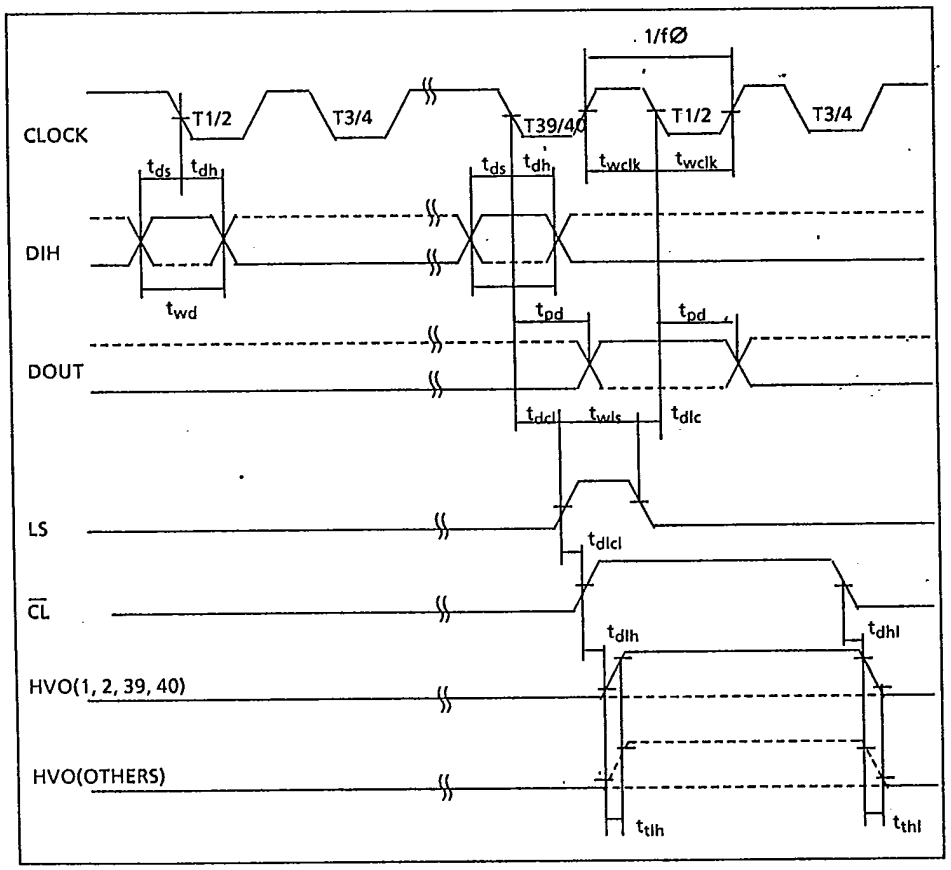
- **AC Characteristics**

V_{CC} = 5V, V_{HV} = 200V, Ta = 25°C

Parameter	Symbol	Conditios	MIN	TYP	MAX	Unit	Note
CLK-DOUT delay time	t_{pd}	See timing chart and test chart.	—	100	150	nS	4
Delay time : L→H	t_{dlh}	See timing chart and test chart.	—	0.3	1	µs	5, 6
Transit time : L→H	t_{tlh}	See timing chart and test chart.	—	2	5	µs	5
Delay time : H→L	t_{dhl}	See timing chart and test chart.	—	0.3	1	µs	5, 6
Transit time : H→L	t_{thl}	See Timing chart and test chart.	—	3	6	µs	5

Note 4 : Applicable to data output terminal.
Note 5 : Applicable to driver output terminal.
Note 6 : t_{dlh} and T_{dhl} are delay times from $\overline{CL}$ signal.

- **Timing Chart**



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TEST CIRCUIT