Video Signal Driver for DVD Players
Monolithic IC MM1568

July 10, 2002

Outline

This IC is a video signal driver IC that supports 6-ch progressive video developed for DVD players. It includes a low-pass filter that attenuates the noise element during DA conversion, and a 3-channel 6dB amp with 75Ω driver (component circuit: 2-channel).
In addition, external ESD protection diodes can be reduced by a sag correction pin for reducing output coupling capacitance, and enhancement of the ESD protection elements for output pins.

Features

1. Includes a SAG correction pin
2. Enabled to drive a 3-channel 6dB amp with 75Ω driver
3. Includes a 4th-order low-pass filter
   Frequency response: 6.75MHz ±1dB / 27MHz - 27dB min.
   13.5MHz ±1dB / 54MHz - 24dB min.
4. Includes a 6dB amp
5. Includes a power save function
6. S/N=80dB typ.(Y/C mix:74dB typ.)
7. ESD strengh (aerial discharge) of ±15kV (IEC standard)
8. The component circuity can support RGB sgnals with the control pin.

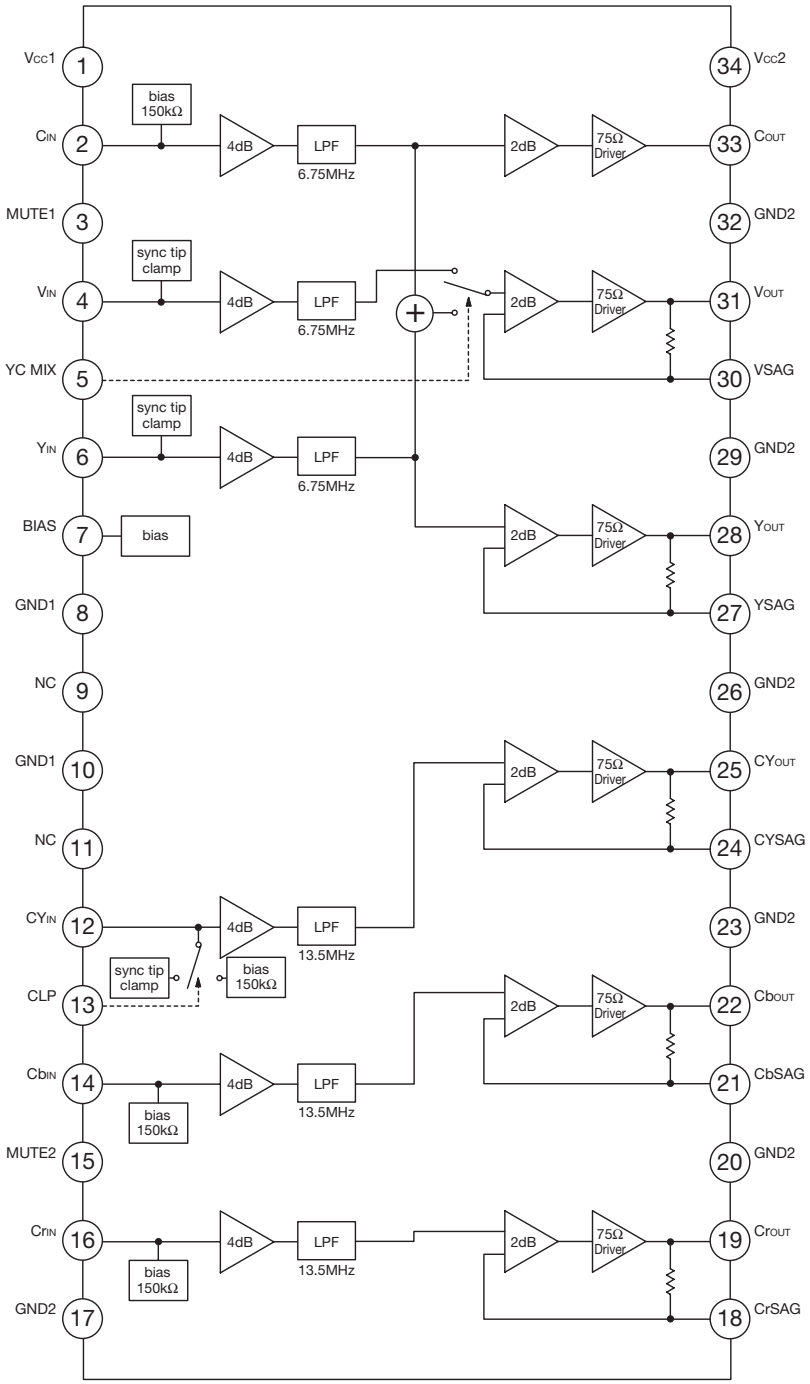
Package

SSOP-34A

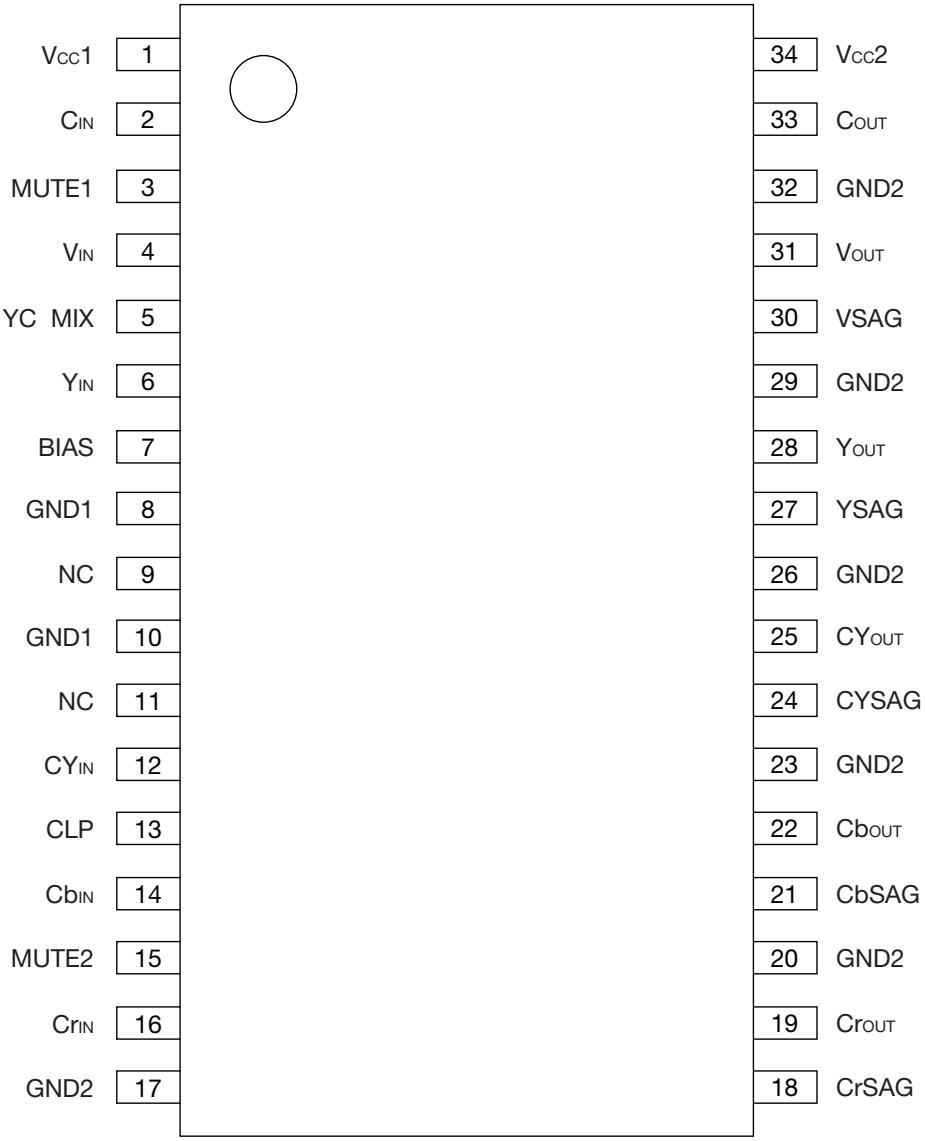
Applications

1. DVD players that support progressive video
2. Digital STB
3. Other digital video equipment

Block diagram



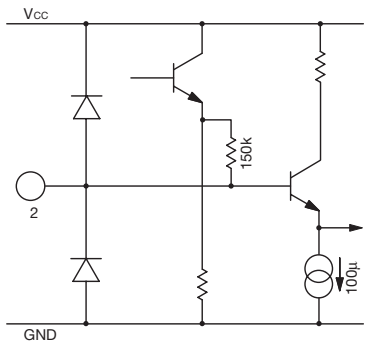
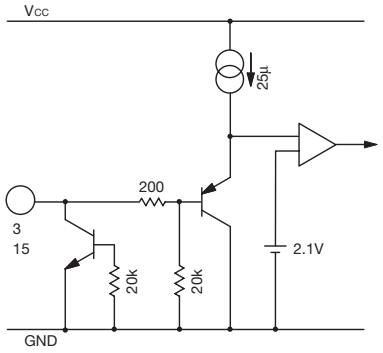
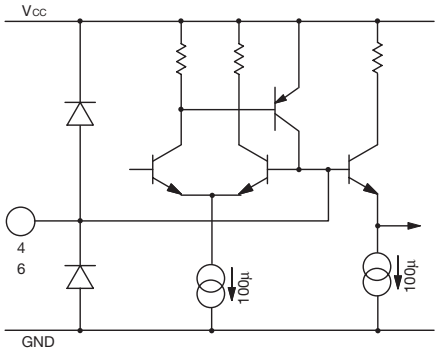
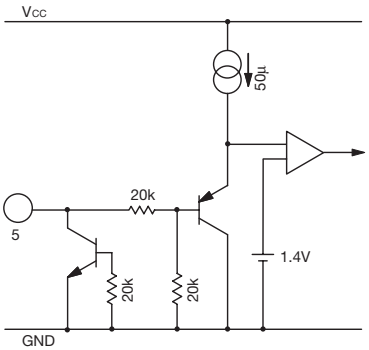
Pin Assignment



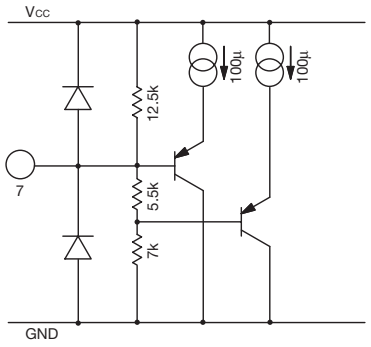
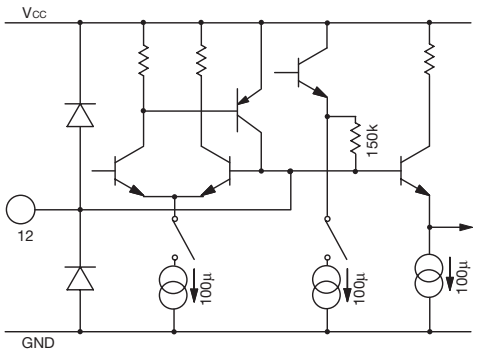
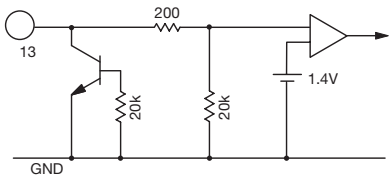
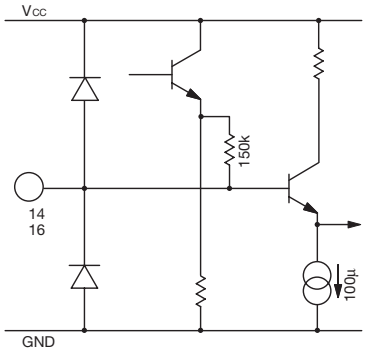
SSOP-34A

1	Vcc1	18	CrSAG
2	CIN	19	CrOUT
3	MUTE1	20	GND2
4	VIN	21	CbSAG
5	YC MIX	22	CbOUT
6	YIN	23	GND2
7	BIAS	24	CYSAG
8	GND1	25	CYOUT
9	NC	26	GND2
10	GND1	27	YSAG
11	NC	28	YOUT
12	CYIN	29	GND2
13	CLP	30	VSAG
14	CbIN	31	VOUT
15	MUTE2	32	GND2
16	CrIN	33	COUT
17	GND2	34	Vcc2

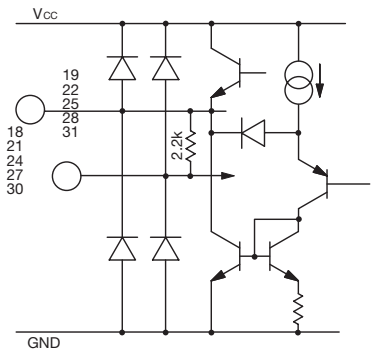
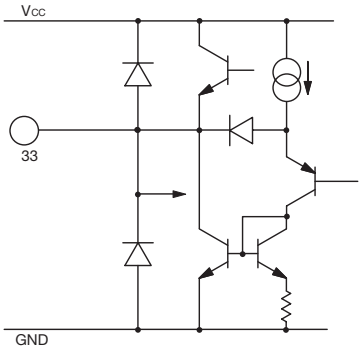
Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
1 34	$V_{CC}1$ $V_{CC}2$	V_{CC}	
2	C_{IN}	Croma input	
3 15	MUTE1 MUTE2	Mute Select Using of Mute and POWER-SAVING	
4 6	V_{IN} Y_{IN}	Video input (Composite or Y) Input clamp:Sync tip	
5	YC MIX	YC MIX select	

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
7	BIAS	Bias	
8 10 17 20 23 26 29 32	GND1 GND1 GND2 GND2 GND2 GND2 GND2 GND2	GND	
9	NC	NC	
11	NC	NC	
12	CY_{IN}	Luminance input The input can select Sync tip clamp or Bias.	
13	CLP	Input clamp select	
14 16	Cb_{IN} Cr_{IN}	Component input	

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
18 21 24 27 30	CROUT CBOUT CYOUT YOUT VOUT	Signal output	
19 22 25 28 31	CrSAG CbSAG CYSAG YSAG VSAG	SAG correction	
33	COUT	Croma output	

Absolute Maximam Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Storage temparature	TSTG	–65 ~ +150	°C
Operating temparature	TOPR	–40 ~ +85	°C
Supply Voltage	VCC max.	7	V
Power dissipation *1	Pd	1.4	W

note *1 Board mounting power dissipation. Board size 100mmX100mmX1.6mm

Recommended Operating Conditions

Item	Symbol	Rating	Unit
Operating temparature	TOPR	–40 ~ +85	°C
Operating Voltage	VCCOP	4.5 ~ 5.5	V

Electrical Characteristics (Unless otherwise specified, Ta=25°C,Vcc=5V)

Item		Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Consumption current		$I_{CC}1$	No signal	74	97	126	mA
		$I_{CC}2$	No signal Mute1:ON	36	51	66	mA
		$I_{CC}3$	No signal Mute2:ON	39	55	71	mA
		$I_{CC}4$	No signal Mute1 and Mute2:ON	1	3	5	mA
Croma input		V_{CIN}		1.9	2.4	2.9	V
Composite video input		V_{VIN}		1.15	1.4	1.65	V
Luminance input		$V_{YIN, CYIN}$		1.15	1.4	1.65	V
Component input		$V_{CbIN, CrIN}$		1.9	2.4	2.9	V
Croma outoput		V_{COUT}			2.4		V
Composite video output		V_{VOUT}			1.1		V
Luminance output		$V_{YOUT, CYOUT}$			1.1		V
Component output		$V_{CbOUT, CrOUT}$			2.4		V
Control terminal Input current	H	I_{IHm}*2				350	µA
	L	I_{ILm}*2				35	µA
Control terminal input voltage	H	Vth_{Hm}*2		2.1			V
	L	Vth_{Lm}*2				0.7	V
Input impedance		$Z_{CIN, CbIN, CrIN}$		100	150	200	kΩ
Voltage gain		$G1_{2,3,5,6}$*3	SIN wave:1V f=100kHz	5.7	6.0	6.3	dB
		$G2_{1,4,7,8}$*3	SIN wave:1V f=100kHz	5.7	6.0	6.3	dB
Frequency characteristic		$f1_{1\sim5}$*3	SIN wave:1V 6.75MHz/100kHz	–1.0	0	1.0	dB
		$f2_{1\sim5}$*3	SIN wave:1V 27MHz/100kHz		–40	–27	dB
		$f3_{6}$*3	SIN wave:1V 13.5MHz/100kHz	0	1.0	2.0	dB
		$f4_{7,8}$*3	SIN wave:0.7V 13.5MHz/100kHz	0	1.0	2.0	dB
		$f5_{6\sim8}$*3	SIN wave:1V 54MHz/100kHz		–40	–24	dB
Differential gain		$DG_{1\sim3}$*3	Staircase signal 1V		0.6	1.0	%
Differential phase		$DP_{1\sim3}$*3	Staircase signal 1V		0.6	1.0	°
Output dynamic range		DR_{n}*3	SIN wave:100kHz THD=1.0%	2.6	3.0		V
Crosstalk		CT_{n}*3	f=4.43MHz, 1V		–60	–55	dB
S/N		$SN1_{4\sim5}$*3	BW:100k ~ 6MHz		–80		dB
		$SN2_{1\sim3}$*3	BW:100k ~ 6MHz at MIX OUT		–74		dB
		$SN3_{6\sim8}$*3			–80		dB
Group delay		$t1_{GD1\sim5}$*3	at 100kHz		50		ns
		$t2_{GD6\sim8}$*3	at 100kHz (Component)		30		ns
Group delay deviation		$\triangle t1_{GDn}$*3	to 3.58MHz		4		ns
		$\triangle t2_{GDn}$*3	to 4.43MHz		7		ns
		$\triangle t3_{GD1\sim5}$*3	to 6MHz		12		ns
		$\triangle t4_{GD6\sim8}$*3	to 6MHz (Component)		4		ns
		$\triangle t5_{GD6\sim8}$*3	to 12MHz (Component)		12		ns

note *2 The subscript number "m" is the terminal of right table.

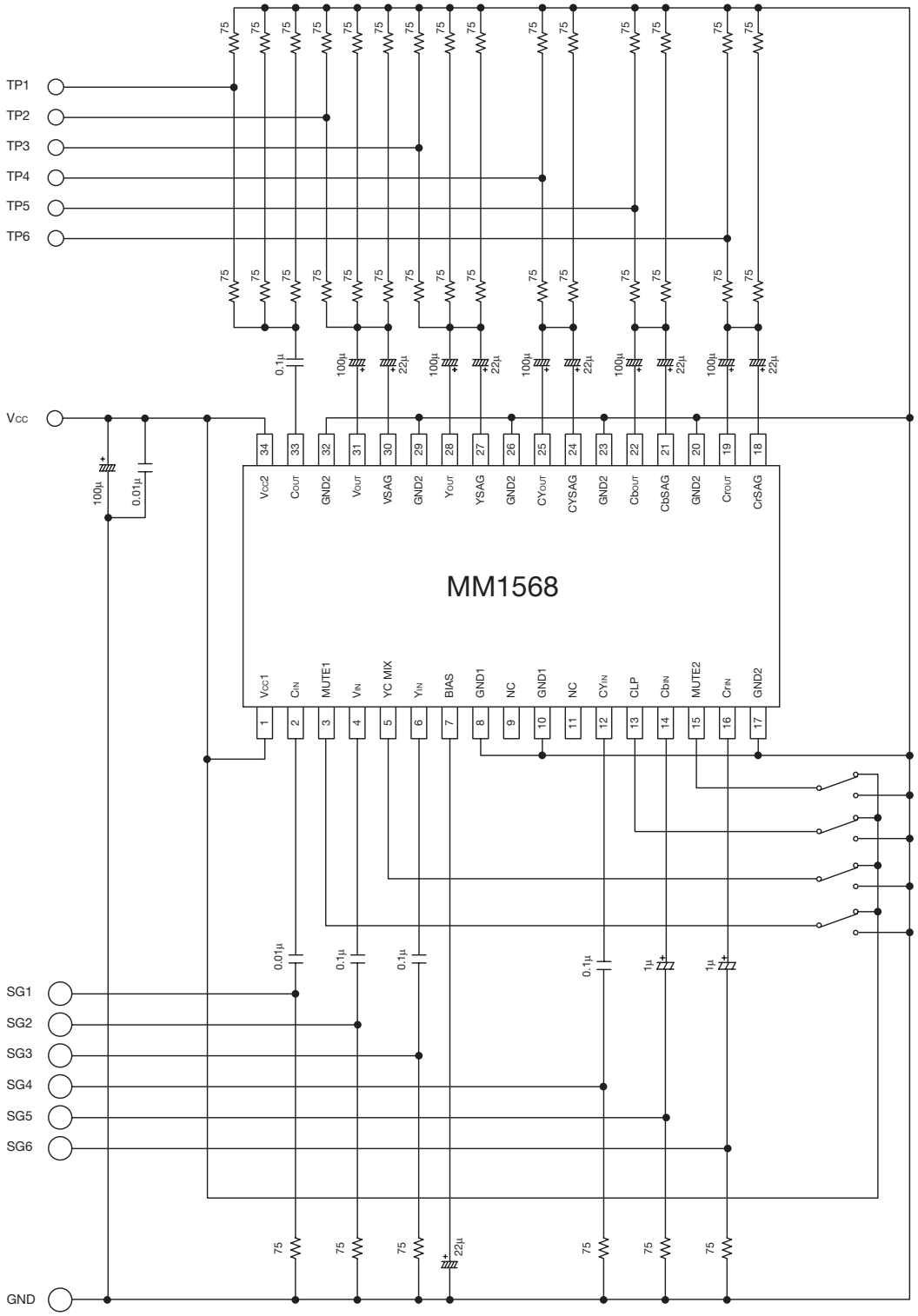
m	Terminal
1	MUTE1
2	MUTE2
3	YC MIX
4	CLP

note *3 The subscript number "n" is the combination of under table.

n	Input	Output
1	C_{IN}	V_{OUT}
2	V_{IN}	
3	Y_{IN}	
4	C_{IN}	C_{OUT}

n	Input	Output
5	Y_{IN}	Y_{OUT}
6	CY_{IN}	CY_{OUT}
7	Cb_{IN}	Cb_{OUT}
8	Cr_{IN}	Cr_{OUT}

Test Circuit

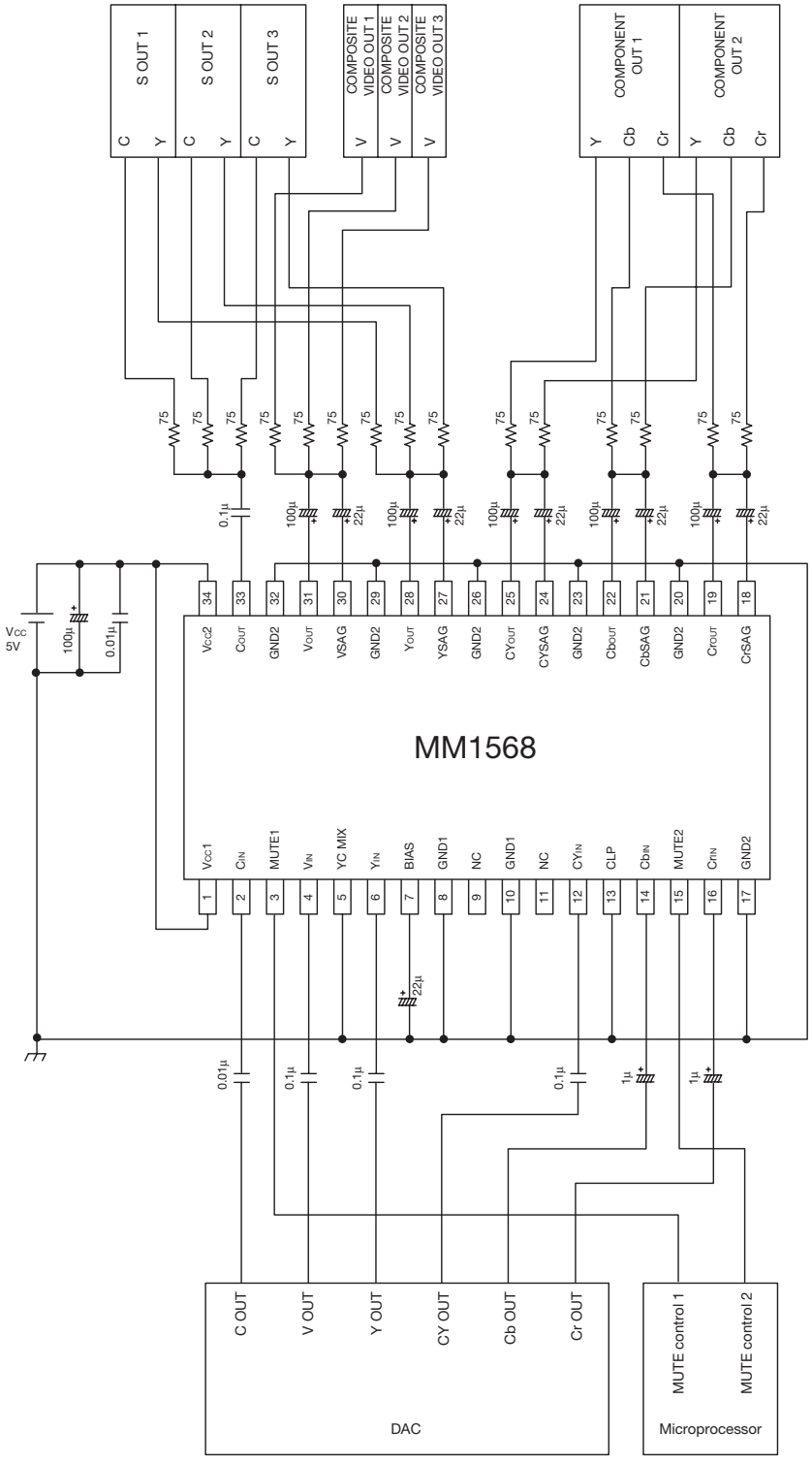


Switch Control Table

Input Select	Output Terminal	Control Terminal			
		MUTE1	YC MIX	MUTE2	CLP
MUTE	C_{OUT}	Low	*	*	*
C_{IN}		High	*	*	*
MUTE	V_{OUT}	Low	*	*	*
$Y_{IN}+C_{IN}$		High	Low	*	*
V_{IN}			High	*	*
MUTE	Y_{OUT}	Low	*	*	*
Y_{IN}		High	*	*	*
MUTE	CY_{OUT}	*	*	Low	*
CY_{IN}(Clamp)		*	*	High	Low
CY_{IN}(Bias)		*	*		High
MUTE	Cb_{OUT}	*	*	Low	*
Cb_{IN}		*	*	High	*
MUTE	Cr_{OUT}	*	*	Low	*
Cr_{IN}		*	*	High	*

* : Don't care

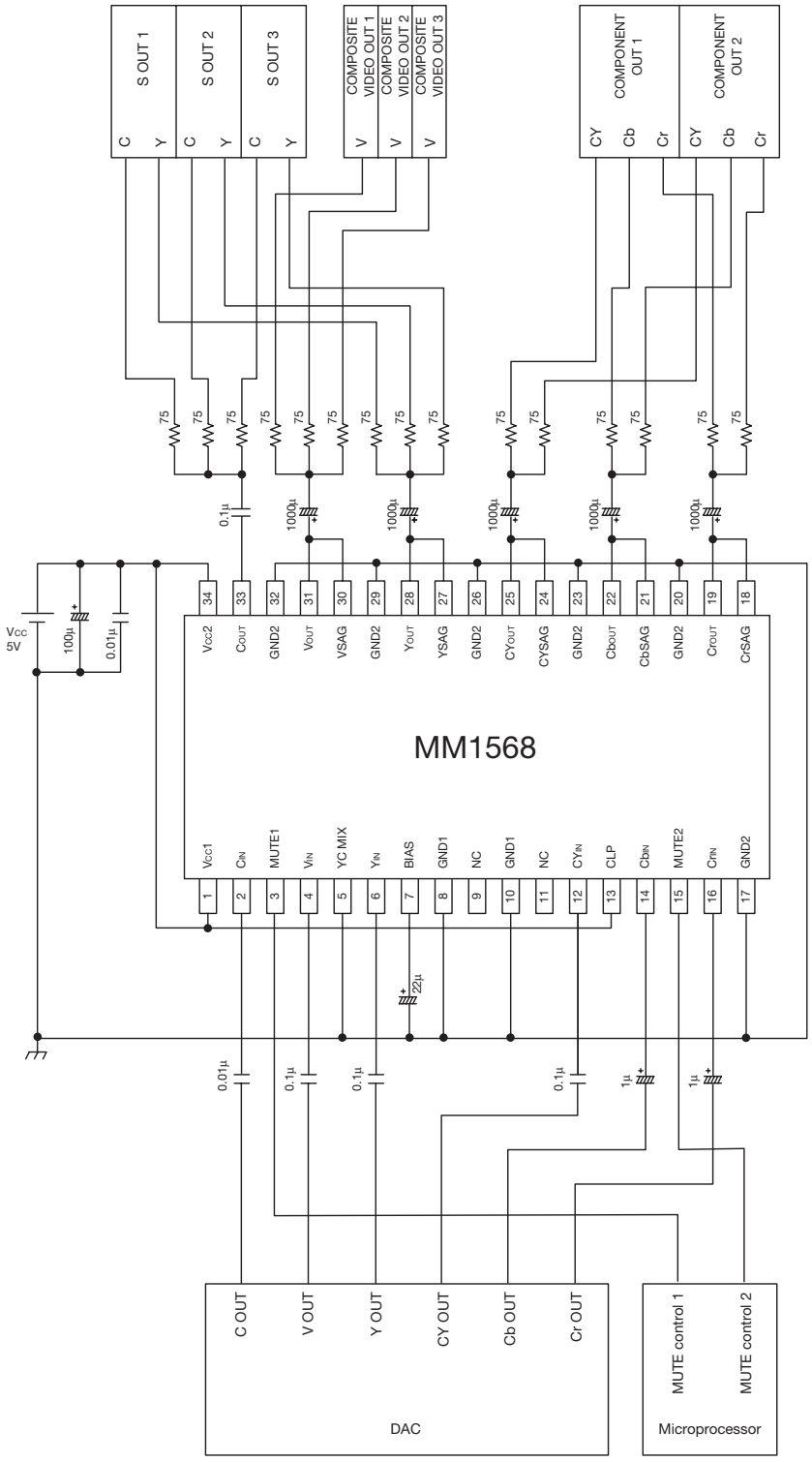
Application Circuit 1



(note) : Please arrange power supply bypass capacitor near the $V_{CC}2$ terminal (34PIN).

Application Circuit 2

At unused the SAG correction function



(note) : Please arrange power supply bypass capacitor near the $V_{CC}2$ terminal (34PIN).