ML2272X-XXX/ML2276X-XXX

Speech Synthesis LSI with Built-in P2ROM Including Speech-Speed Conversion/Pitch Conversion Functions

GENERAL DESCRIPTION

The ML2272X(ML22725/ML22724/ML22723-XXX) and ML2276X(ML22765/ML22764/ML22763-XXX) are speech synthesis LSIs with built-in P2ROM that stores speech data.
These LSIs include speech speed conversion, pitch conversion, edit ROMs, ADPCM2 decoders, 16-bit DA converters, low pass filters, and monaural speaker amplifiers. The ML2272X supports the synchronous serial interface and the ML2276X supports the I2C interface. By integrating all the functions required for speech output into a single chip, these LSIs can be more easily incorporated in compact portable devices.

- Built-in memory capacity and maximum vocal reproduction time:
  the following table (in 4-bit OKI ADPCM2 mode)

Product name	ROM capacity	Maximum vocal reproduction time (sec) *		
		F_S = 8.0 kHz	F_S = 16 kHz	F_S = 32 kHz
ML22725-XXX/ML22765	16 Mbits	522	261	130
ML22724-XXX/ML22764	8 Mbits	260	130	64
ML22723-XXX/ML22763	4 Mbits	129	64	32

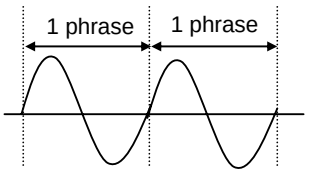
(*: Speech -speed or pitch conversion functions is not used.)

- voice synthesis method: 4-bit OKI ADPCM2
  8-bit Nonlinear PCM
  8-bit PCM, 16-bit PCM
  Can be specified for each phrase.
- Sampling frequency(F_S): 4.0 / 5.3 / 6.4 / 8.0 / 10.6 / 12.0 / 12.8 / 16.0 / 21.3 / 24.0 / 25.6 / 32.0 / 48.0 kHz
  F_S can be specified for each phrase.
- Built-in low-pass filter and 16-bit DA converter
- Speaker driving amplifier: 0.7 W (8Ω , DV_{DD}=5 V, Ta=25°C)
  Analog input: 2ch (internal: 1ch, external: 1ch)
- CPU command interface: 3-wired serial clock-synchronized (ML2272X)
  I2C interface (ML2276X)
- Maximum number of phrases: 4096 phrases, from 000h to 3FFh (1024 phrases/bank)
- Memory bank switching: Enabled between bank 1 and bank 4 using the SEL0 and SEL1 pins.
- Volume control: 32 levels (OFF is included) can be set by CVOL command.
  50 levels (OFF is included) can be set by AVOL command.
- Repeat function: LOOP commands
- Speech speed conversion function ×0.50 to ×2.00 (150 levels: 0.01 step)
- Pitch conversion function ±20% (40 levels: 1% step width)
- Source oscillation frequency: 4.096 MHz
- Power supply voltage: 2.7 to 3.6V / 4.5 to 5.5 V
- Operating temperature range: –40°C to +85°C
- Package: 30-pins plastic SSOP (SSOP30-P-56-0.65-K-MC)
- Product name: ML22725-xxxMB,ML22724-xxxMB, ML22723-xxxMB
  ML22765-xxxMB,ML22764-xxxMB, ML22763-xxxMB
  (xxx: ROM code No.)

The table below summarizes the differences from the ML2216 and ML22800 series.

Parameter	ML2216	ML22800 series	ML22725/ML22724/ ML22723-XXX	ML22765/ML22764/ ML22763-XXX
CPU interface	Serial	←	←	I2C
Playback method	4-bit Oki ADPCM2 8-bit straight PCM 8-bit nonlinear PCM 16-bit straight PCM	←	←	←
Maximum number of phrases	256	1024 (256/bank)	4096 (1024/bank)	←
Sampling frequency (kHz)	4.0/5.3/6.4/ 8.0/10.6/12.8 16.0	←	4.0/5.3/6.4/8.0/ 10.6/12.0/12.8/ 16.0/21.3/24.0/ 25.6/32.0/48.0	←
Clock frequency	4.096MHz (with a built-in crystal oscillator circuit)	←	←	←
D/A converter	12 bits	12 bits	16 bits	←
Low-pass filter	3rd order comb filter	3rd order comb filter	FIR interpolation filter	←
Speaker driving amplifier	Built-in 0.3W (8Ω, DV_{DD} = 5 V)	No	Built-in 0.7W (8Ω, DV_{DD} = 5 V)	←
Speech speed/pitch conversion	No	←	Yes	←
Edit ROM function	Yes	←	←	←
Volume control	16 levels	←	32 levels	←
Silence insertion	Yes 20 ms to 1024 ms (4 ms/step)	←	←	←
Repeat function	Yes	←	←	←
Interval at which a seam is silent during continuous playback (Note)	No	←	←	←
Power supply voltage	2.7 V to 5.5 V	2.7 V to 3.6 V	2.7 V to 5.5 V	←
Package	44-pin QFP	30-pin SSOP	←	←

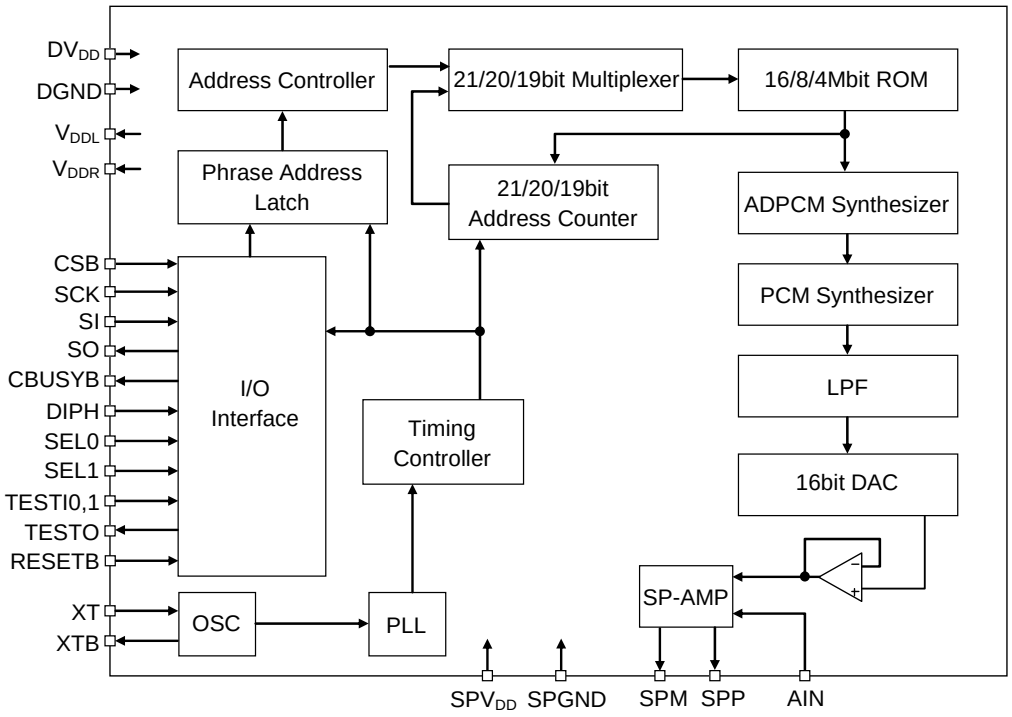
*1: Continuous playback as shown below is possible.



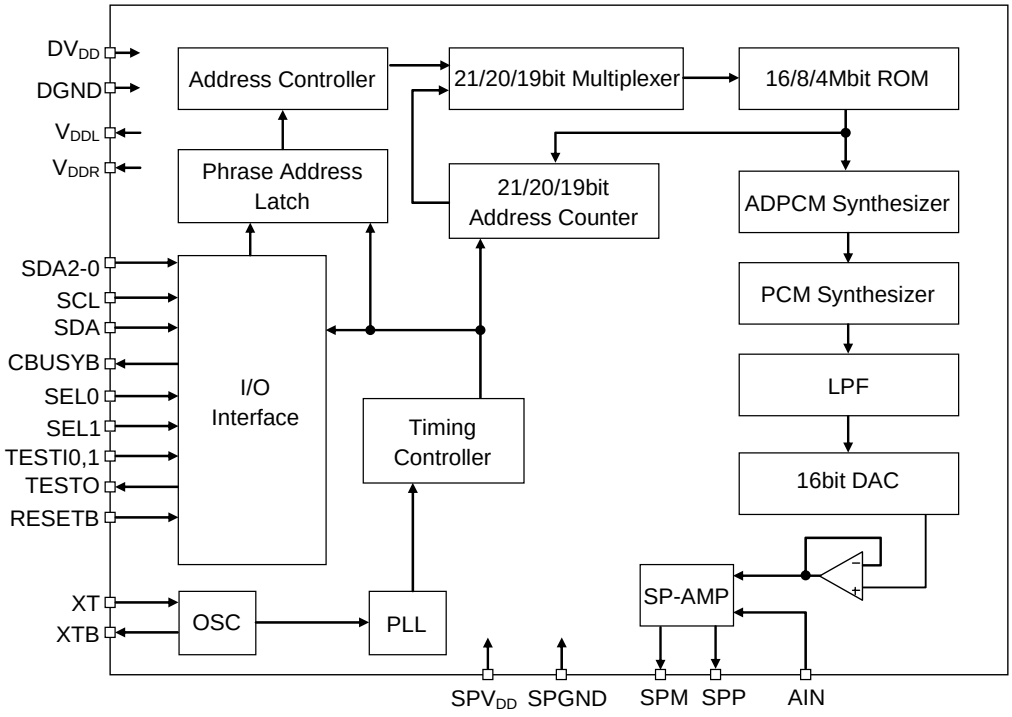
No silence interval

BLOCK DIAGRAMS

(ML22725/ML22724/ML22723-XXX)

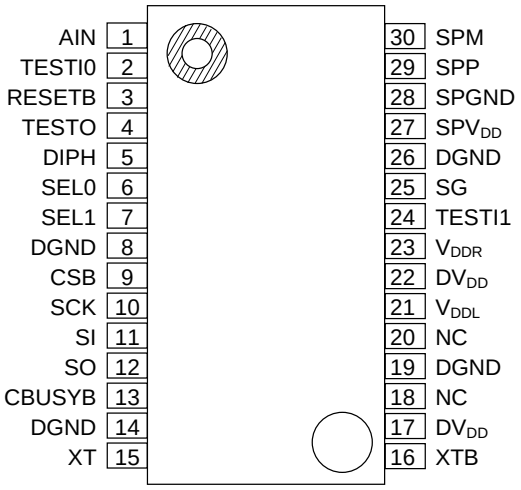


(ML22765/ML22764/ML22763-XXX)



PIN CONFIGURATIONS (TOP VIEW)

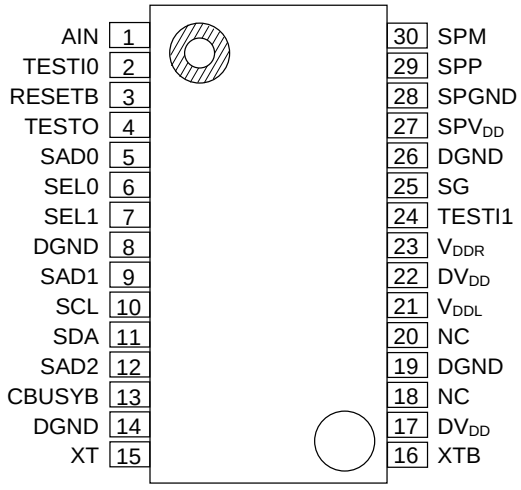
ML22725/ML22724/ML22723-XXXMB (Synchronous serial interface)



NC: No Connection

30-Pin Plastic SSOP

ML22765/ML22764/ML22763-XXXMB (I2C interface)



NC: No Connection

30-Pin Plastic SSOP

PIN DESCRIPTION (COMMON TO ALL PRODUCTS)

Pin	Symbol	I/O	Initial value (*1)	Description
1	AIN	I	0	Input pin for speaker amplifier.
2	TESTI0	I	0	Input pin for testing. Fix this pin to “L” level (DGND level). This pin has a pull-down resistor built in.
3	RESETB	I	0 (*2)	Input pin for reset.. At the “L” level, the LSI enters initial state. During reset, the entire circuitry stops and enters power down state. Input “L” level when power is supplied. After the power supply voltage is stable, drive this pin to “H” level. Then the entire circuitry can be powered up. This pin has a pull-up resistor built in.
4	TESTO	O	Hi-Z	Output pin for testing. Leave this pin open.
6, 7	SEL0 SEL1	I	0	Memory bank switching pins. Fix these pins to “L” level when the memory bank function is not used.
8, 14, 19, 26	DGND	—	—	Digital ground pin. Also serves as a ground pin for the internal memory.
13	CBUSYB	O	1	Output pin for command processing status.. This pin outputs “L” level during command processing. Any command should be entered when this pin is “H” level.
15	XT	I	0	Connect to the crystal or ceramic resonator. A feedback resistor around 1 MΩ is built in between this pin and the XTB pin. Use this pin if need to use an external clock. If the resonator is used, connect it as close to this pin as possible.
16	XTB	O	1	Connects to the crystal or ceramic resonator. When to use an external clock, leave this pin open. If the resonator is used, connect it as close to this pin as possible.
17, 22	DV_{DD}	—	—	Power supply pins for logic circuitry. Connect a capacitor of 0.1 μF or more between these pins and DGND pins.
18, 20	N.C	—	—	No-connected pins. Leave these pins open.
21	V_{DDL}	—	0	Regulator output pin for internal logic circuitry. Connect a capacitor recommended between this pin and DGND pin.
23	V_{DDR}	—	0	Regulator output pin for Built-in ROM. Connect a capacitor recommended between this pin and DGND pin.
24	TESTI1	I	0	Input pin for testing. Fix this pin to “L” level (DGND level). This pin has a pull-down resistor built in.
25	SG	—	0	Reference voltage output pin for the speaker amplifier built-in. Connect a capacitor recommended between this pin and DGND pin.
27	SPV_{DD}	—	—	Power supply pin for the speaker amplifier. Connect a bypass capacitor of 0.1 F or more between this pin and SPGND pin.
28	SPGND	—	—	Ground pin for the speaker amplifier.
29	SPP	O	0	Positive(+) output pin of the speaker amplifier built-in. Serves as the LINE output (*3), if built-in speaker amplifier is not used.
30	SPM	O	Hi-Z	Negative(-) output pin of the speaker amplifier built-in.

*1: Indicates the initial value during reset input or power down.
*2: “H” during power down.
*3: Outputs a voice signal before amplified by the speaker amplifier built-in.

PIN DESCRIPTION (FOR ML2272X SYNCHRONOUS SERIAL INTERFACE)

Pin	Symbol	I/O	Initial value (*1)	Description
5	DIPH	I	0	Set pin of the SCK clock edge. When this pin is “L” level, rising edge is available for input(SI) and falling edge is available for output(SO). When this pin is “H” level, falling edge is available for input(SI) and rising edge is available for output(SO).
9	CSB	I	1	Chip select pin. At the “L” level, data input/output is available.
10	SCK	I	0	Synchronous clock input pin for serial interface.
11	SI	I	0	Input pin of synchronous serial data. When the DIPH pin is “L” level, data is shifted in at the rising edges of the SCK clock pulses. When the DIPH pin is “H” level, data is shifted in at the falling edges of the SCK clock pulses.
12	SO	O	Hi-Z	Output pin of synchronous serial data. When the DIPH pin is “L” level, data is output at the falling edges of the SCK clock pulses. When the DIPH pin is “H” level, data is output at the rising edges of the SCK clock pulses. When the CSB pin is “H” level, this pin is Hi-Z state.

*1: Indicates the initial value during reset input or power down.

PIN DESCRIPTION (FOR ML2276X I2C INTERFACE)

Pin	Symbol	I/O	Initial value (*1)	Description
5, 9, 12	SAD0 SAD1 SAD2	I	0	Set pin of the slave address.
10	SCL	I	0	Clock input pin for I2C serial interface. This pin should be connected to pull-up resistor.
11	SDA	IO	0	Input/output pin for I2C serial data. Use for setting the mode of write/read and writing address, writing data or reading data. This pin should be connected to pull-up resistor. (N-ch MOS) open drain, when output mode. High impedance(Hi-Z), when input mode.

*1: Indicates the initial value during reset or power down.

ABSOLUTE MAXIMUM RATINGS

(DGND = SPGND = 0 V, Ta = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	DV_{DD}, SPV_{DD}	—	−0.3 to +7.0	V
Input voltage	V_{IN}	—	−0.3 to DV_{DD}+0.3	V
Power dissipation	P_D		938	mW
Output short-circuit current	I_{OS}	Applies to all pins except SPM, SPP, V_{DDL}, and V_{DDR}.	10	mA
		Applies to SPM and SPP pins.	300	mA
		Applies to V_{DDL} and V_{DDR} pins.	50	mA
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(DGND = SPGND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	DV_{DD}, SPV_{DD}	—	2.7 to 5.5			V
Operating temperature	T_{OP}	—	−40 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
External capacitors for crystal oscillator	Cd, Cg	—	15	30	45	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics (for the 3V applications)

DV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.86×DV_{DD}	—	DV_{DD}	V
"L" input voltage	V_{IL}	—	0	—	0.14×DV_{DD}	V
"H" output voltage 1	V_{OH1}	I_{OH} = –1 mA	DV_{DD}–0.4	—	—	V
"H" output voltage 2 (*1)	V_{OH2}	I_{OH} = –50 µA	DV_{DD}–0.4	—	—	V
"L" output voltage 1	V_{OL1}	I_{OL} = 2 mA	—	—	0.4	V
"L" output voltage 2 (*1)	V_{OL2}	I_{OL} = 50 µA	—	—	0.4	V
"L" output voltage 3 (*2)	V_{OL3}	I_{OL} = 3 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	µA
"H" input current 2 (*3)	I_{IH2}	V_{IH} = DV_{DD}	0.3	2.0	15	µA
"H" input current 3 (*4)	I_{IH3}	V_{IH} = DV_{DD}	2	30	200	µA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current 2 (*3)	I_{IL2}	V_{IL} = GND	–15	–2.0	–0.3	µA
"L" input current 3 (*5)	I_{IL3}	V_{IL} = GND	–200	–30	–2	µA
"H" output leak current 3 (*6)	I_{ILOH}	V_{OH} = DV_{DD}	—	—	10	µA
"L" output leak current 3 (*6)	I_{ILOL}	V_{OL} = GND	–10	—	—	µA
Supply current during playback	I_{DD}	f_{OSC} = 4.096 MHz No output load	—	—	20	mA
Power-down supply current	I_{DDS}	Ta = –40 to +40°C	—	1	10	µA
		Ta = –40 to +85°C	—	1	20	µA

*1: Applies to the XTB pin.
*2: Applies to the SCL and SDA pins.
*3: Applies to the XT pin.
*4: Applies to the TESTI0 pin.
*5: Applies to the RESETB pin.
*6: Applies to the TESTO pin.

DC Characteristics (for the 5V applications)

DV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.8×DV_{DD}	—	DV_{DD}	V
"L" input voltage	V_{IL}	—	0	—	0.2×DV_{DD}	V
"H" output voltage 1	V_{OH1}	I_{OH} = –1 mA	DV_{DD}–0.4	—	—	V
"H" output voltage 2 (*1)	V_{OH2}	I_{OH} = –50µA	DV_{DD}–0.4	—	—	V
"L" output voltage 1	V_{OL1}	I_{OL} = 2 mA	—	—	0.4	V
"L" output voltage 2 (*1)	V_{OL2}	I_{OL} = 50 µA	—	—	0.4	V
"L" output voltage 3 (*2)	V_{OL3}	I_{OL} = 3 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	µA
"H" input current 2 (*3)	I_{IH2}	V_{IH} = DV_{DD}	0.8	5.0	20	µA
"H" input current 3 (*4)	I_{IH3}	V_{IH} = DV_{DD}	20	100	400	µA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current 2 (*3)	I_{IL2}	V_{IL} = GND	–20	–5.0	–0.8	µA
"L" input current 3 (*5)	I_{IL3}	V_{IL} = GND	–400	–100	–20	µA
"L" output leak current 2 (*6)	I_{ILOH}	V_{OH} = DV_{DD}	—	—	10	µA
"L" output leak current 3 (*6)	I_{ILOL}	V_{OL} = GND	–10	—	—	µA
Supply current during playback	I_{DD}	f_{OSC} = 4.096 MHz No output load	—	—	25	mA
Power-down supply current	I_{DDS}	Ta = –40 to +40°C	—	1	15	µA
		Ta = –40 to +85°C	—	1	30	µA

*1: Applies to the XTB pin.
*2: Applies to the SCL and SDA pins.
*3: Applies to the XT pin.
*4: Applies to the TESTI0 pin.
*5: Applies to the RESETB pin.
*6: Applies to the TESTO pin.

Characteristics of Analog Circuitry (for the 3V applications)

DV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	—	15	20	25	kΩ
AIN input voltage range	V_{AIN}		—	—	DV_{DD}×2/3	Vp-p
LINE output load resistance	R_{LA}	During 1/2 DV_{DD} output	10	—	—	kΩ
LINE output voltage range	V_{AO}	No output load	DV_{DD}/6	—	DV_{DD}×5/6	V
SG output voltage	V_{SG}	—	0.95×V_{DDL}/2	V_{DDL}/2	1.05×V_{DDL}/2	V
SG output resistance	R_{SG}	During power down	57	96	135	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output power	P_{SPO}	SPV_{DD} = 3.3V, f = 1kHz R_{SPO} = 8Ω, THD≥10%	100	300	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0dB With a load of 8Ω	–50	—	+50	mV

Characteristics of Analog Circuitry (for the 5V applications)

DV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	—	15	20	25	kΩ
AIN input voltage range	V_{AIN}		—	—	DV_{DD}×2/3	Vp-p
LINE output load resistance	R_{LA}	During 1/2 DV_{DD} output	10	—	—	kΩ
LINE output voltage range	V_{AO}	No output load	DV_{DD}/6	—	DV_{DD}×5/6	V
SG output voltage	V_{SG}	—	0.95×V_{DDL}/2	V_{DDL}/2	1.05×V_{DDL}/2	V
SG output resistance	R_{SG}	During power down	57	96	135	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output power	P_{SPO}	SPV_{DD} = 5.0V, f = 1kHz R_{SPO} = 8Ω, THD≥10% Ta=25°C	500	700	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0dB With a load of 8Ω	–50	—	+50	mV

FUNCTIONAL DESCRIPTION

Synchronous Serial Command Interface (Applied to ML2272X)

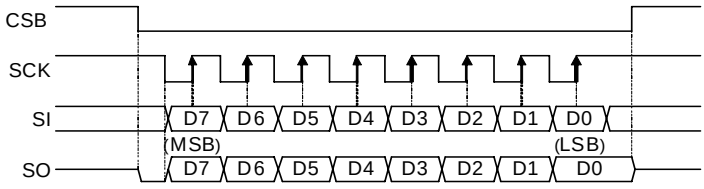
The CSB, SCK, SI, and SO pins are used to input the command data or to read the status. Driving the CSB pin to "L" level enables the serial CPU interface.
After the CSB pin is driven to "L" level, the command data are input through the SI pin from the MSB synchronized with the SCK clock. The command data shifts in through the SI pin at the rising or falling edge of the SCK clock pulse. Then, a command is executed at the rising or falling edge of the eighth pulse of the SCK clock.
As for status reading, status is output from the SO pin, synchronized with the SCK clock after the CSB pin is driven to "L" level.
The SCK clock edge is specified by the input level of the DIPH pin.

- When the DIPH pin is "L" level, rising edge is available for input from SI pin and falling edge is available for output from SO pin.
- When the DIPH pin is "H" level, falling edge is available for input from SI pin and rising edge is available for output from SO pin.

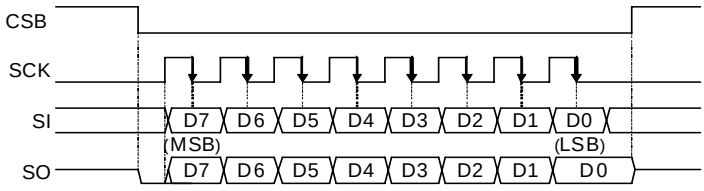
It is possible to input command data, even if the CSB pin is fixed by "L" level. However, if unexpected pulses caused by noise are induced through the SCK pin, SCK clock pulses are incorrectly counted, causing a failure in normal recognition of command. Then it is recommended that the CSB pin is "L" level only for command input.
The count of the SCK clock pulse is initialized when the CSB pin goes to "H" level.

Command Data Input or Status Read Timing

• When DIPH pin is "L" level



• When DIPH pin is "H" level



The following table shows the contents of each data output at a status read.

	Output status signal
MSB	—
7SB	—
6SB	—
5SB	BUSYB output
4SB	—
3SB	—
2SB	—
LSB	NCR output

The BUSYB output is “L” level when a command is being processed or playback is going on. In other states, the BUSYB output is “H” level. The NCR signal output is “L” level when a command is being processed or playback is in a standby state. In other states, the NCR output is “H” level.

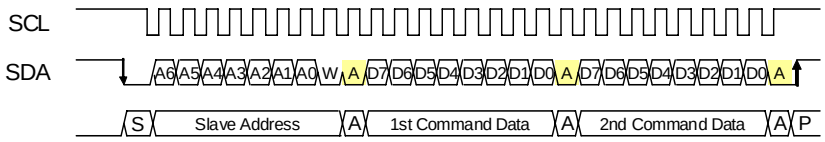
I2C Command Interface (Applied to ML2276X)

The I2C Interface built-in is an serial interface (: slave side) that is compliant with I2C bus specification. It supports Fast mode and enables data transmission/reception at 400 kbps. The SCL and SDA pins are used to input the command data or to read the status. Pins (:SAD0, 1 and 2) are used to set the slave address.
Pull-up resister should be connected to SCL pin and SDA pin.
For the master on the I2C bus to communicate with this device (: slave), input the slave address with the first seven bits after setting the start condition. The upper three bits of the slave address can be set using the SAD0 to 2 pins. The eighth bit of slave address is used to set the direction (: write or read) of communication. If the eighth bit is "0" level, it is write mode from master to slave. And, if the eighth bit is "1" level, it is read mode from master.
The communication is made in the unit of byte. And acknowledge is needed for each byte.

The protocol of I2C communication is shown below.

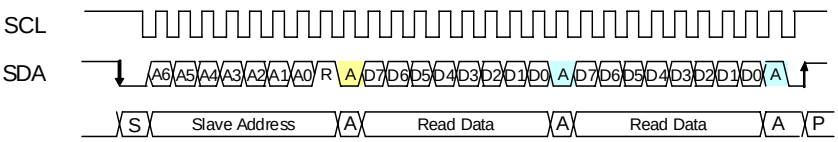
– Command flow at data write
  Start condition
  Slave address +W(0)
  Write address (ex. 1st byte of a command)
  Write data (ex. 2nd byte of a command)
  STOP condition

• Data write timing



– Command flow at the data read
  Start condition
  Slave address +R (1)
  Read data (ex. Status read)
  STOP condition

• Data read timing



Setting of the slave address using the SAD0 to 2 pins

SAD2	SAD1	SAD0	Lower 4 bits
0	0	0	0101
0	0	1	0101
0	1	0	0101
0	1	1	0101
1	0	0	0101
1	0	1	0101
1	1	0	0101
1	1	1	0101

The following table shows the contents of each data output at the status read. Status is updated by the RDSTAT command, therefore, be sure to input the RDSTAT command in order to read status.

	Output status signal
MSB	
7SB	
6SB	
5SB	BUSYB output (BUSYB0)
4SB	
3SB	
2SB	
LSB	NCR output (NCR0)

The BUSYB signal is “L” level when either a command is being processed or the playback of a particular channel is going on. In other states, the BUSYB signal is “H” level. The NCR signal is “L” level when either a command is being processed or a particular channel is in standby for playback. In other states, the NCR signal is “H” level.

Command List

Each command is configured in 1-byte (8-bit) units. Each of the AMODE, AVOL FADR, PLAY, MUON, CVOL, VPITCH, and VSPD commands forms one command by two bytes.

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP	0	0	0	0	0	0	S1	S0	Power-up command. shift from the power down state to the command waiting state. Also, sets the number of memory banks.
PDWN	0	0	1	0	0	0	0	0	Power-down command. shift from the command waiting state to the power down state.
RDSTAT	1	0	1	1	0	0	0	0	Status read command. Read the command status of each channel.
AMODE	0	0	0	0	0	1	0	0	Control command of analog circuitry. Set operation of power-up/dpwn and input/output.
	FAD	DAG1	DAG0	AIG1	AIG0	DAEN	SPEN	POP	
PLAY	0	1	0	0	F9	F8	0	0	Playback start command. Use the data of the 2nd byte to specify a phrase number.
	F7	F6	F5	F4	F3	F2	F1	F0	
STOP	0	1	1	0	0	0	0	0	Playback stop command.
FADR	0	0	1	1	F9	F8	0	0	Set command of playback phrase. Use START command to start.
	F7	F6	F5	F4	F3	F2	F1	F0	
START	0	1	0	1	0	0	0	0	Playback start command without phrase spec. Use FADR command to set phrase. After played back by PLAY command, the same phrase can be played back with this command.
MUON	0	1	1	1	0	0	0	0	Silence insertion command. Set the silent time length using M7 to M0 bits in the 2nd byte.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	0	0	0	0	0	Set command of repeat playback. Setting is enabled during playback.
CLOOP	1	0	0	1	0	0	0	0	Stop command of repeat playback. Also, repeat playback is released by STOP command automatically.
CVOL	1	0	1	0	0	0	0	0	Volume control command. Set volume using CV4 to CV0 bits in the 2nd byte.
	0	0	0	CV4	CV3	CV2	CV1	CV0	
AVOL	0	0	0	0	1	0	0	0	Analog volume control command. Set volume using AV5 to AV0 bits.
	0	0	AV5	AV4	AV3	AV2	AV1	AV0	
VPITCH	1	1	1	0	0	0	0	0	Pitch conversion command. Can be specified pitch.
	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	
VSPD	1	1	0	1	0	0	0	0	Speech speed conversion command. Can be specified speed.
	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	

Voice Synthesis Algorithm

Four types of voice synthesis algorithm are supported. They are OKI 4-bit ADPCM2, OKI 8-bit non-linear PCM, 8-bit straight PCM and 16-bit straight PCM. Select the best one according to the characteristics of playback voice.

The following table shows key features of each algorithm.

Voice synthesis algorithm	Applied waveform	Feature
OKI 4-bit ADPCM2	Normal voice waveform	Up version of OKI's specific voice synthesis algorithm (:OKI 4-bit ADPCM). Voice quality is improved.
OKI 8-bit Nonlinear PCM	Waveform including high frequency signals (sound effect, etc.)	Algorithm which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit straight PCM		Normal 8-bit PCM algorithm.
16-bit straight PCM		Normal 16-bit PCM algorithm,

Memory Allocation and Creating Voice Data

The ROM is partitioned into four data areas: voice (i.e., phrase) control area, test area, voice area, and edit ROM area.
The voice control area manages the voice data in the ROM. It contains data for controlling the start/stop addresses of voice data for 1,024 phrases, use/non-use of the edit ROM function and so on.
The test area contains data for testing.
The voice area contains actual waveform data.
The edit ROM area contains data for effective use of voice data. For the details, refer to the section of "Edit ROM Function."
The edit ROM area is not available if the edit ROM is not used.

The ROM data is created using a dedicated tool.

Configuration of ROM data

0x00000 0x01FFF	Voice control area (Fixed 64 Kbits)
0x02000 0x0205F	Test area
0x02060 max: 0x1FFFFF	Voice area
max: 0x1FFFFF	Edit ROM area Depends on creation of ROM data.

Playback Time and Memory Capacity

The playback time depends on the memory capacity, sampling frequency, and playback method.
The equation to know the playback time is shown below. But this is not applied if the edit ROM function is used.

$$\text{Playback time [sec]} = \frac{1.024 \times (\text{Memory capacity} - 64.75\ [\text{Kbits}])}{\text{Sampling frequency [kHz]} \times \text{Bit length}}$$

(Bit length is 4 at the 4-bit ADPCM2 and 8/16 at the PCM.)

Example) In the case that the sampling frequency is 16 kHz, algorithm is 4-bit ADPCM2 and ROM capacity is 16 Mbits, the playback time is approx. 261 seconds, as shown below.

$$\text{Playback time} = \frac{1.024 \times (16834 - 64.75)\ [\text{Kbits}]}{16\ [\text{kHz}] \times 4\ [\text{bits}]} \cong 261\ [\text{sec}]$$

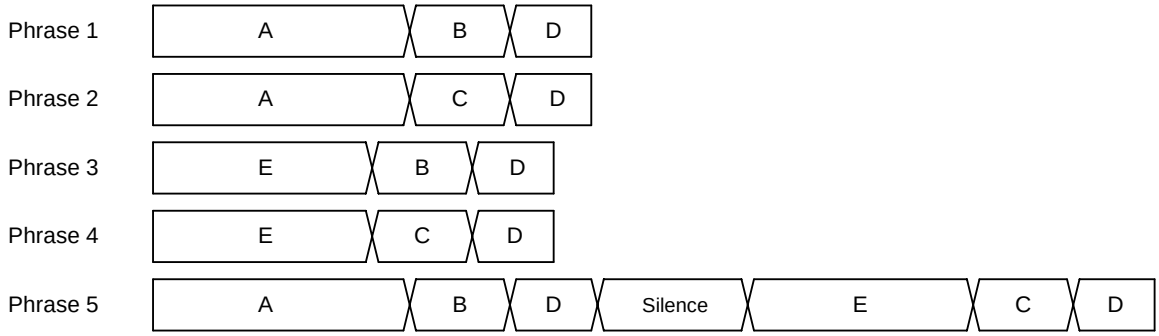
Edit ROM Function

The edit ROM function makes it possible to play back multiple phrases in succession. The following functions are set using the edit ROM function:

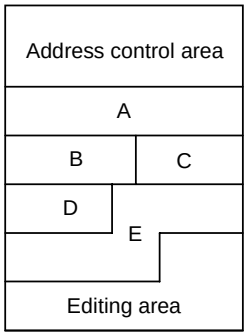
- Continuous playback: There is no limit to set the number of times of continuous playback. It depends on the memory capacity only.
- Silence insertion: 20ms to 1,024 ms

It is possible to use voice ROM effectively to use the edit ROM function.
Below is an example of the ROM structure, case of using the edit ROM function.

Example 1) Phrases using the Edit ROM Function



Example 2) Structure of the ROM that contents of example 1 are stored



Memory Bank Switching Function

The memory bank switching function enables the the built-in ROM area that is divivided into up to four banks to be used. When four banks are used, the maximum number of phrases per bank is 1024 so that up to 4096 phrases can be played back.
Using this function, multiple ROM codes can be grouped into one code.
The settings of SEL1 pin and SEL0 pin determines which memory bank is used. To playback phrases, the number of memory banks must be specified in PUP.

When using a memory bank switching function, data must be divided and saved in the specified areas at ROM data creation.

– When the number of memory banks is 1

SEL1	SEL0	ML22725-XXX ML22765-XXX	ML22724-XXX ML22764-XXX	ML22723-XXX ML22763-XXX
0	0	00000h – 1FFFFFh	00000h – FFFFFh	00000h -7FFFFh

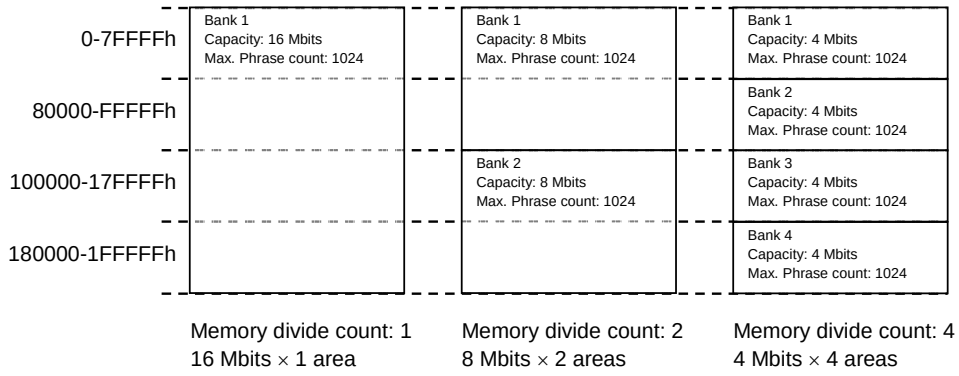
– When the number of memory banks is 2

SEL1	SEL0	ML22725-XXX ML22765-XXX	ML22724-XXX ML22764-XXX	ML22723-XXX ML22763-XXX
0	0	00000h – FFFFFh	00000h – 7FFFFh	00000h – 3FFFFh
0	1	100000h – 1FFFFFh	80000h – FFFFFh	40000h – 7FFFFh

– When the number of memory banks is 4

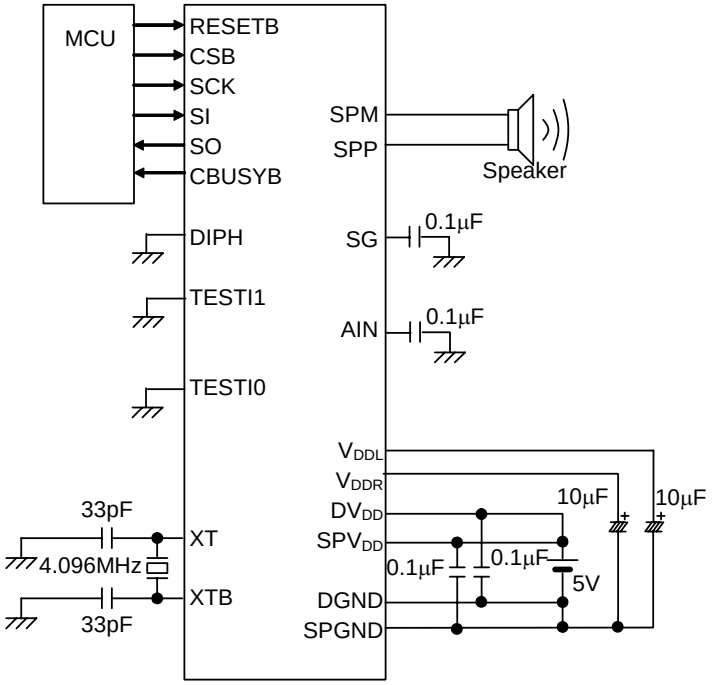
SEL1	SEL0	ML22725-XXX ML22765-XXX	ML22724-XXX ML22764-XXX	ML22723-XXX ML22763-XXX
0	0	00000h – 7FFFFh	00000h – 3FFFFh	00000h – 1FFFFh
0	1	80000h – FFFFFh	40000h – 7FFFFh	20000h – 3FFFFh
1	0	100000h – 17FFFFh	80000h – BFFFFh	40000h – 5FFFFh
1	1	180000h – 1FFFFFh	C0000h – FFFFFh	60000h – 7FFFFh

The memory (16 Mbits) in the ML22725 is divided as shown below.

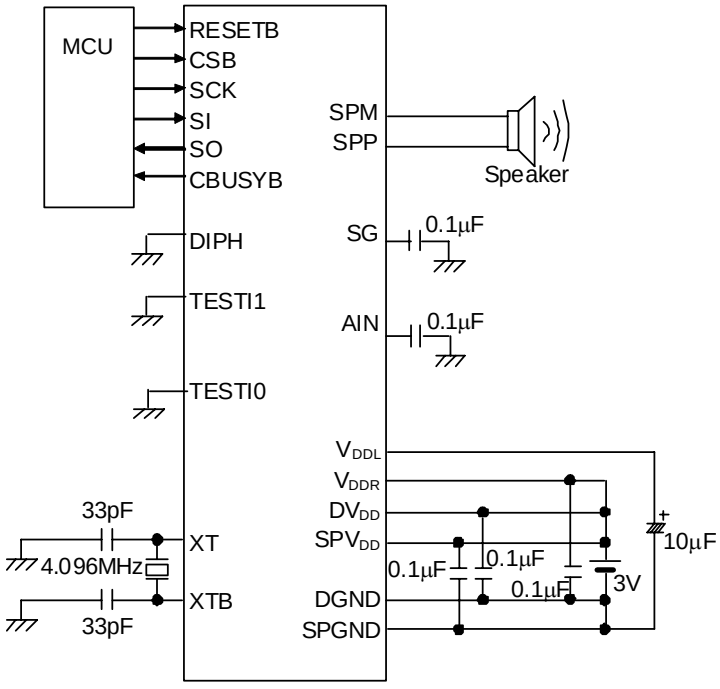


APPLICATION CIRCUIT

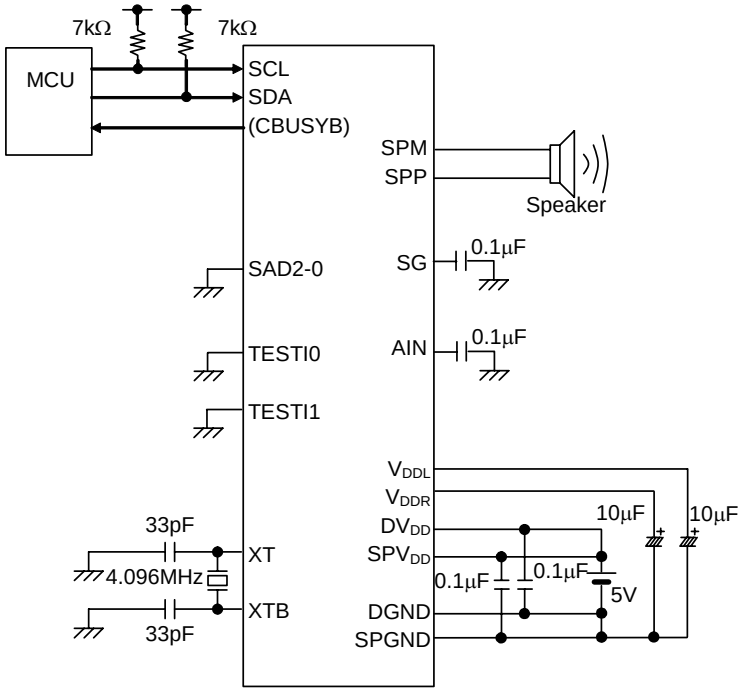
ML2272X: DV_{DD}=SPV_{DD}=5V



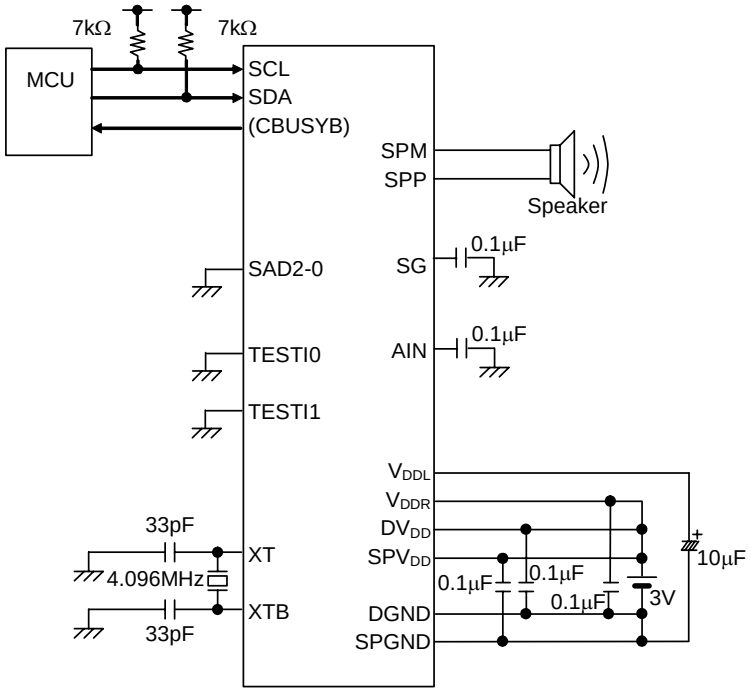
ML2272X: DV_{DD}=SPV_{DD}=3V



ML2276X: DV_{DD}=SPV_{DD}=5V

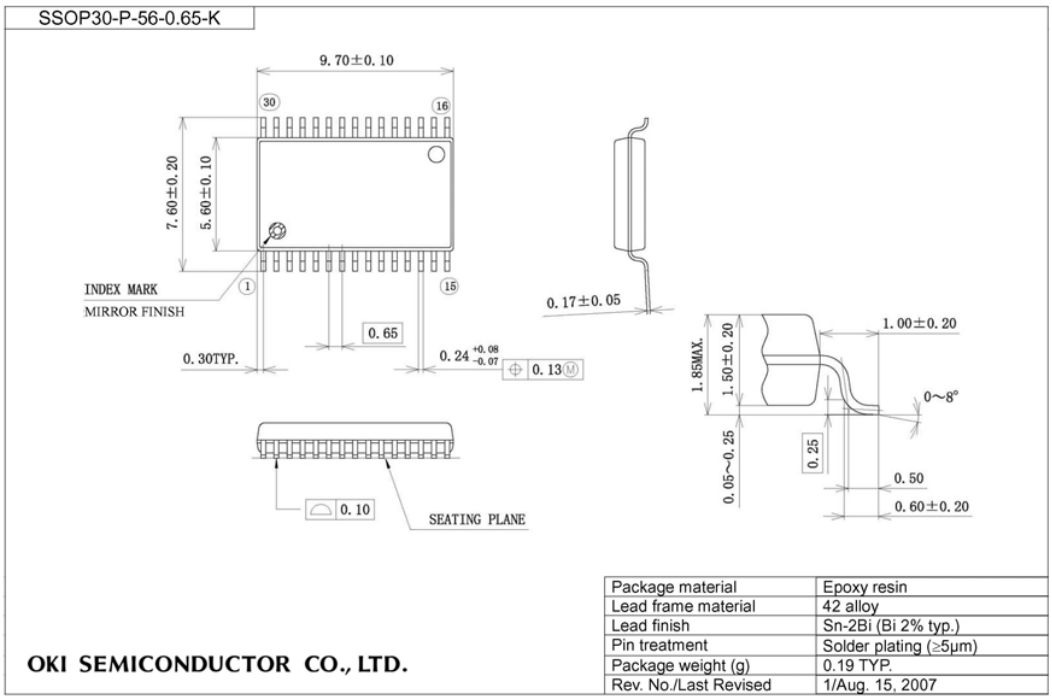


ML2276X: DV_{DD}=SPV_{DD}=3V



PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.19 TYP.
Rev. No./Last Revised	1/Aug. 15, 2007

Notes for Mounting the Surface Mount Type Package:

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact OKI's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL2272X FULL-01	Dec. 17, 2007	–	–	Preliminary edition 1
FEDL227XXDIGEST-01	Apr. 18, 2008	–	–	Final edition 1
FEDL227XXDIGEST-02	May. 29, 2008	–	–	Final edition 2
FEDL227XXDIGEST-03	Mar. 25, 2009	5,6	5,6	Common terminal explanation attribute change (TESTI1,SPP,SPM)
		11	11	Max value change within the range of LINE output voltage
		12	12	Min, Typ, and Max value change of CBUSYB ("L" level output time)
		17	17	Bit name of AMODE command (PUP->POP)
		21,22	21,22	Modify application circuit

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