SM802112

ClockWorks™ 3-Output, 480MHz/80MHz, Ultra-Low Jitter LVDS/CMOS Frequency Synthesizer

General Description

The SM802112 is a member of the ClockWorks™ family of devices from Micrel and provides extremely low-noise clock signals. It is based upon a unique patented RotaryWave® architecture that provides very-low phase noise.

The device operates from a 3.3V or 2.5V power supply and synthesizes two LVDS output clocks, one at 480MHz and one at 80MHz and one LVCMOS clock at 80MHz. The SM802112 accepts an 80MHz LVCMOS reference clock or an 80MHz 1Vp-p sine wave.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

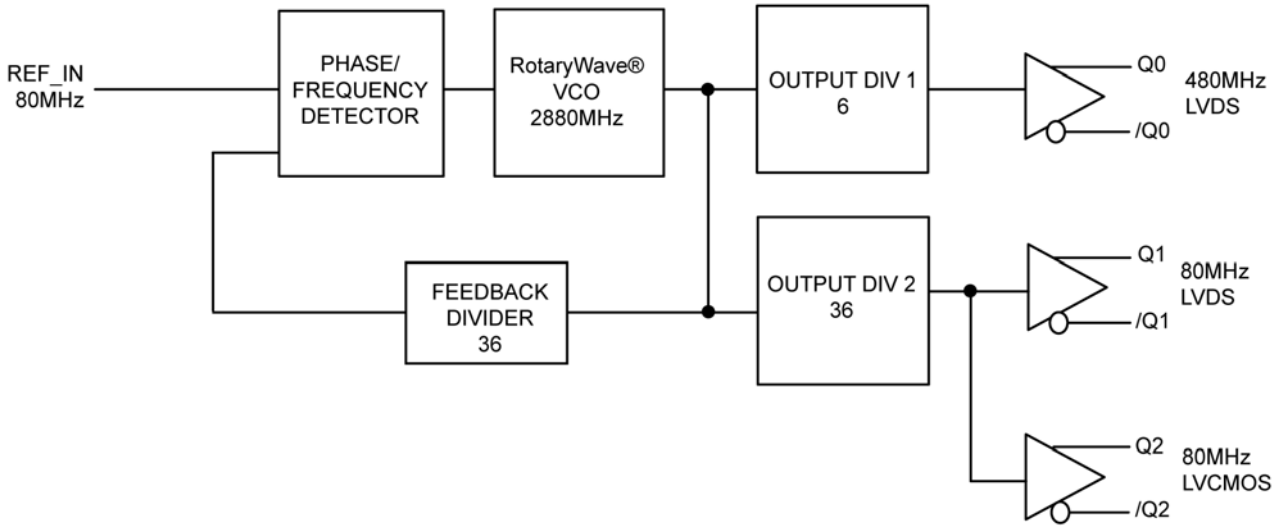
Features

- Generates two LVDS clock outputs, one at 480MHz and one at 80MHz
- Generates one LVCMOS clock output at 80MHz
- 2.5V or 3.3V operating range
- Typical phase jitter @ 480MHz (12kHz to 20MHz): 290fs
- Industrial temperature range (–40°C to +85°C)
- Green, RoHS, and PFOS compliant
- Available in 44-pin 7mm × 7mm QFN package

Applications

- Set Top Box

Block Diagram



ClockWorks is a trademark of Micrel, Inc
RotaryWave is a registered trademark of Multigig, Inc.

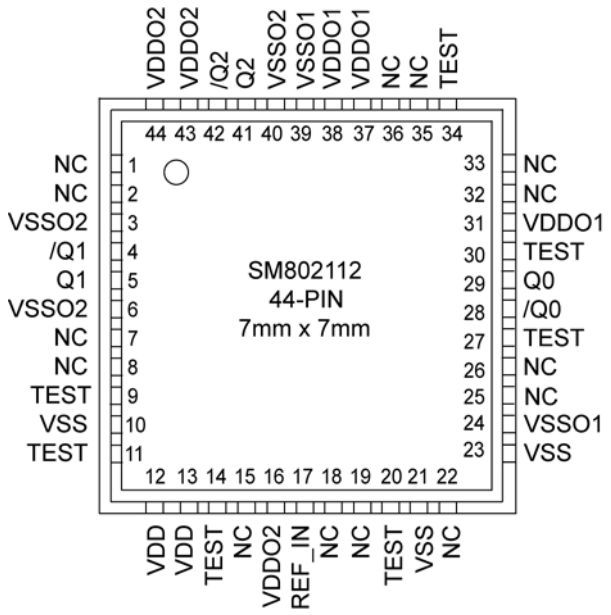
Ordering Information[1]

Part Number	Marking	Shipping	Temperature Range	Package
SM802112UMG	802112	Tray	–40°C to +85°C	44-Pin QFN
SM802112UMGTR	802112	Tape and Reel	–40°C to +85°C	44-Pin QFN

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



44-Pin QFN
(Top View)

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
28, 29	/Q0, Q0	O, (DIF)	LVDS	Differential Clock Output from Bank 1, 480MHz.
4, 5	/Q1, Q1	O, (DIF)	LVDS	Differential Clock Output from Bank 2, 80MHz.
42, 41	/Q2, Q2	O, (DIF)	LVCMOS	Differential Clock Output from Bank 2, 80MHz.
12, 13	VDD	PWR		Power Supply.
31, 37, 38	VDDO1	PWR		Power Supply for Output Q0.
16, 43, 44	VDDO2	PWR		Power Supply for Outputs Q1, Q2.
10, 21, 23	VSS (Exposed Pad)	PWR		Core Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
24, 39	VSSO1	PWR		Power Supply Ground for Outputs Q0.
3, 6, 40	VSSO2	PWR		Power Supply Ground for Outputs Q1, Q2.

Pin Description (Continued)

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
17	REF_IN	I, SE	LVCMOS	Reference Clock Input, 80MHz.
9, 11, 14, 20, 27, 30, 30	TEST			Factory Test Pins. Do not connect anything to these pins.
1, 2, 7, 8, 15, 18, 19, 22, 25, 26, 32, 33, 35, 36	NC			No Connect. Do not connect anything to these pins.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}, $V_{DDO1/2}$) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.50V to V_{DD} + 0.5V
Lead Temperature (soldering, 20s) ..... 260°C
Case Temperature ..... 115°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{DD}, $V_{DDO1/2}$) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance[3]
QFN (θ_{JA})
Still-Air ..... 24°C/W
QFN (ψ_{JB})
Junction-to-Board ..... 8°C/W

DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, $V_{DDO1/2}$	2.5V Operating Voltage		2.375	2.5	2.625	V
V_{DD}, $V_{DDO1/2}$	3.3V Operating Voltage		3.135	3.3	3.465	V
I_{DD}	Supply current V_{DD} + V_{DDO}	Outputs open		125	158	mA

LVDS DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C. R_L = 100Ω across Q and /Q.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage	Figures 1, 4	275	350	475	mV
ΔV_{OD}	V_{OD} Magnitude Change				40	mV
V_{OS}	Offset Voltage		1.15	1.25	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table(s) after thermal equilibrium has been established.

LVCMOS OUTPUT DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C. R_L = 50Ω to V_{DDO}/2.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	Figure 5	V_{DD0} – 0.7			V
V_{OL}	Output Low Voltage	Figure 5			0.6	V

REF_IN DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		1.1		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.6	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	–5		5	µA

AC Electrical Characteristics[4, 5]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency	Q0 Output		480		MHz
		Q1, Q2 Outputs		80		
F_{REF}	Reference Input Frequency			80		MHz
T_R/T_F	LVDS Output Rise/Fall Time	20% – 80%	100	250	400	ps
	LCMOS Output Rise/Fall Time	20% – 80%	100	250	500	
ODC	Output Duty Cycle	LVDS Outputs	48	50	52	%
		LVCMOS Output	45	50	55	
T_{SKEW}	Output-to-Output Skew	Q1 to Q2, Note 6		60	150	ps
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter[7]	480MHz LVDS Integration Range (1kHz – 100MHz)		300	600	fs
		80MHz LVDS, LVCMOS Integration Range (1kHz – 20MHz)		290	600	
Phase Noise	Input Phase Noise	80MHz Input Frequency Offset Frequency: 1kHz 10kHz 100kHz 1MHz			 –124 –135 –143 –145	dBc
Phase Noise	Output Phase Noise	480MHz Output Frequency Offset Frequency: 1kHz 10kHz 100kHz 1MHz 10MHz 20MHz 100MHz			 –105 –115 –120 –120 –150 –154 –160	dBc
	Spurious Noise Components	80MHz for Q0 480MHz		–58	-48	dBc

Notes:

5. All phase noise measurements were taken with an Agilent 5052B phase noise system.
6. Defined as skew between outputs at the same supply voltage and temperature. Measured as the difference of the output differential crossing point of Q1 and /Q1 80MHz LVDS, and the 50% point of LVCMOS Q2. LVCMOS Q2 and /Q2 are both ac coupled into 50 ohms.
7. REF_IN driven with a low-noise source, ClockWorks SM802001 programmed for an 80MHz CMOS output. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz. Measured with input noise of 1kHz -126dBc, 10kHz -136dBc, 100kHz -143dBc, 1MHz -146dBc.

Application Information

REF_IN Input

For a $1V_{P-P}$ sine wave signal applied to REF_IN with the part operating at 3.3V, AC couple REF_IN with a 50Ω termination of 206Ω to V_{DD} and 66Ω to ground, close to the input. This provides 50Ω Thevenin termination and a DC voltage of 0.8V.

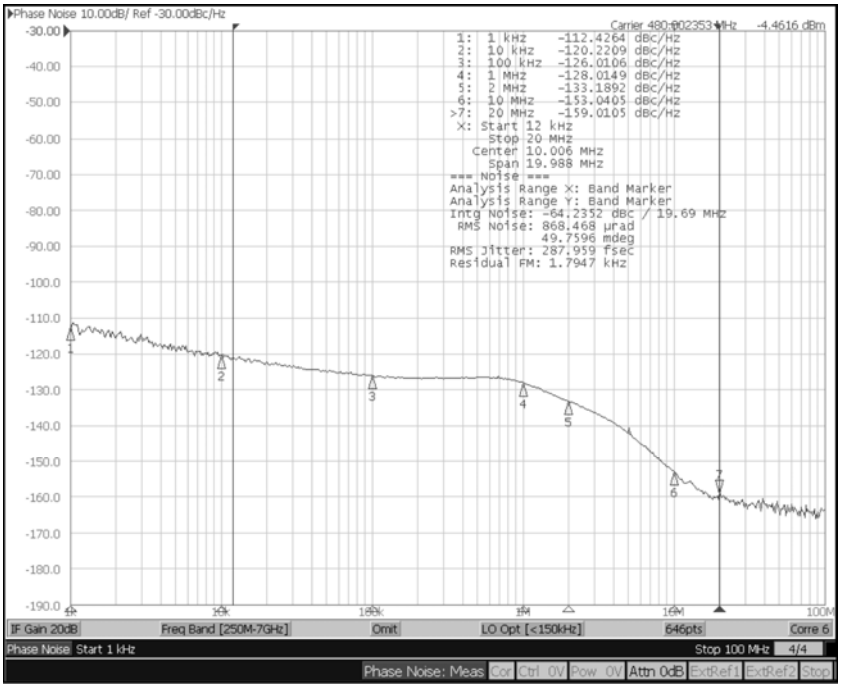
LVDS Outputs

LVDS outputs are to be terminated with 100Ω across Q and /Q. For best performance load all outputs. You can DC or AC-couple the outputs.

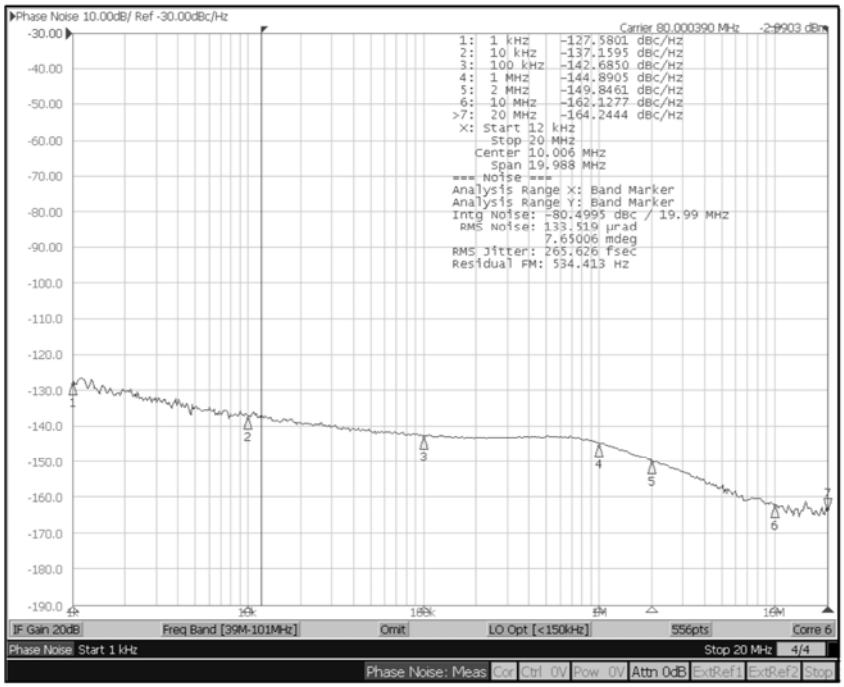
LVCMOS Outputs

LVCMOS output Q2 and /Q2 are 80MHz complimentary outputs to reduce switching noise. Terminate both outputs with identical loads to minimize noise.

Phase Noise Plots

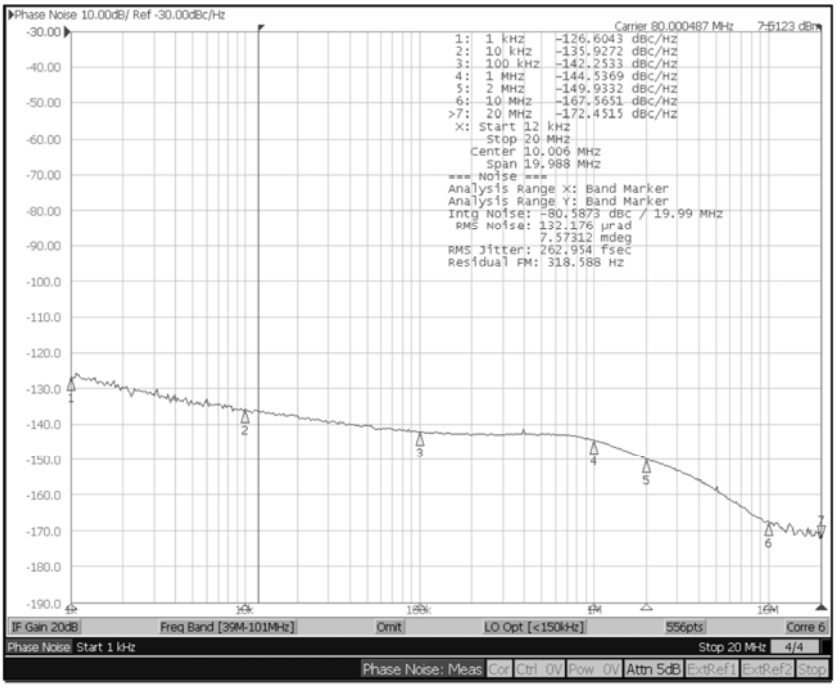


Phase Noise Plot: 480MHz LVDS



Phase Noise Plot: 80MHz LVDS

Phase Noise Plots (Continued)



Phase Noise Plot: 80MHz LVCMOS

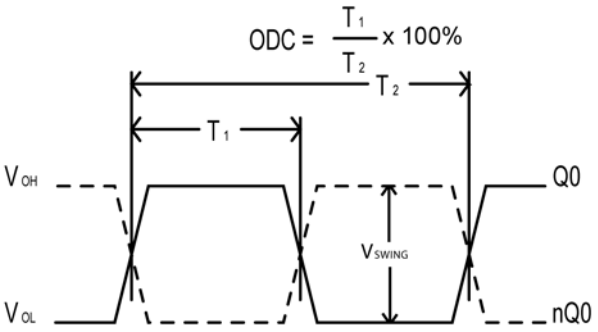


Figure 1. Duty Cycle Timing

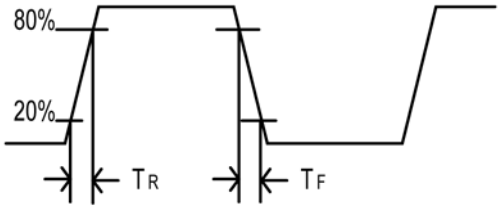


Figure 2. All Outputs Rise/Fall Time

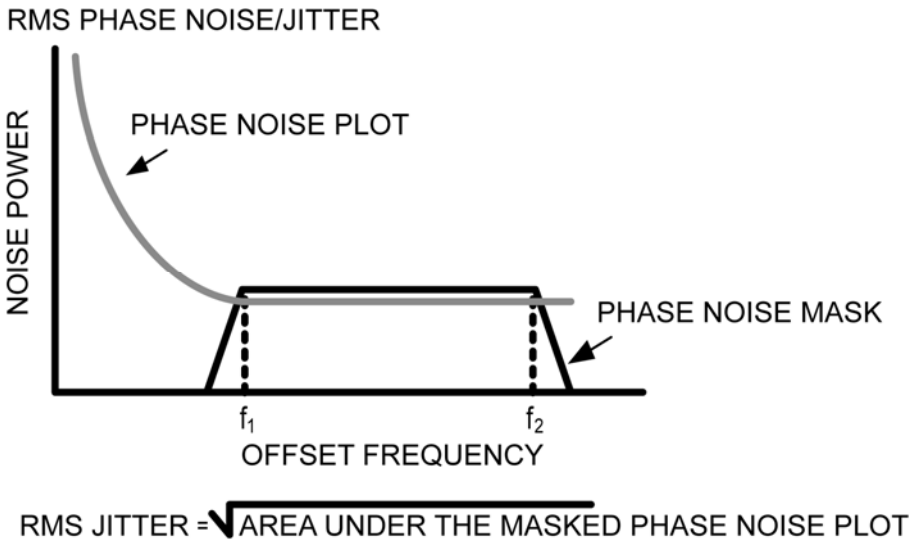


Figure 3. RMS Phase/Noise Jitter

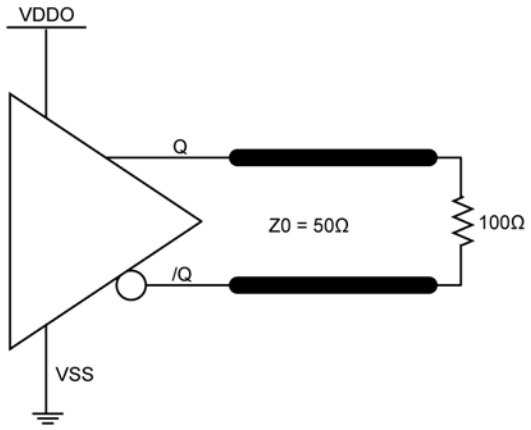


Figure 4. LVDS Output Load and Test Circuit

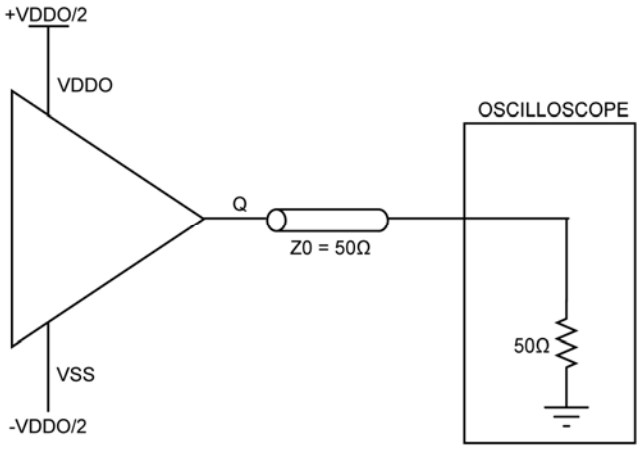
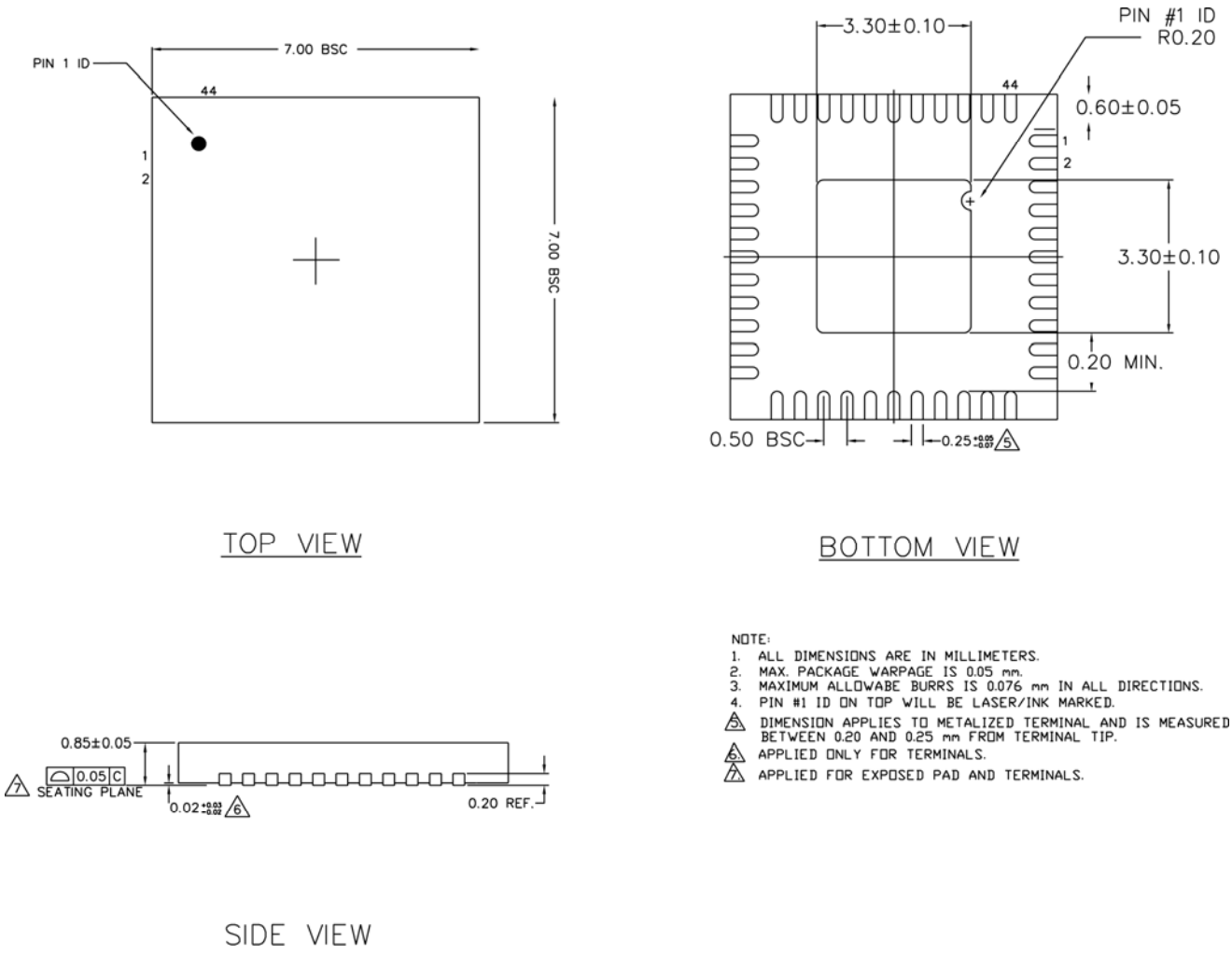


Figure 5. LVCMOS Output Test Load

LVDS and LVCMOS Output Load and Test Circuit

Package Information



44-Pin QFN

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