



# SM802101

## ClockWorks™ PCI-e Octal 100MHz/200MHz Ultra-Low Jitter, HCSL Frequency Synthesizer

### General Description

The SM802101 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution for PCI-Express clock signals. It is based upon a unique patented architecture that provides very-low phase noise.

The device operates from a 3.3V or 2.5V power supply and synthesizes eight HCSL output clocks at 100MHz or 200MHz. The SM802101 accepts a 25MHz crystal or LVCMOS reference clock.

Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).



ClockWorks™

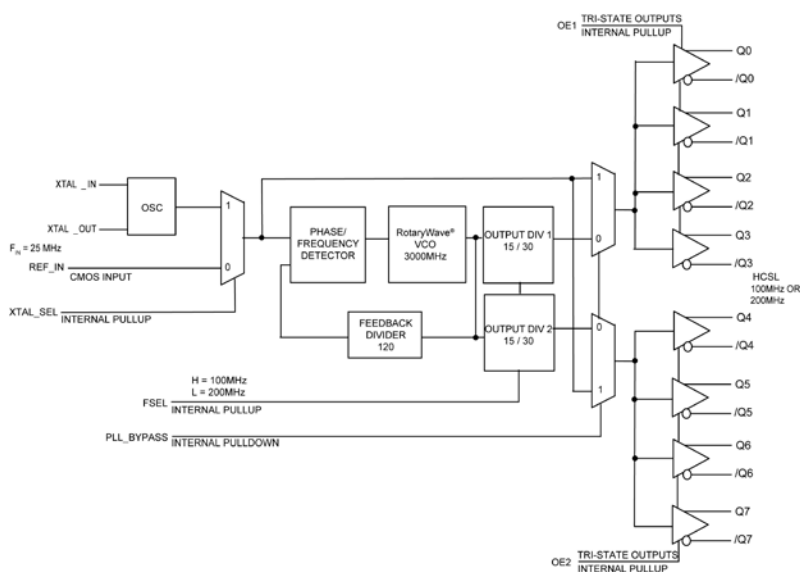
### Features

- Generates eight HCSL clock outputs at 100MHz or 200MHz
- 2.5V or 3.3V operating range
- Typical phase jitter @ 100MHz (1.875MHz to 20MHz): 105fs
- Industrial temperature range (-40°C to +85°C)
- Green, RoHS, and PFOS compliant
- Available in 44-pin 7mm × 7mm QFN package

### Applications

- PCI-Express

### Block Diagram



ClockWorks is a trademark of Micrel, Inc.

Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax + 1 (408) 474-1000 • <http://www.micrel.com>

March 27, 2013

Revision 1.3  
[hbwhelp@micrel.com](mailto:hbwhelp@micrel.com) or (408) 955-1690

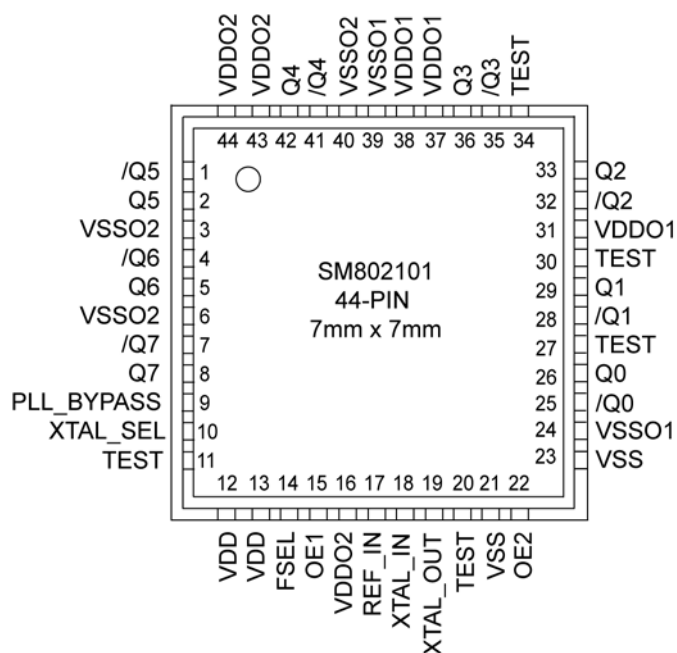
## Ordering Information<sup>(1)</sup>

Part Number	Marking	Shipping	Temperature Range	Package
SM802101UMG	802101	Tray	-40°C to +85°C	44-Pin QFN
SM802101UMGR	802101	Tape and Reel	-40°C to +85°C	44-Pin QFN

**Note:**

1. Devices are Green, RoHS, and PFOS compliant.

## Pin Configuration



**44-Pin QFN  
(Top View)**

## Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1, 2	/Q5, Q5	O, (DIF)	HCSL	Differential Clock Output
4, 5	/Q6, Q6			
7, 8	/Q7, Q7			
25, 26	/Q0, Q0			
28, 29	/Q1, Q1			
32, 33	/Q2, Q2			
35, 36	/Q3, Q3			
41, 42	/Q4, Q4			

**Pin Description (Continued)**

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
14	FSEL	I, (SE)	LVC MOS	Frequency Select, 1 = 100MHz, 0 = 200MHz, 45K $\Omega$ pull-up
12, 13	VDD	PWR		Power Supply
31, 37, 38	VDDO1	PWR		Power Supply for Outputs Q0 – Q3
16, 43, 44	VDDO2	PWR		Power Supply for Outputs Q4 – Q7
21, 23	VSS (Exposed Pad)	PWR		Core Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
24, 39	VSSO1	PWR		Power Supply Ground for Q0 – Q3
3, 6, 40	VSSO2	PWR		Power Supply Ground for Outputs Q4 – Q7
9	PLL_BYPASS	I, (SE)	LVC MOS	PLL Bypass, Selects Output Source 0 = Normal PLL Operation 1 = Output from Input Reference Clock or Crystal 45K $\Omega$ pull-down
10	XTAL_SEL	I, (SE)	LVC MOS	Selects PLL Input Reference Source 0 = REF_IN, 1 = XTAL, 45K $\Omega$ pull-up
11, 20, 27, 30, 34	TEST			Factory Test pins, Do not connect anything to these pins.
17	REF_IN	I, (SE)	LVC MOS	Reference Clock Input
18	XTAL_IN	I, (SE)	10pF crystal	Crystal Reference Input, no load caps needed (see Figure 5).
19	XTAL_OUT	O, (SE)	10pF crystal	Crystal Reference Output, no load caps needed (see Figure 5).
15	OE1	I, (SE)	LVC MOS	Output Enable, Outputs Q0 – Q3 disable to tri-state, 0 = Disabled, 1 = Enabled, 45K $\Omega$ pull-up
22	OE2	I, (SE)	LVC MOS	Output Enable, Outputs Q4 – Q7 disable to tri-state, 0 = Disabled, 1 = Enabled, 45K $\Omega$ pull-up

**Truth Tables**

PLL_BYPASS	XTAL_SEL	OE2	OE1	INPUT	OUTPUT
0	–	1	1	–	PLL
1	–	1	1	–	XTAL/REF_IN
–	0	1	1	REF_IN	–
–	1	1	1	XTAL	–
–	–	0	1	–	Q4-Q7 Tri-state
–	–	1	0	–	Q0-Q3 Tri-state

FSEL	Output Frequency (MHz)
0	200
1	100

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage ( $V_{DD}$ , $V_{DDO1/2}$ )	+4.6V
Input Voltage ( $V_{IN}$ )	-0.50V to $V_{DD} + 0.5V$
Lead Temperature (soldering, 20s)	260°C
Case Temperature	115°C
Storage Temperature ( $T_s$ )	-65°C to +150°C

### Operating Ratings<sup>(2)</sup>

Supply Voltage ( $V_{DD}$ , $V_{DDO1/2}$ )	+2.375V to +3.465V
Ambient Temperature ( $T_A$ )	-40° C to +85°C
Junction Thermal Resistance <sup>(3)</sup>	
QFN ( $\theta_{JA}$ )	
Still-Air	24°C/W
QFN ( $\psi_{JB}$ )	
Junction-to-Board	8°C/W

### DC Electrical Characteristics<sup>(4)</sup>

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$   
 $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO1/2} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$   
 $T_A = -40^\circ C$  to  $+85^\circ C$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{DD}$ , $V_{DDO1/2}$	2.5V Operating Voltage		2.375	2.5	2.625	V
$V_{DD}$ , $V_{DDO1/2}$	3.3V Operating Voltage		3.135	3.3	3.465	V
$I_{DD}$	Supply current $V_{DD} + V_{DDO}$	Eight Outputs enabled, 100MHz Outputs 50Ω to $V_{SS}$		217	270	mA
		Eight Outputs enabled, 200MHz Outputs 50Ω to $V_{SS}$		229	285	
		Four Outputs enabled, 100MHz Outputs 50Ω to $V_{SS}$ , OE1 or OE2 = 0		149	185	
		Four Outputs enabled, 200MHz Outputs 50Ω to $V_{SS}$ , OE1 or OE2 = 0		158	197	

### HCSL DC Electrical Characteristics<sup>(4)</sup>

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$   
 $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO1/2} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$   
 $T_A = -40^\circ C$  to  $+85^\circ C$ .  $R_L = 50\Omega$  to  $V_{SS}$

Symbol	Parameter	Condition	Min	Typ.	Max.	Units
$V_{OH}$	Output High Voltage		660	700	850	mV
$V_{OL}$	Output Low Voltage		-150	0	27	mV
$V_{CROSS}$	Crossing Point Voltage		250	350	550	mV

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table(s) after thermal equilibrium has been established.

## LVC MOS (PLL\_BYPASS, XTAL\_SEL, FSEL, OE1, OE2) DC Electrical Characteristics<sup>(4)</sup>

$V_{DD} = 3.3V \pm 5\%$ , or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	$V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	$V_{DD} = 3.465V, V_{IN} = 0V$	-150			$\mu A$

## REF\_IN DC Electrical Characteristics<sup>(4)</sup>

$V_{DD} = 3.3V \pm 5\%$ , or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{IH}$	Input High Voltage		1.1		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.6	V
$I_{IN}$	Input Current	$XTAL\_SEL = V_{IL}, V_{IN} = 0V$ to $V_{DD}$	-5		5	$\mu A$
		$XTAL\_SEL = V_{IH}, V_{IN} = V_{DD}$		20		

## Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	10pF Load	<b>Fundamental, Parallel Resonant</b>			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitor, $C_0$			1	5	pF
Correlation Drive Level			10	100	$\mu W$

**AC Electrical Characteristics**<sup>(4, 5)</sup>
 $V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ 
 $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO1/2} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ 
 $T_A = -40^\circ C$  to  $+85^\circ C$ .  $R_L = 50\Omega$  to  $V_{SS}$ 

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F <sub>OUT1</sub>	Output Frequency	FSEL=1		100		MHz
F <sub>OUT2</sub>	Output Frequency	FSEL=0		200		MHz
F <sub>REF</sub>	Reference Input Frequency			25		MHz
T <sub>R</sub> /T <sub>F</sub>	LVPECL Output Rise/Fall Time	20% – 80%	150	300	450	ps
ODC	Output Duty Cycle		48	50	52	%
T <sub>SKEW</sub>	Output-to-Output Skew	Note 6			45	ps
T <sub>LOCK</sub>	PLL Lock Time				20	ms
T <sub>jit</sub> (∅)	RMS Phase Jitter <sup>(7)</sup>	100MHz Integration Range (1.875MHz – 20MHz) Integration Range (12kHz – 20MHz)  200MHz Integration Range (1.875MHz – 20MHz) Integration Range (12kHz – 20MHz)		105 250  100 250		fs
	Spurious Noise Components	25MHz using 100MHz 25MHz using 200MHz		-85 -90		dBc

**Notes:**

- All phase noise measurements were taken with an Agilent 5052B phase noise system.
- Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.
- Measured using 25MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.

## Application Information

### Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF\_IN.

### Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal.

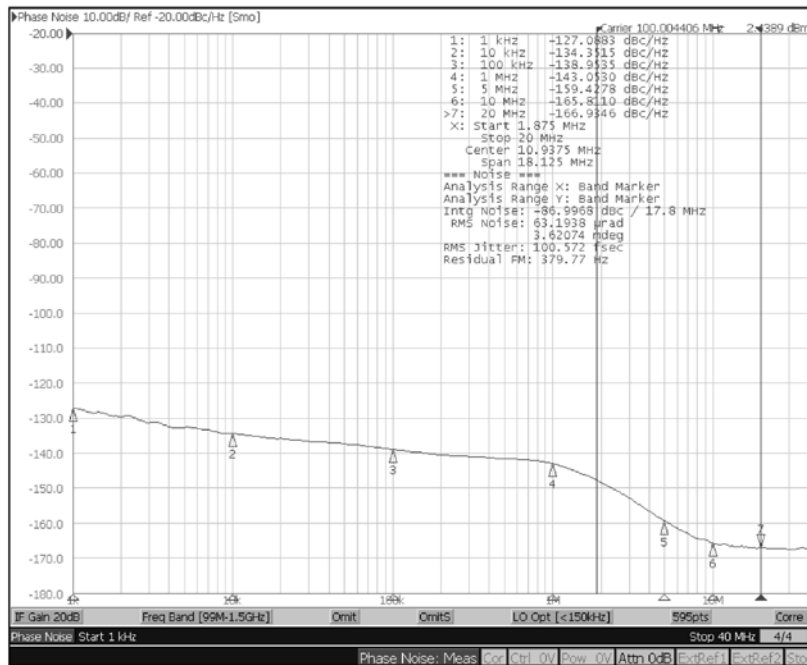
Crystal load capacitance is built inside the die so no external capacitance is needed. See the *Selecting a Quartz crystal for the Clockworks Flex I Family of Precision Synthesizers* application note for further details.

Contact Micrel's HBW applications group if you need assistance on selecting a suitable crystal for your application at: [hbwhelp@micrel.com](mailto:hbwhelp@micrel.com).

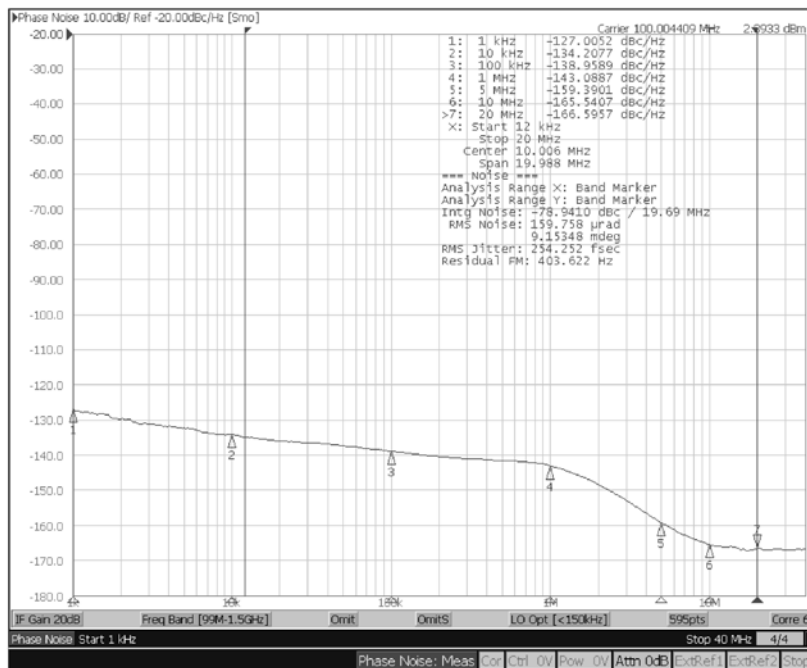
### HCSL Outputs

HCSL outputs are to be terminated with  $50\Omega$  to  $V_{SS}$ . For best performance load all outputs. If you want to AC-couple or change the termination, contact Micrel's application group at: [hbwhelp@micrel.com](mailto:hbwhelp@micrel.com).

## Phase Noise Plots



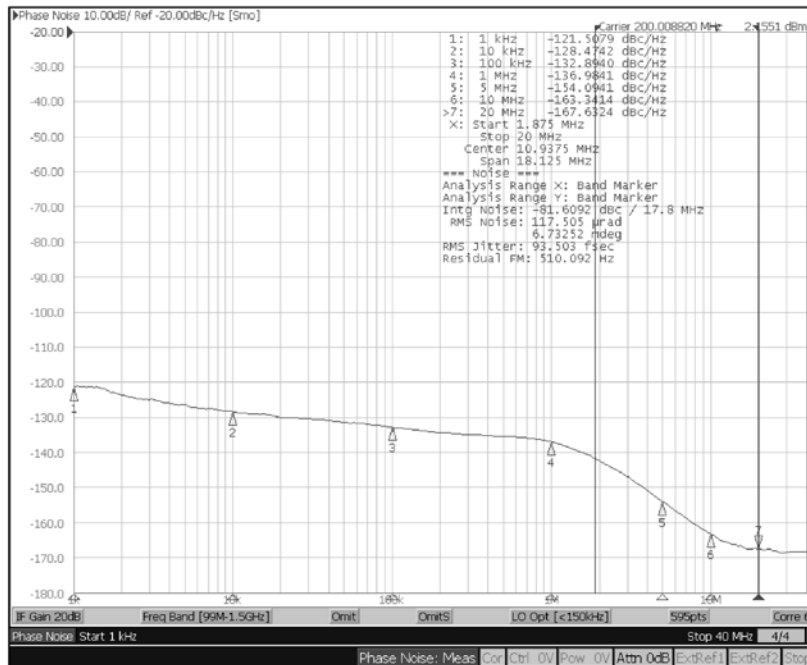
Phase Noise Plot: 100MHz, 1.875MHz – 20MHz 101fs



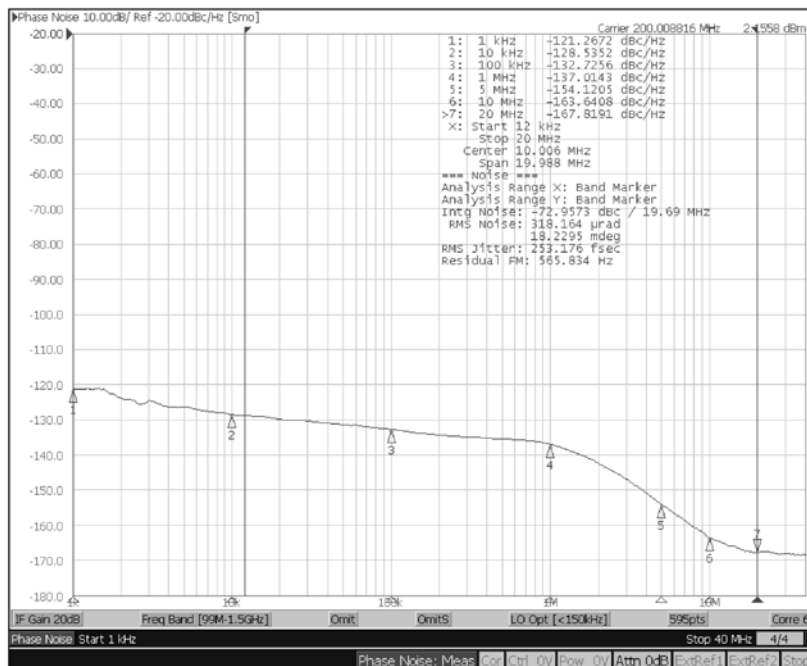
Phase Noise Plot: 100MHz, 12kHz – 20MHz 254fs



## Phase Noise Plots (Continued)



Phase Noise Plot: 200MHz, 1.875MHz – 20MHz 94fS



Phase Noise Plot: 200MHz, 12kHz – 20MHz 253fS

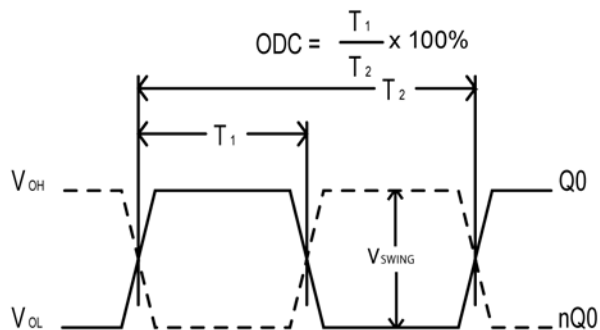


Figure 1. Duty Cycle Timing

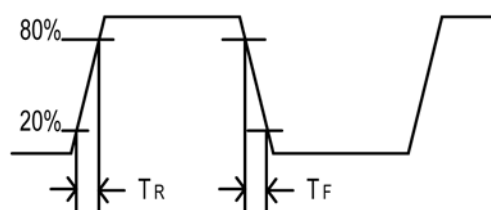


Figure 2. All Outputs Rise/Fall Time

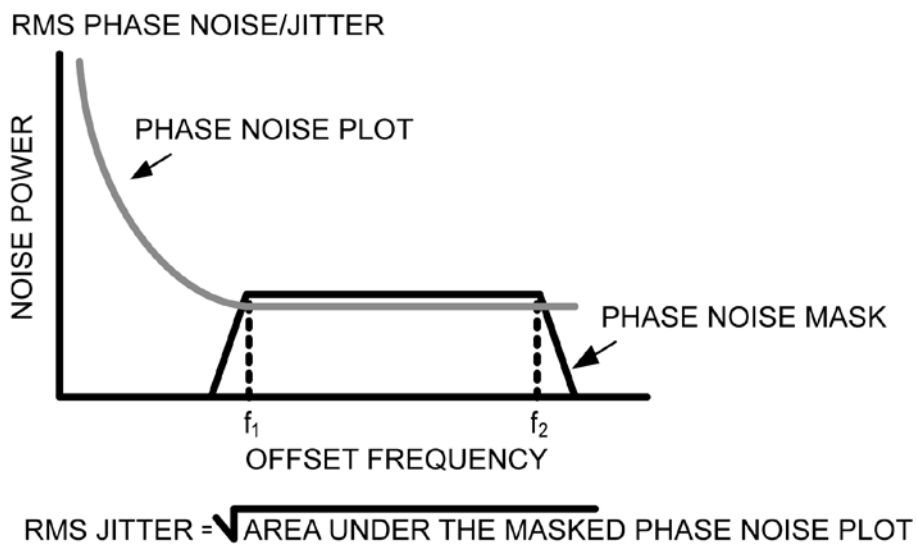


Figure 3. RMS Phase/Noise Jitter

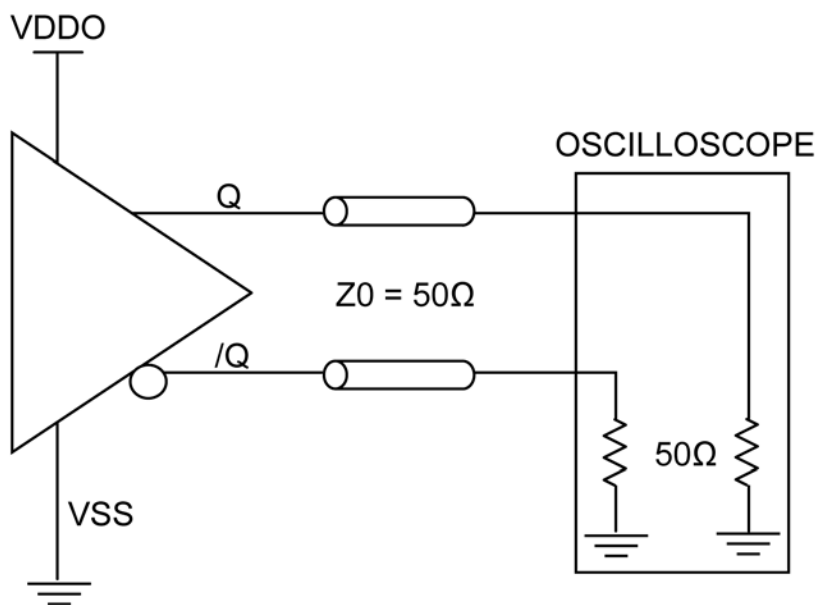


Figure 4. HCSL Output Load and Test Circuit

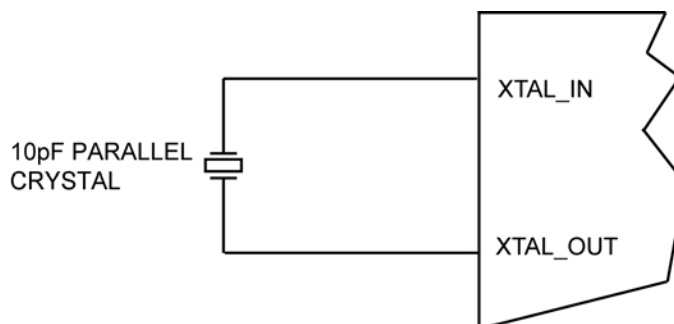
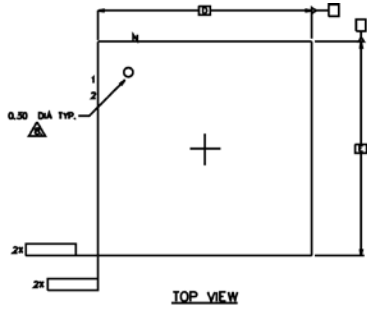


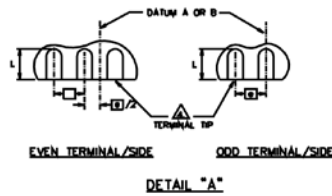
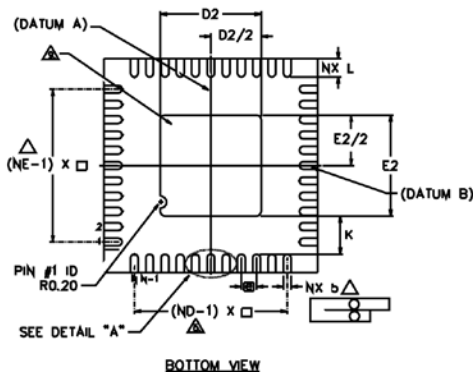
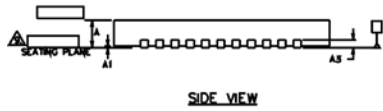
Figure 5. Crystal Input Interface

# Package Information<sup>(1)</sup>



**NOTES :**

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. - 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, ° IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
- △ DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
- △ ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
- △ PIN #1 ID ON TOP WILL BE LASER MARKED.
- △ BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMS TO JEDEC REGISTERED OUTLINE MO-220



SYMBOL	DIMENSIONS			No. of
	MIN.	NOM.	MAX.	
Ⓟ	0.50 BSC			
N	44			3
ND	11			△
NE	11			
L	0.55	0.60	0.65	
b	0.18	0.25	0.30	△
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
D	7.00 BSC			
E	7.00 BSC			
A	0.80	0.85	1.00	
A1	0.00	0.02	0.05	
K	0.20 MIN.			
⊖	0	—	12	2

## 44-Pin QFN

**Note:**

1. Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).

---

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

Micrel makes no representations or warranties with respect to the accuracy or completeness of the information furnished in this data sheet. This information is not intended as a warranty and Micrel does not assume responsibility for its use. Micrel reserves the right to change circuitry, specifications and descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Micrel's terms and conditions of sale for such products, Micrel assumes no liability whatsoever, and Micrel disclaims any express or implied warranty relating to the sale and/or use of Micrel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2011 Micrel, Incorporated.