MLX71122

300 to 930MHz
FSK/FM/ASK Receiver

Features

- Programmable PLL synthesizer
- 8-channel preconfigured or fully programmable SPI mode
- Double super-heterodyne receiver architecture with 2nd mixer as image rejection mixer
- Reception of FSK, FM and ASK modulated signals
- Low shut-down and operating currents
- AGC – automatic gain control
- On-chip IF filter
- Fully integrated FSK/FM demodulator
- RSSI for level indication and ASK detection
- 2nd order low-pass data filter
- Positive and negative peak detectors
- Data slicer (with averaging or peak-detector adaptive threshold)
- 32-pin Quad Flat No-Lead Package (QFN)
- EVB programming software is available on Melexis web site

Ordering Information

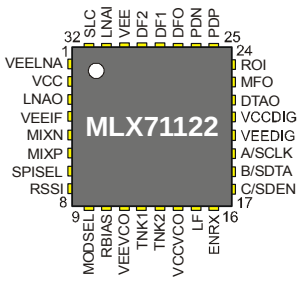
Part Number	*Temperature Code*	*Package Code*	*Delivery Form*
MLX71122	R (-40 °C to 105 °C)	LQ (32 L QFN 5x5 Quad)	73 pc/tube 5000 pc/T&R

Application Examples

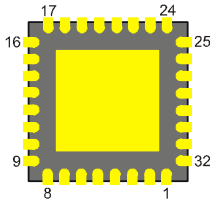
- General digital and analog RF receivers at 300 to 930MHz
- Tire pressure monitoring systems (TPMS)
- Remote keyless entry (RKE)
- Low power telemetry systems
- Alarm and security systems
- Active RFID tags
- Remote controls
- Garage door openers
- Home and building automation

Pin Description

top



bottom



General Description

The MLX71122 is a multi-channel RF receiver IC based on a double-conversion super-heterodyne architecture. It is designed to receive FSK and ASK modulated RF signals either in 8 predefined frequency channels or frequency programmable via a 3-wire serial programming interface (SPI).
The IC is designed for a variety of applications, for example in the European bands at 433MHz and 868MHz or for the use in North America or Asia, e.g. at 315MHz, 447MHz or 915MHz.

Document Content

1 Theory of Operation

1.1 General

The MLX71122 receiver architecture is based on a double-conversion super-heterodyne approach. The two LO signals are derived from an on-chip integer-N PLL frequency synthesizer. The PLL reference frequency is derived from a crystal (XTAL). The PLL synthesizer consists of an integrated voltage-controlled oscillator with external inductor, a programmable feedback divider chain, a programmable reference divider, a phase-frequency detector with a charge pump and an external loop filter.

In the receiver's down-conversion chain, two mixers MIX1 and MIX2 are driven by the internal local oscillator signals LO1 and LO2, respectively. The second mixer MIX2 is an image-reject mixer. As the first intermediate frequency (IF1) is very high (typically above 100 MHz), a reasonably high degree of image rejection is provided even without using an RF front-end filter. At applications asking for very high image rejections, cost-efficient RF front-end filtering can be realized by using a SAW filter in front of the LNA.

The receiver signal chain is set up by a low noise amplifier (LNA), two down-conversion mixers (MIX1 and MIX2), an on-chip IF filter (IFF) as well as an IF amplifier (IFA). By choosing the required modulation via an FSK/ASK switch (at pin MODSEL), either the on-chip FSK demodulator (FSK DEMOD) or the RSSI-based ASK detector is selected. A second order data filter (OA1) and a data slicer (OA2) follow the demodulator. The data slicer threshold can be generated from the mean-value of the data stream or by means of the positive and negative peak detectors (PKDET+/-).

In general the MLX71122 can be set to shut-down mode, where all receiver functions are completely turned off, and to several other operating modes. There are two global operating modes that are selectable via the logic level at pin SPISEL:

- 8-channel preconfigured mode (**ABC mode**)
- fully programmable mode (**SPI mode**).

In ABC mode the number of frequency channels is limited to eight but no microcontroller programming is required. In this case the three lines of the serial programming interface (SPI) are used to select one of the eight predefined frequency channels via simple 3-bit parallel programming. Pins ENRX and MODSEL are used to enable/disable the receiver and to select FSK or ASK demodulation, respectively.

SPI mode is recommended for full programming flexibility. In this case the three lines of the SPI are configured as a standard 3-wire bus (SDEN, SDTA and SCLK). This allows changing many parameters of the
receiver, for example more operating modes, channels, frequency resolutions, gains, demodulation types, data slicer settings and more. The pin MODSEL has no effect in this mode.

1.2 Technical Data Overview

- ❒ Input frequency ranges: 300 to 930MHz
- ❒ Power supply range: 3.0 to 5.5V
- ❒ Temperature range: -40 to +105°C
- ❒ Shutdown current: 50nA
- ❒ Operating current: 12mA (typ.)
- ❒ FSK input sensitivity: -107dBm (typ.)
- ❒ ASK input sensitivity: -112dBm (typ.)
- ❒ Internal IF2: 2MHz with 230kHz 3dB bandwidth
- ❒ Maximum data rate: 100kbps NRZ code, 50kbps bi-phase code
- ❒ Minimum frequency resolution: 10kHz
- ❒ Total image rejection: > 65dB (with external RF front-end filter)
- ❒ FSK/FM deviation range: ±2 to ±50kHz
- ❒ Spurious emission: < -70dBm
- ❒ Linear RSSI range: > 50dB
- ❒ FSK input frequency acceptance range: 180kHz (3dB sensitivity loss)
- ❒ Crystal reference frequency: 10MHz

1.3 Block Diagram

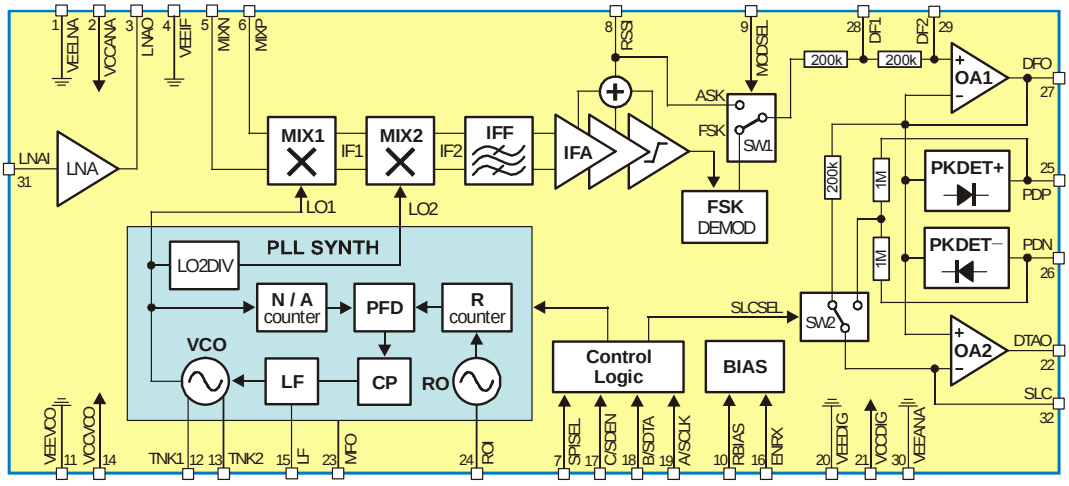


Fig. 1: MLX71122 block diagram

The MLX71122 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) to generate the first and second local oscillator signals LO1 and LO2, parts of the PLL SYNTH are the voltage-controlled oscillator (VCO), the feedback dividers N/A and R, the phase-frequency detector (PFD), the charge pump (CP) and the crystal-based reference oscillator (RO)
- Low-noise amplifier (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the first IF (intermediate frequency)
- Second mixer (MIX2) with image rejection for down-conversion from the first to the second IF
- IF Filter (IFF) with a 2MHz center frequency and a 230kHz 3dB bandwidth
- IF amplifier (IFA) to provide a large amount of voltage gain and an RSSI signal output
- FSK demodulator (FSK DEMOD)
- Operational amplifiers OA1 and OA2 for low-pass filtering and data slicing, respectively
- Positive (PKDET+) and negative (PKDET-) peak detectors
- Switches SW1 to select between FSK and ASK as well as SW2 to chose between averaging or peak detector data slicer
- Control logic with 3-wire bus serial programming interface (SPI)
- Biasing circuit with modes control

1.4 Enable/Disable in ABC Mode

ENRX	Description
0	Shutdown mode
1	Receive mode

Pin ENRX is pulled down internally. Device is in shutdown by default, after power supply on.
If ENRX = 0 and SPISEL = 1 then operating modes according to OPMODE bit (refer to control word R0).
If ENRX = 1 then OPMODE bit has no effect (hardwired receive mode).

1.5 Demodulation Selection in ABC Mode

MODSEL	Description
0	FSK demodulation
1	ASK demodulation

Pin MODSEL has no effect in SPI mode (SPISEL = 1). We recommend connecting it to ground to avoid a floating CMOS gate.

1.6 Programming Modes

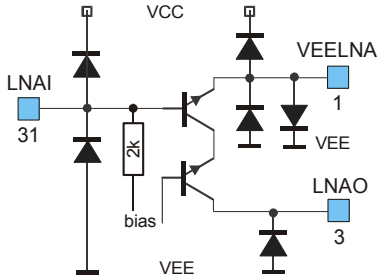
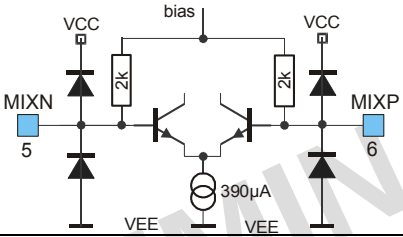
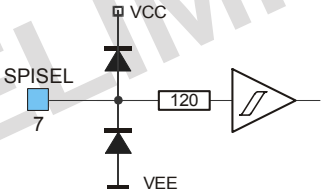
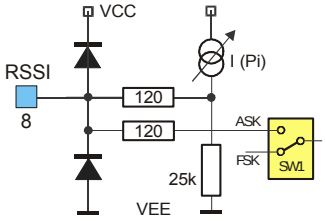
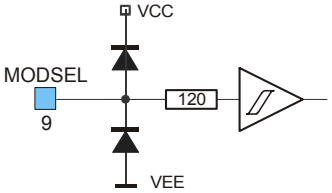
SPISEL	Description
0	ABC mode (8 channels preconfigured)
1	SPI mode (programming via 3-wire bus)

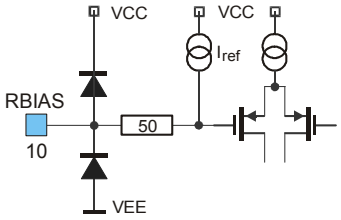
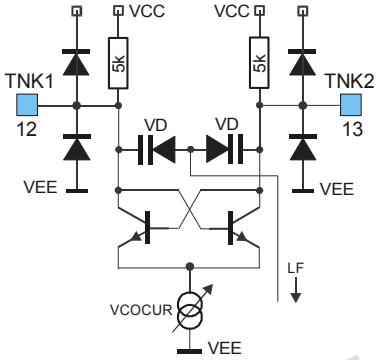
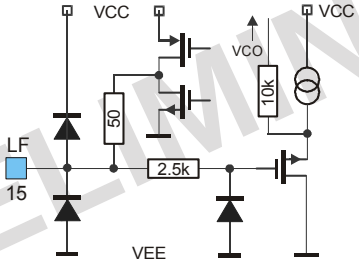
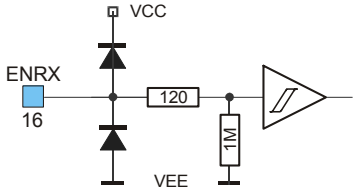
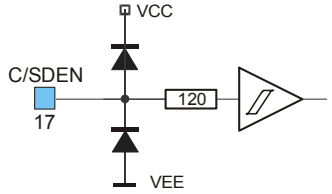
1.7 Preconfigured Frequencies in ABC Mode

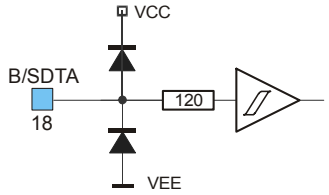
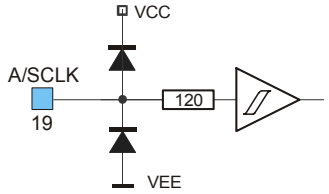
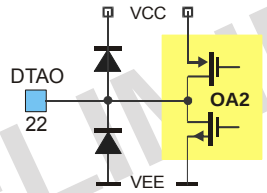
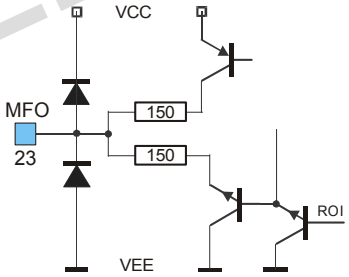
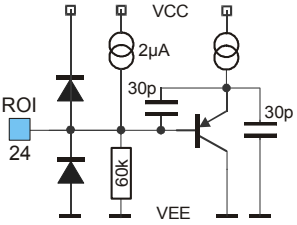
A	B	C	Receive Frequency
0	0	0	FSK1: 369.5 MHz
0	1	0	FSK5: 388.3 MHz
1	0	0	FSK2: 371.1 MHz
1	1	0	FSK4: 376.9 MHz
0	0	1	FSK3: 375.3 MHz
0	1	1	FSK7: 394.3 MHz
1	0	1	FSK6: 391.5 MHz
1	1	1	FSK8: 395.9 MHz

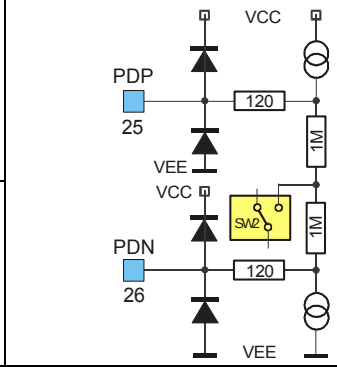
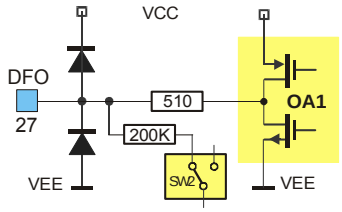
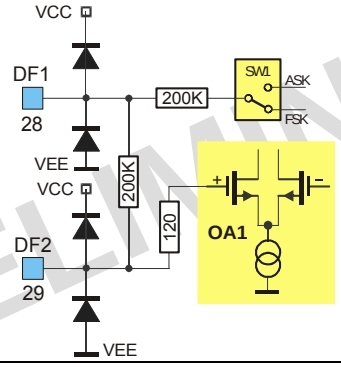
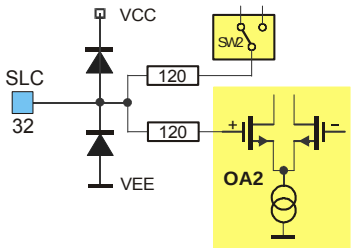
As all pins, pins A, B, and C are equipped with ESD protection diodes that are tied to VCC and to VEE. Therefore these pins should not be directly connected to positive supply (a logic “1”) before the supply voltage is applied to the IC. Otherwise the IC will be supplied through these control lines and it may enter into an unpredictable mode. In case the user wants to apply a positive supply voltage to these pins before the supply voltage is applied to the IC, a protection resistor should be inserted in each control line.

2 Pin Definitions and Descriptions

Pin No.	Name	I/O Type	Functional Schematic	Description
1	VEELNA	ground		ground of LNA core
31	LNAI	analog input		LNA input, approx. 27Ω single-ended
3	LNAO	analog output		LNA open-collector output, to be connected to external LC tank that resonates at RF
2	VCCANA	supply		positive supply of LNA, MIX1 MIX2, IFF, IFA, FSK DEMOD, OA1, OA2, PKDET+, PKDET- and BIAS
4	VEEIF	ground		negative supply of LNA, MIX1 MIX2, IFF, IFA, and FSK DEMOD
5	MIXN	analog input		mixer 1 negative input
6	MIXP	analog input		mixer 1 positive input
7	SPISEL	CMOS input		SPI select input
8	RSSI	analog output		RSSI output, approx. 25kΩ
9	MODSEL	CMOS input		demodulation select input (FSK or ASK demodulation)

Pin No.	Name	I/O Type	Functional Schematic	Description
10	RBIAS	analog I/O		external resistor for voltage and current biasing, 30kΩ by default, to provide stable parameters over temperature and supply variations
11	VEEVCO	ground		ground of VCO
12	TNK1	analog I/O		VCO collector output, connection 1 to external LC tank
13	TNK2	analog I/O		VCO collector output, connection 2 to external LC tank
15	LF	analog I/O		charge pump output, connection to external loop filter
14	VCCVCO	supply		positive supply of VCO
16	ENRX	CMOS input		enable/disable control input (with internal pull-down)
17	C/SDEN	CMOS input		frequency control line C or SPI control line SDEN

Pin No.	Name	I/O Type	Functional Schematic	Description
18	B/SDTA	CMOS input		frequency control line B or SPI control line SDTA
19	A/SCLK	CMOS input		frequency control line A or SPI control line SCLK
20	VEEDIG	ground		ground of PLL SYNT (except of VCO), Control Logic, and OA2 out stage
21	VCCDIG	supply		positive supply of PLL SYNT (except of VCO), Control Logic, RO and OA2 out stage
22	DTAO	CMOS output		data output, 2mA sink or source capability
23	MFO			multifunctional output, reference oscillator output by default
24	ROI	analog input		reference oscillator input for connecting an external crystal, Colpitts type oscillator with internal feedback capacitors

Pin No.	Name	I/O Type	Functional Schematic	Description
25	PDP	analog I/O		peak detector positive output for connecting an external capacitor
26	PDN	analog I/O		peak detector positive output for connecting an external capacitor
27	DFO	analog output		data filter output
28	DF1	analog I/O		data filter connection 1 for connecting an external capacitor
29	DF2	analog I/O		data filter connection 2 for connecting an external capacitor
30	VEEANA	ground		ground of RO, OA1, OA2, PKD+, PKD- and BIAS
32	SLC	analog I/O		slicer reference input for connecting an external capacitor

3 Functional Description

3.1 Frequency Planning

Because of the double conversion architecture that employs two mixers and two IF signals, there are four different combinations for injecting the LO1 and LO2 signals:

- LO1 high side and LO2 high side: receiving at f_{RF}(high-high)
- LO1 high side and LO2 low side: receiving at f_{RF}(high-low)
- LO1 low side and LO2 high side: receiving at f_{RF}(low-high)
- LO1 low side and LO2 low side: receiving at f_{RF}(low-low)

As a result, four different radio frequencies (RFs) could yield one and the same second IF (IF2). Fig. 2 shows this for the case of receiving at f_{RF}(high-high). In the example of Fig. 2, the image signals at f_{RF}(low-high) and f_{RF}(low-low) are suppressed by the bandpass characteristic provided by the RF front-end. The bandpass shape can be achieved either with a SAW filter (featuring just a couple of MHz bandwidth), or by the tank circuits at the LNA input and output (this typically yields 30 to 60MHz bandwidth). In any case, the high value of the first IF (IF1) helps to suppress the image signals at f_{RF}(low-high) and f_{RF}(low-low).

The two remaining signals at IF1 resulting from f_{RF}(high-high) and f_{RF}(high-low) are entering the second mixer MIX2. This mixer features image rejection with so-called single-sideband (SSB) selection. This means either the upper or lower sideband of IF1 can be selected. In the example of Fig. 2, LO2 high-side injection has been chosen to select the IF2 signal resulting from f_{RF}(high-high).

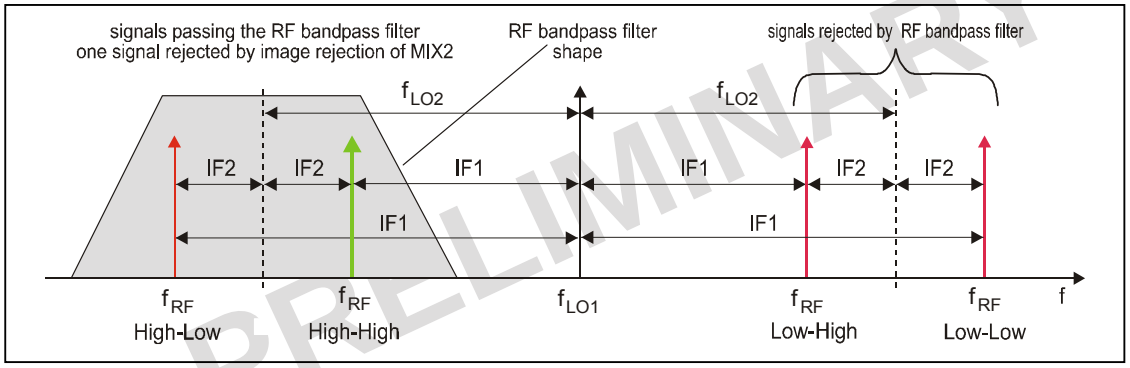


Fig. 2: The four receiving frequencies in a double conversion superhet receiver

It can be seen from the block diagram of Fig. 1 that there is a fixed relationship between the LO1 signal frequency f_{LO1} and the LO2 signal frequency f_{LO2}.

$$LO2DIV = N_{LO2} = \frac{f_{LO1}}{f_{LO2}} \quad (1)$$

The LO1 signal frequency f_{LO1} is directly synthesized from the crystal reference oscillator frequency f_{RO} by means of an integer-N PLL synthesizer. The PLL consists of a dual-modulus prescaler (P/P+1), a program counter N and a swallow counter A.

$$f_{LO1} = \frac{f_{RO}}{R}(N \cdot P + A) = f_{PFD}(N \cdot P + A) = f_{PFD} \cdot N_{tot} \quad (2)$$

Due to the double superhet receiver architecture, the channel frequency step size f_{CH} is not equal to the phase-frequency detector (PFD) frequency f_{PFD}. For high-side injection, the channel step size f_{CH} is given by:

$$f_{CH} = \frac{f_{RO}}{R}\frac{N_{LO2}-1}{N_{LO2}} = f_{PFD}\frac{N_{LO2}-1}{N_{LO2}} \quad (3)$$

While the following equation is valid for low-side injection:

$$f_{CH} = \frac{f_{RO}}{R}\frac{N_{LO2}+1}{N_{LO2}} = f_{PFD}\frac{N_{LO2}+1}{N_{LO2}} \quad (4)$$

3.2 Calculation of Counter Settings

Frequency planning and the selection of the MLX71122's PLL counter settings are straightforward and can be laid out on the following procedure.

Usually the receive frequency f_{RF} and the channel step size f_{CH} are given by system requirements. The N and A counter settings can be derived from N_{tot} or f_{LO1} and f_{PFD} by using the following equations.

$$N = \text{floor}\left(\frac{N_{tot}}{P}\right) = \text{floor}\left(\frac{N_{tot}}{32}\right);\ A = N_{tot} - N \cdot P = N_{tot} - N \cdot 32 \quad (5)$$

3.2.1 Calculation of LO1 and IF1 frequency for Low Frequency Bands

High-high injection must be used for the low frequency bands. First of all choose a PFD frequency f_{PFD} according to below table. The R counter values are valid for a 10MHz crystal reference frequency f_{RO}. The PFD frequency is given by $f_{PFD} = f_{RO}/R$.

Injection Type	f_{CH} [kHz]	f_{PFD} [kHz]	R
h-h	10	13.3	750
h-h	12.5	16.7	600
h-h	20	26.7	375
h-h	25	33.3	300
h-h	50	66.7	150
h-h	100	133.3	75
h-h	250	333.3	30

The second step is to calculate the missing parameters f_{LO1}, f_{IF1}, N_{tot}, N and A. While the second IF (f_{IF2}), the N_{LO2} divider ratio and the prescaler divider ratio P are bound to f_{IF2} = 2MHz, N_{LO2} = 4 (or 8) and P =32.

$$f_{LO1} = \frac{N_{LO2}}{N_{LO2}-1}(f_{RF} - f_{IF2}) \qquad f_{LO1} = \frac{4}{3}(f_{RF} - 2\text{MHz}) \quad (6)$$

$$f_{IF1} = \frac{f_{RF} - N_{LO2}f_{IF2}}{N_{LO2}-1} \qquad f_{IF1} = \frac{f_{RF} - 8\text{MHz}}{3} \quad (7)$$

Finally N and A can be calculated with formula (5).

3.2.2 Calculation of LO1 and IF1 frequency for High Frequency Bands

Typical ISM band operating frequencies like 868.3 and 915MHz can be covered without changing the crystal nor the VCO inductor.
Low-low injection should be used for the high frequency bands. First of all choose a PFD frequency f_{PFD} according to below table. The R counter values are valid for a 10MHz crystal reference. The PFD frequency is given by $f_{PFD} = f_{RO} /R$.

Injection Type	f_{CH} [kHz]	f_{PFD} [kHz]	R
l-l	20	16	625
l-l	25	20	500
l-l	50	40	250
l-l	100	80	125
l-l	250	200	50
l-l	500	400	25

The second step is to calculate the missing parameters f_{LO1}, f_{IF1}, N_{tot}, N and A. While the second IF (f_{IF2}), the N_{LO2} divider ratio and the prescaler divider ratio P are bound to f_{IF2} = 2MHz, N_{Lo2} = 4 (or 8) and P =32.

$$f_{LO1} = \frac{N_{LO2}}{N_{LO2}+1}(f_{RF} - f_{IF2}) \qquad f_{LO1} = \frac{4}{5}(f_{RF} - 2MHz) \tag{8}$$

$$f_{IF1} = \frac{f_{RF} + N_{LO2} f_{IF2}}{N_{LO2}+1} \qquad f_{IF1} = \frac{f_{RF} + 8MHz}{5} \tag{9}$$

Finally N and A can be calculated with formula (5).

3.2.3 Counter Setting Examples for SPI Mode

To provide some examples, the following table shows some counter settings for the reception of the well-known ISM and SRD frequency bands. The channel spacing is assumed to be f_{CH} = 100kHz. In below table all frequency units are in MHz.

Inj	f_{RF}	f_{IF1}	f_{LO1}	N_{tot}	N	P	A	f_{PFD}	R	f_{REF}	f_{LO2}	f_{IF2}
h-h	300	97.3	397.3	2980	93	32	4	0.133	75	10	99.3	2
h-h	315	102.3	417.3	3130	97	32	26	0.133	75	10	104.3	2
h-h	434	142	576	4320	135	32	0	0.133	75	10	144	2
h-h	470	154	624	4680	146	32	8	0.133	75	10	156	2
l-l	850	171.6	678.4	8480	256	32	0	0.08	125	10	169.6	2
l-l	868	175.2	692.8	8660	270	32	20	0.08	125	10	173.2	2
l-l	915	184.6	730.4	9130	285	32	10	0.08	125	10	182.6	2
l-l	930	187.6	742.4	9280	290	32	0	0.08	125	10	185.6	2

3.2.4 Counter Settings in ABC Mode – 8+1 Preconfigured Channels

In ABC mode (SPISEL=0), the counter settings are hard-wired. In below table all frequency units are in MHz.

CH	Inj	f_{RF}	f_{IF1}	f_{LO1}	N_{tot}	N	P	A	f_{PFD}	R	f_{REF}	f_{LO2}	f_{IF2}
1	h-l	369.5	125.8	495.3	3715	116	32	3	0.133	75	10	123.8	2
2	h-l	371.1	126.4	497.5	3731	116	32	19	0.133	75	10	124.4	2
3	h-l	375.3	127.8	503.1	3773	117	32	29	0.133	75	10	125.8	2
4	h-l	376.9	128.3	505.2	3789	118	32	13	0.133	75	10	126.3	2
5	h-l	384.0	130.7	514.7	3860	120	32	20	0.133	75	10	128.7	2
6	h-l	388.3	132.1	520.4	3903	121	32	31	0.133	75	10	130.1	2
7	h-l	391.5	133.2	524.7	3935	122	32	31	0.133	75	10	131.2	2
8	h-l	394.3	134.1	528.4	3963	123	32	27	0.133	75	10	132.1	2
9	h-l	395.9	134.6	530.5	3979	124	32	11	0.133	75	10	132.6	2

3.3 PLL Frequency Synthesizer

The MLX71122 contains an integer-N PLL frequency synthesizer. The reference frequency f_R is derived from a stable crystal reference oscillator.

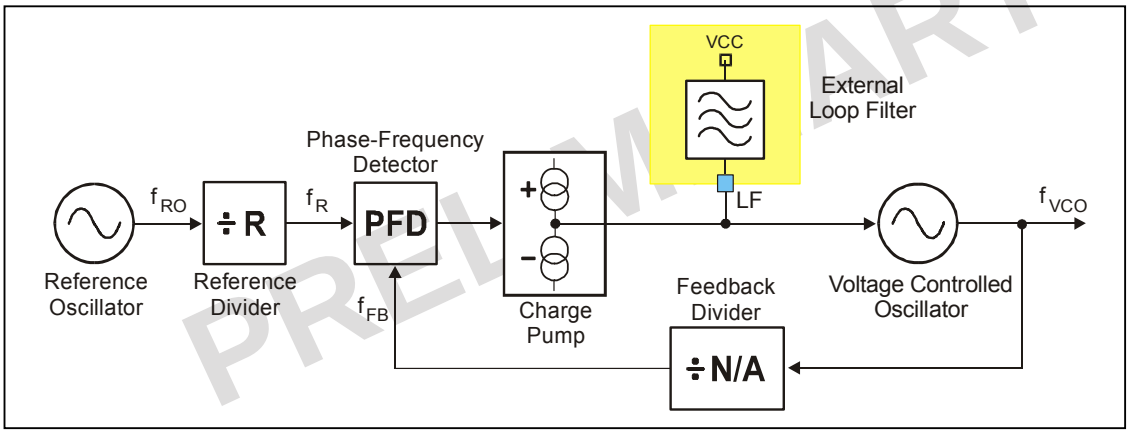


Fig. 3: Integer-N PLL Frequency Synthesizer Topology

The locked state of the PLL is defined by the following relations:

$$\frac{f_{RO}}{R} = f_R = f_{PFD} = f_{FB} = \frac{f_{VCO}}{N_{tot}} = \frac{f_{VCO}}{N \cdot P + A}. \qquad (10)$$

In this formula the total PLL feedback divider ratio is called N_{tot}. The synthesized output frequency f_{VCO} can be changed by reprogramming the reference divider or the feedback divider according to

$$f_{VCO} = N_{tot} \frac{f_{RO}}{R} = (N \cdot P + A) \frac{f_{RO}}{R}. \qquad (11)$$

The R counter is used to set the channel spacing. Different channels can be selected by changing the total feedback divider ratio.

List of Mathematical Acronyms	
A	divider ratio of the swallow counter (part of feedback divider)
f_{FB}	frequency at the feedback divider output
$\text{floor}(x)$	The floor function gives the largest integer less than or equal to x. For example, floor(5.4) gives 5, floor(-6.3) gives -7.
f_{PFD}	PFD frequency in locked state
$\frac{f_{RO}}{R} = f_R$	reference frequency of the PLL
f_{RO}	frequency of the crystal reference oscillator
f_{VCO}	frequency of the VCO (equals the LO1 signal of the first mixer)
$N_{tot} = N \cdot P + A$	total divider ratio of the PLL feedback path
N	divider ratio of the program counter (part of feedback divider)
N_{LO2}	LO2DIV divider ratio, to derive the LO2 signal from LO1 (N_1 = 4 or 8)
P	divider ratio of the prescaler (part of feedback divider)
R	divider ratio of the reference divider R

3.3.1 Pulse Swallow Counter

The programmable feedback divider of the PLL is based on a pulse-swallow topology. Fig. 4 depicts its implementation, consisting of a dual-modulus prescaler, an RS latch and two programmable counters.

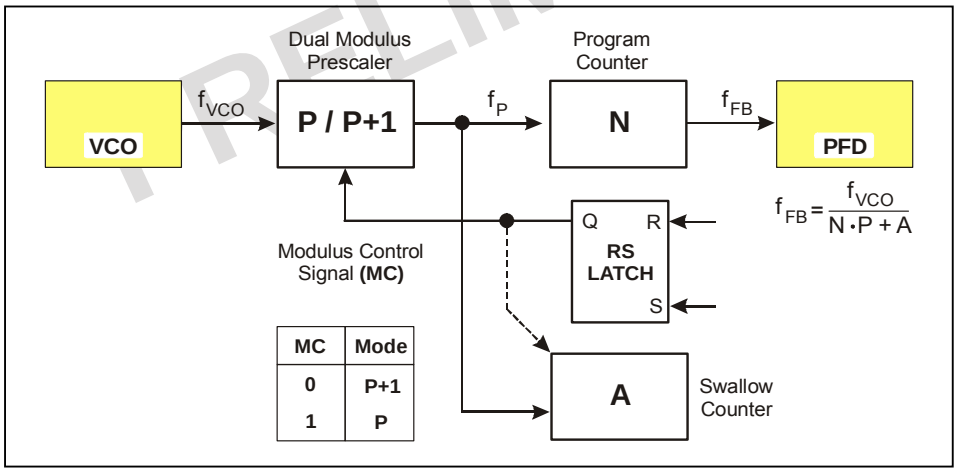


Fig. 4 Pulse Swallow Counter Topology

During one cycle of f_{FB} the prescaler begins the operation by dividing by P+1 until the swallow counter A is full. The RS latch is then set and changes the prescaler modulus to P (via the modulus control signal MC) and disables the swallow counter. The division process continues until the program counter N is full and the RS latch is reset.

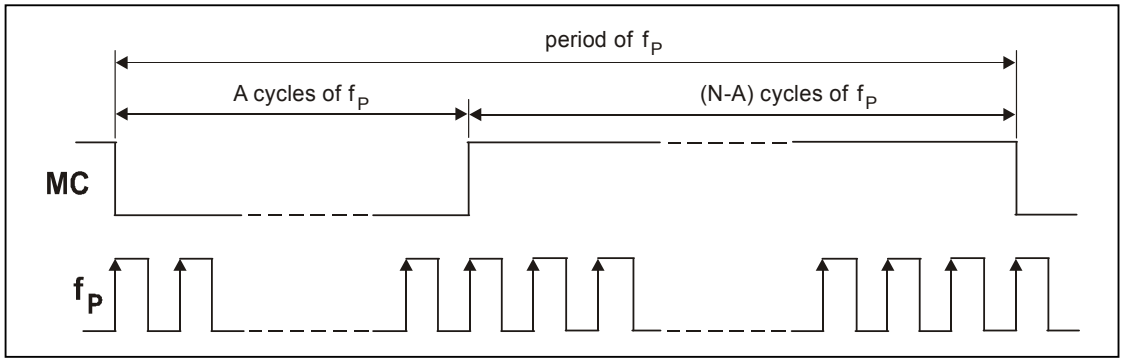


Fig. 5 Pulse Swallow Divider Timing

Therefore the overall feedback divide ratio is:

$$(P+1)\cdot A + P\cdot(N-A) = N\cdot P + A\,. \qquad (12)$$

Further restrictions can be derived from above equation: A < P and A < N.
Simple math shows that for uniform frequency steps the following condition is necessary:

$$N\cdot P + A \geq P\cdot P\,. \qquad (13)$$

3.3.2 PLL Counter Ranges

In order to cover the frequency range of about 300 to 930MHz the following counter values are implemented in the receiver:

PLL Counter Ranges			
A	**N**	**R**	**P**
0 to 31 (5bit)	3 to 2047 (11bit)	3 to 2047 (11bit)	32

Therefore the minimum and maximum divider ratios of the PLL feedback divider are given by:

$$N_{totmin} = 32\cdot 32 = 1024 \qquad N_{totmax} = 2047\cdot 32 + 31 = 65535$$

3.3.3 Reference Oscillator (RO)

The reference oscillator is based on a Colpitts topology with two integrated functional capacitors as shown in figure 7. The circuitry is optimized for a load capacitance range of 10pF to 15pF. The equivalent input capacitance CRO offered by the oscillator input pin ROI is about 15pF. To ensure a fast and reliable start-up and a very stable frequency over the specified supply voltage and temperature range, the oscillator bias circuitry provides an amplitude regulation. Via SPI it is possible to adjust the typical core current with register ROCUR. There are four values available (see 4.1.7). At the default setting 355µA, the amplitude at pin ROI is monitored in order to regulate the current of the oscillator core I_{RO}.

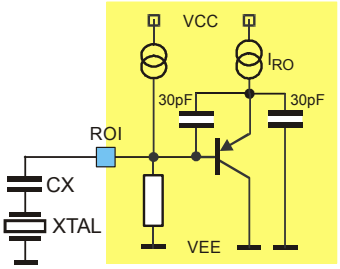


Fig.6: RO schematic

3.3.4 Phase-Frequency Detector (PFD)

The phase-frequency detector (in conjunction with the charge pump) generates a voltage step at the loop filter pin LF. This voltage step is proportional to the phase difference between the digital input signals f_R and f_{FB}. The implementation of the phase detector is phase-frequency type. This circuitry is very useful because it decreases the acquisition time significantly even if both frequencies differ very much. The phase-frequency detector creates Up and Down signals that control the charge pump and that are also used for the lock detection circuit. The first rising edge of one of the input signals, after a reset of Up and Down, sets either the Up or the Down signal from LOW to HIGH. The following rising edge of the other signal resets Up and Down. If the register setting PFDPOL (see 4.1.2) is HIGH, the PFD polarity is positive. This means a rising edge of the signal f_R sets Up from LOW to HIGH and a rising edge of the signal f_{FB} sets Down from LOW to HIGH. If PFDPOL is LOW, the PFD polarity is negative and the assignment of Up and Down to the signals f_R and f_{FB} is swapped.

In the MLX71122 receiver the VCO frequency increases if the loop filter output voltage increases and vice versa. The PFD polarity needs to be positive to achieve the correct feedback in the PLL loop. If an external varactor diode is added to the VCO tank, the tuning characteristic may change from positive to negative depending on the particular varactor diode circuitry. Therefore the PFDPOL bit can be used to define the phase-frequency detector polarity.

3.3.5 Charge Pump (CP)

The Charge Pump is controlled by the Up and Down signals of the Phase-Frequency Detector. If the Up signal is HIGH, then the charge pump current I_{CP} is sourced from the positive supply rail to the loop filter pin LF (pin 15). If the Down signal is HIGH, then the current I_{CP} is drained from pin LF to ground.
The gain of the phase detector in conjunction with the charge pump can be expressed as:

$$K_{PD} = \frac{I_{CP}}{2\pi}\ , \qquad (14)$$

whereat I_{CP} is the charge pump current which is set via register CPCUR (see 4.1.2). Default of I_{CP} is 100µA. The static Up and Down selections of I_{CP} can be used for test purposes.

3.3.6 Loop Filter (LF)

Since the loop filter has a strong impact on the function of the PLL, it must be chosen carefully. The suggested filter topology is shown in Fig. 7.

The loop filter of the PLL is set up by an external resistor and two external capacitors. It constitutes a 2nd order passive filter. This approach allows the user to easily adapt the loop filter bandwidth to different requirements. As a rule of thumb the loop filter bandwidth of an integer-N PLL should be set 10 times smaller than the PFD frequency. This is to achieve a stable PLL with a flat VCO noise floor.

The loop filter bandwidth depends on the external resistor and capacitors as well as on the VCO gain, the charge pump current and the so-called phase margin. A phase margin of 45° is commonly used for highest PLL stability. It is recommended to follow the component lists of section 6 for choosing appropriate values of the loop filter resistor and capacitors.

A good source for a detailed PLL analysis is: “Gardner, F.M., Phase-Locked Loop Techniques, John Wiley & Sons, 1980.”

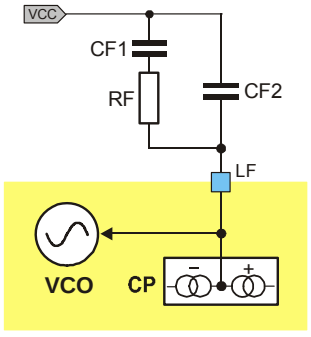


Fig. 7: 2nd order Loop filter

3.3.7 Lock Detector (LD)

In SPI mode a lock-detect signal LD is available at pin 23 if MFO is set to 1000 (binary) in control word R3 (see 4.1.4). The pin output is HIGH when the PLL is locked in. Alternatively the lock-detect signal is visible in bit 10 of R7 (see 4.1.8) if bit SHOWLD in R1 (see 4.1.2) is HIGH. The lock detection circuitry uses the Up and Down signals from the phase-frequency detector to check them for phase coherency. Figure 8 shows an overview of the lock signal generation. The locked state and the unlock condition will be controlled by the register settings of LDTIME and LDERR. During the start-up phase of the PLL, Up and Down signals are quite unbalanced. Therefore the Lock Detector circuit waits the time span that is programmed in divider DIV_LDTIME before a first lock can occur. The time span is dependent on the period of the reference signal f_R. By default it is $16/f_R$ (see 4.1.2). When the PLL approaches steady state, the signals Up and Down begin to overlap. The time span within which the signals are not overlapping is assessed by using a programmable delay gate. If it is shorter than programmed in LDERR (see 4.1.2) then the LD output is set to HIGH. By default the error time should be shorter than 15ns. A second option is shorter than 30ns.
After LD is set to HIGH the divider is disabled and the lock state remains unchanged until the unlock signal resets the divider.

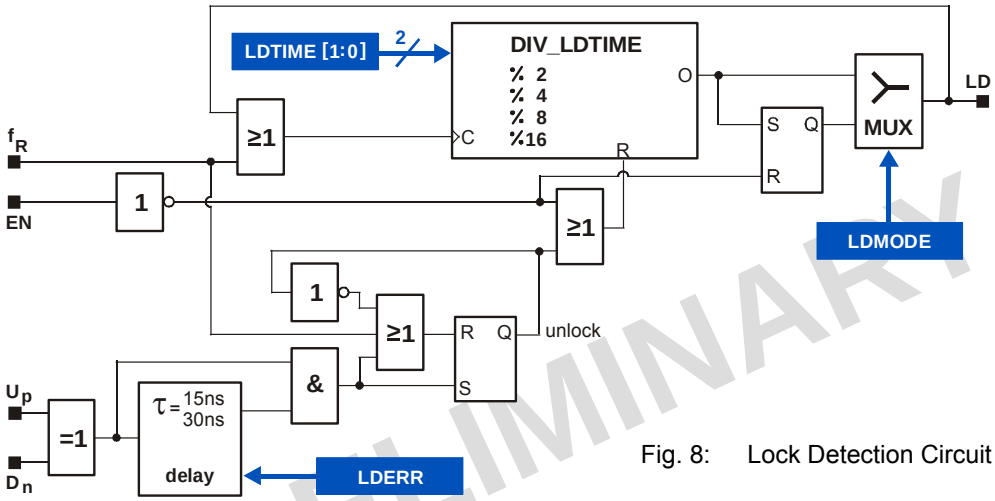


Fig. 8: Lock Detection Circuit

3.3.8 Voltage Controlled Oscillator (VCO)

The receiver includes an LC-based voltage controlled oscillator with an external inductor connected between pins TNK1 and TNK2. Two internal varactor diodes in series combination are forming the tuneable part of the oscillator tank. The oscillation frequency is adjusted by the DC voltage at pin LF. The tuning sensitivity of the VCO is approximately 83MHz/V for 433MHz operation and 105MHz/V at 868MHz, respectively. Since the cathodes of the varactors is tied to VCC, a higher voltage at pin LF or an Up-signal of the PFD forces the capacitance to decrease and the VCO frequency to increase. With positive phase detector polarity (PFDPOL = HIGH) the edges of the signal f_{FB} will catch up to the reference signal f_R (see Fig. 3).
The VCO current VCOCUR can be adjusted via the SPI in order to ensure stable oscillations over the whole frequency range. Also the bias current of the output buffer can be increased with VCOBUF to enhance its driving capability at the high frequency bands above 800MHz (see section 4.1.2). If the supply voltage is lower than 5V it is possible to adjust the tuning range of the VCO with VCORANGE (see 4.1.2). The minimum supply voltage is 3V.

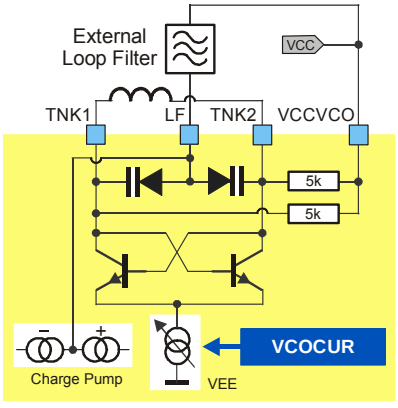


Fig.9: VCO schematic

3.4 Receiver Front End

The radio frequency (RF) front-end of the receiver is a double-superheterodyne configuration that converts the input RF signal via a first intermediate frequency (IF1) signal to a second intermediate frequency (IF2) signal. While the range of IF1 can vary between 100 and 200MHz, IF2 is fixed to 2MHz. Both signals are completely processed internally. According to the block diagram (see Fig. 1), the front-end consists of an LNA, a first mixer (MIX1), a second mixer (MIX2), an internal IF filter (IFF) and an IF limiting amplifier (IFA) with received signal strength indicator (RSSI). The local oscillator signal for mixer 1 (LO1) is directly generated in the PLL frequency synthesizer. The LO2 signal for mixer 2 is derived from the LO1 signal via a divider (see 4.1.4).

There is no inherent suppression of the first mixer's image frequency. It depends on the particular application and the system's environmental conditions whether an RF front-end filter should be added or not. If image rejection and/or good blocking immunity are relevant system parameters, a band-pass filter must be placed either in front or after the LNA. This filter can be a SAW (surface acoustic wave) or LC-based filter (e.g. helical type). Because mixer 2 is an image rejection mixer, the image frequencies of the second mixing process are suppressed (see Fig. 2). The advantage of a two stage mixing receiver is the higher gain that can be achieved in the front end.

3.4.1 Low Noise Amplifier (LNA) and Mixer 1 (MIX1)

The LNA is based on a cascode topology for low-noise, high gain and good reverse isolation. The open collector output has to be connected to an external resonance circuit tuned to the receive frequency. The gain of the LNA can be changed to achieve a high dynamic range. There are four gain settings selectable by the control bits LNAGAIN (see 4.1.1). Default setting is the highest gain. The gain settings are automatically set if the automatic gain control (AGC) feature is activated (see 4.1.4).

The first mixer is a double-balanced mixer which converts the receive frequency to IF1. The default LO injection type for RF frequencies below 600MHz should be high side ($f_{LO1} = f_{RX} + f_{IF1}$). Low side injection ($f_{LO1} = f_{RX} - f_{IF1}$) is recommended for the higher frequency bands. Since the data polarity of an FSK modulated signal will be inverted by changing the injection side it is possible to change the data polarity at the data output (DTAO) via bit DTAPOL (see 4.1.1). Two gain settings of mixer 1 can be selected through MIX1GAIN (see 4.1.1): 14dB as a default value or 0dB optionally.

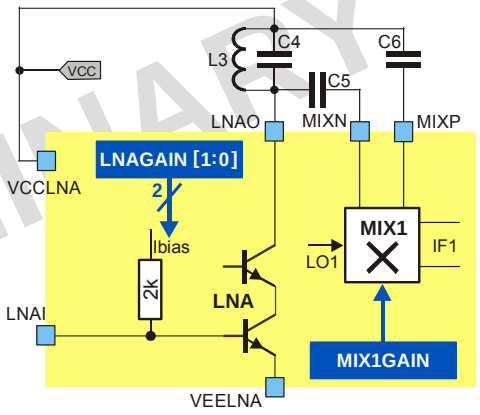


Fig. 10: LNA and Mixer 1

3.4.2 Mixer 2 (MIX2)

The second mixer is a double-balanced image rejection mixer in Hartley architecture using a complex poly-phase filter that converts the IF1 to the IF2 signal. The default LO injection type is low side ($f_{LO2} = f_{IF1} - f_{IF2}$), but also high side injection is possible ($f_{LO2} = f_{IF1} + f_{IF2}$), by setting SSBSEL to LOW (see 4.1.1). As for mixer 1, the injection side determines the polarity of the output signal. Two gain settings of mixer 2 can be selected by MIX2GAIN (see 4.1.1), a setting at 9dB (default) and one at -2dB.

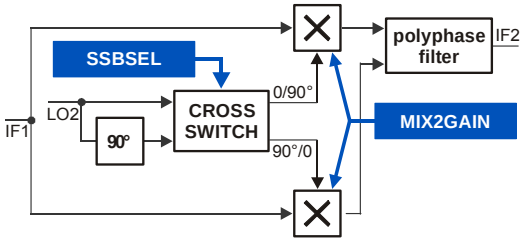


Fig. 11: Mixer 2 (Image Rejection Mixer)

3.4.3 IF Filter (IFF)

The MLX71122 comprises an internal IF filter with a -3dB bandwidth of 230kHz and a -40dB attenuation bandwidth of 1.6MHz. The filter contains three capacitively coupled bi-quad stages that represent resonant tanks at a filter center frequency of 2MHz. Each bi-quad stage uses transconductance cells that can be tuned by changing their bias current. An auto-tuning mechanism is implemented that permanently adjusts the bias current to eliminate process, temperature and supply voltage variations. A matched master bi-quad is used in a current controlled oscillator (CCO) at 3MHz embedded in a PLL structure. The PFD-frequency of this PLL is derived from the RO signal using divider RIFF (see 4.1.6). The actual internal control word IFFVAL of the filter can be read out from register 7 (see. 4.1.8). At power on and after deactivation of the IF filter with IFFTUNE (see 4.1.7), the preset value that is stored in IFFPRES in register 6 (see 4.1.7) will be loaded into the internal control word. If the filter auto tuning is halted via IFFHLT (see 4.1.7) then the actual word remains in the internal control word but is not updated. We recommend to turn off the IFF auto tuning after the PLL lock during FSK-reception in peak detector mode since the auto tuning generates unwanted positive voltage pulses of about 100mV on the DFO voltage. The internal control word determines the current consumption of the filter and therefore of the whole receiver. Higher values lead to higher current consumptions. The deviation from the nominal current consumption can be about ±0.75mA. Four gain settings of the IF filter are selectable via IFFGAIN in register R0 (see 4.1.1). The default value is 0dB, other options are -14dB, -6dB and +6dB. It is recommended to leave the value at 0dB.

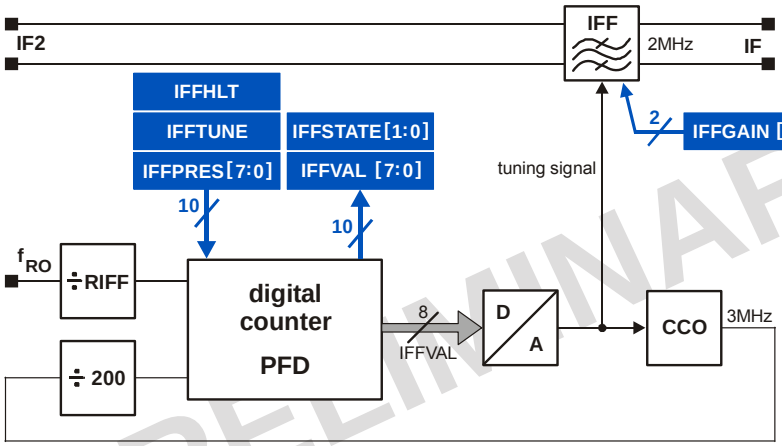


Fig. 12: IF filter auto-tuning circuit

3.4.4 IF Amplifier (IFA)

After passing the IF filter the receiving signal is amplitude limited by means of a high gain limiting amplifier. Its small signal gain is about 68dB. A received signal strength indicator (RSSI) voltage is generated in the IF amplifier. It is available at pin RSSI. The voltage at this pin is proportional to the input level of the receiver (in dB scales). There are two sensitivity settings selectable with RSSIGAIN (see 4.1.2), one with about 39mV/dB and the default setting with about 51mV/dB. By using this RSSI output signal the incoming signal strength of different transmitters can be determined. The same RSSI signal is used for receiving ASK modulated signals if MODSEL (see 4.1.6) is HIGH.

The IFA generates two digital signals RSSIL and RSSIH that indicate the level range of the RSSI voltage. If the level is in the lower quarter of the RSSI voltage range then both signals are LOW. If it is in the upper quarter of the RSSI range then both signals are HIGH. In between, the RSSIL signal is HIGH and RSSIH is LOW. Both values can be read out from register R7 of the IC (see 4.1.8). These two signals are also used for the AGC feature.

3.4.5 Automatic Gain Control (AGC)

The Automatic Gain Control (AGC) can be activated in SPI mode with AGCEN (see 4.1.4). By default, it is turned off. It uses the RSSIH and RSSIL signals of the IF amplifier to determine whether the gain has to be increased or decreased. The gain will be decreased beginning with the gain of the last stage. The gain increase works vice versa. The AGC circuit controls the gain of the LNA, and of mixer 1 and mixer 2. To avoid rapid gain switching, caused by short signal strength fluctuations or during ASK reception, the gain control operates with a time delay that can be programmed via AGCDEL (see 4.1.4). The time delay also depends on the PFD frequency of the IF filter auto-tuning circuit. There is no delay by default. AGCMODE (see 4.1.5), a second setting, determines whether the delay is applied for gain increase and decrease or only for gain increase. By default, a delay for increase and decrease is used.

3.4.6 FSK Demodulator

FSK reception is turned on if bit MODSEL in register R5 is set to LOW (default). The demodulator is completely internally implemented, so no external, expensive discriminator device is needed. The used FSK demodulator is based on a LC phase shifter and a mixer. The phase shifter provides a phase shift of 90 degrees to the original IF signal at exactly 10.7MHz. The phase shift is regulated by the same control loop that controls the center frequency of the IF-filter. Tuning of the IF-filter will also change the DC value of the demodulator output. We recommend stalling the tuning in the reception phase with IFFHLT (see 4.1.7) for small frequency deviations below ±20kHz. The gain of the demodulator can be changed with bit DEMGAIN (see 4.1.1). It can be set to 12mV/kHz (default) or to 14.5mV/kHz.

3.5 Data Path

The data path contains all circuitry that is used to process the baseband signal. The MLX71122 comprises a second order Sallen-Key lowpass filter, two peak detectors and an output comparator as digital signal output.

3.5.1 Data Filter (DF)

The receive part of the MLX71122 contains a 2nd order Sallen-Key low-pass filter that can be configured by connecting two external capacitors C8 and C9 to the IC (see sec. 6). This data filter removes high frequency components and noise from the demodulated signal that may otherwise lower the signal to noise ratio at the comparator input. The filter bandwidth has to be adjusted to the maximum data rate. A good choice for the -3dB bandwidth is 75% of the data rate for NRZ codes and 150% for bi-phase or Manchester codes.
A Bessel characteristic is best used in the data filter.
Since the internal resistors of the filter are both 200kΩ and the overall gain is set to unity we obtain the following table for the capacitor values:

Coding	C8	C9
NRZ Code	$1.33 \cdot C9$	$\frac{640\,pF}{data\ rate\ /\ kbps}$
Bi-Phase Code	$1.33 \cdot C9$	$\frac{320\,pF}{data\ rate\ /\ kbps}$

Example: base band signal 4kbps, NRZ coding

$$C9 = \frac{640pF}{4[kbps]} = 160pF \qquad \text{in E-series} \Rightarrow \quad C9 = 150pF$$

$$C8 = 1.33 \cdot 150pF = 200pF \qquad \text{in E-series} \Rightarrow \quad C8 = 220pF$$

3.5.2 Averaging Data Slicer Mode

The averaging data slicer mode is the default setting for the data path of the MLX71122. Bit SLCSEL in register R0 (see 4.1.1) is LOW if it is active and switch SW2 connects the pin SLC with DFO via a 200kΩ resistor (see Fig. 1). With an external capacitor C10 at pin SLC, a simple low pass filter is formed that generates the threshold voltage for the output comparator. The value of C10 depends on the length of the packet preamble, the coding and the data rate. The larger the C10 value the longer the time until valid output data can be received at pin DTAO.
We recommend using the averaging data slicer mode for bi-phase or Manchester encoded bit streams since the DC-content of these codes is almost zero. The RC-time constant of the slicer can be calculated using:

$$t_{SLC} = 200k\Omega \cdot C10 \qquad (15)$$

We recommend that t_{SLC} is at least 25 times as long as the bit time of the equivalent NRZ signal.

Example: base band signal 4kbps, NRZ coding

$$C10 = \frac{25 \cdot 0.25ms}{200k\Omega} = 31.25nF \qquad \text{in E-series} \Rightarrow \quad C10 = 33nF$$

3.5.3 Peak Detectors (PKDET)

Peak detector mode is recommended for fast acquisition of the received data and if NRZ code is used. We recommend to turn off the IFF auto tuning after the PLL lock during FSK-reception in peak detector mode. The peak detectors can be activated by setting SLCSEL to HIGH in register R0 (see 4.1.1). This connects SLC (pin 32) with the resistive voltage divider between PDP (pin 25) and PDN (pin 26) (see Fig. 1). The peak detector at PDP is used to detect the maximum of the voltage at DFO and the peak detector at PDN detects the minimum of the voltage at DFO. Since the voltage divider is symmetric, the threshold voltage will be in the middle of the minimum and maximum voltages at DFO. The peak voltages are proportional to the charge that is stored on the peak detector capacitors at PDP (C11) and PDN (C12). All pull-up and pull-down currents are given in sec. 5.5. Because both pins are connected via a 2MΩ resistor, both peak detector capacitors will be discharged with a time constant depending on the value of the capacitors. For equal values of both capacitors (C = C11 = C12), the time constant will be:

$$t_{DIS} = 2M\Omega \cdot 0.5 \cdot C \qquad (16)$$

The minimum value of t_{DIS} is limited by the maximum number of equally consecutive bits. A value of t_{DIS} of at least 128 times the bit time is a good choice since this is a common data package length.

Example: base band signal 4kbps, NRZ coding

$$C11 = C12 = \frac{128 \cdot 0.25ms}{0.5 \cdot 2M\Omega} = 32nF \qquad \text{in E-series} \Rightarrow \quad C11 = C12 = 33nF$$

The maximum capacitor value may also be limited by the pull-up and pull-down currents of the peak detectors given in sec. 5.5, because C11 and C12 have to be charged during the first bits of the preamble of the data packet. It is also possible to connect the PDN capacitor to the positive supply in order to speed up the charging after the first power-up of the circuit.

3.5.4 Output Comparator

The output comparator or data slicer decides whether the incoming signal is a digital LOW or HIGH by using the reference voltage at SLC (pin 32). If the internal voltage is larger than the reference then the output is HIGH and vice versa. Nevertheless, the polarity of the output comparator can be inverted. The driving capability of the comparator output is ±2mA and in standby mode the tri-state output is at high impedance.
Pin DTAO must not be connected by a low impedance to a fixed voltage supply or a stronger driver output! We recommend using a series resistance of 10kΩ to connect DTAO.

3.6 Frequency Acceptance Range

The frequency acceptance range is defined as the bandwidth where the input sensitivity can be degraded by 3dB at a maximum, compared to the sensitivity at the center frequency of the channel.
Typically, the frequency acceptance range of the MLX71122 is about 180kHz, see Fig.13.
The frequency acceptance range is mainly depending on the frequency deviation, and slightly on the modulation frequency. The larger the frequency deviation the smaller the acceptance range.

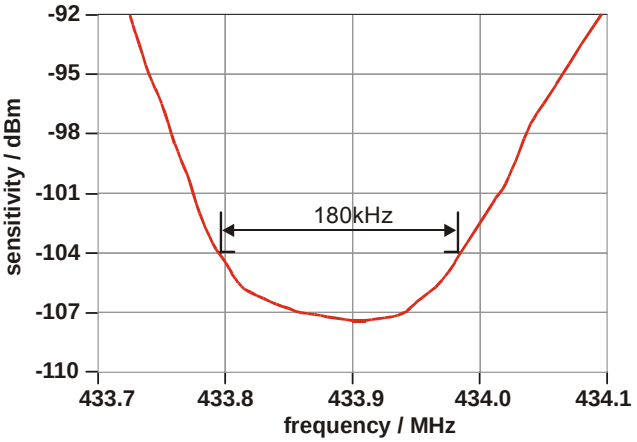


Fig. 13: Measured sensitivity characteristic (BER=$3 \cdot 10^{-3}$, 4kbps, Δf=±20kHz)

3.7 Biasing System

The biasing system needs an external 30kΩ resistor that is connected between RBIAS (pin 10) and the PCB ground. The band-gap voltage at RBIAS causes a reference current flow of about 42µA through this reference current resistor. The accuracy of the external resistor should be within ±2%. To minimize the temperature dependency it is recommended to use a metal film resistor.

3.8 Operating Modes

The MLX71122 has four operating modes having an impact on the receiver's current consumption. The OPMODE bits in register R0 (see 4.1.1) determine the operating mode. Selections are:

- 00 – Shutdown — all blocks deactivated, only SPI active (default)
- 01 – Receive — receiving data from LNAI at selected frequency
- 10 – RO and bias only — only biasing system and reference oscillator are working
- 11 – Synthesizer only — only biasing system, reference oscillator and PLL are working

The first operating mode consumes virtually no current. The circuit is dead except of the SPI that can listen to commands. In Receive mode all necessary blocks are turned on in order to receive data at the programmed frequency.
The last two operating modes can be used to accelerate the start-up time of the circuit after periods of silence. With RO and bias only, the start-up time of the reference oscillator (RO) can be circumvented. RO and biasing consume not as much current as the whole receiver. With Synthesizer only the full PLL is already working and locked. Current consuming blocks as the LNA, the IF-filter and the FSK-demodulator are turned off in this state. The last mode is useful if the receiver has to listen frequently.

3.9 Multi Functional Output

The Multi Functional Output (pin 23) can be used to read out the control register settings or to make other internal signals available at this pin. The output is controlled by the bits MFO in register R3 (see 4.1.4). The most important selections are:

- 0000 – Z-State — MFO pin is in high impedance mode
- 0001 – SPI-out — MFO pin is digital serial output for data of registers (default in SPI-mode)
- 0010 – Logic-0 — MFO pin is pulled to ground
- 0011 – Logic-1 — MFO pin is pulled to VCC
- 0100 – RO-out — MFO pin is buffered, analogue output of RO frequency (default in ABC-mode)
- 0101 – IF-out — MFO pin is buffered, analogue output of IF2 signal after the IF-filter
- 1000 – LD-out — MFO pin represents lock state of PLL

Z-State, Logic-0 and Logic-1 can be used to provide digital control signals to other circuits on the PCB. In state RO-out a 10MHz clock frequency is available at MFO, e.g. for driving a microcontroller. At IF-out pin MFO provides the IFF output, amplified by a factor of 5 (unloaded). In this case the output resistance is about 610Ω. The IF-out mode can be used for checking the IFF characteristics or for further signal processing, e.g. to add an external limiting amplifier and demodulator. With the LD-out setting the state of the PLL can be read out. All other selections are for test purposes

3.10 SPI Description

3.10.1 General

Serial programming interface (SPI) mode can be activated by choosing SPISEL = 1 (e.g. at positive supply voltage V_{CC}). In this mode, the input pins 17, 18 and 19 are used as a 3-wire unidirectional serial bus interface (SDEN, SDTA, SCLK). The internal latches contain all user programmable variables including counter settings, mode bits etc.

In addition the MFO pin can be programmed as an output (see section 4.1.4) in order to read data from the internal latches and it can be used as an output for different test modes as well.

At each rising edge of the SCLK signal, the logic value at the SDTA terminal is written into a shift register. The programming information is taken over into internal latches with the rising edge of SDEN. Additional leading bits are ignored, only the last bits are serially clocked into the shift register. A normal write operation shifts 16 bits into the SPI, a normal read operation shifts 4 bits into the SPI and reads additional 12 bits from the MFO pin. If less than 12 data bits are shifted into SDTA during the write operation then the control register may contain invalid information.

In general a control word has the following format. Bit 0 is the Read/Write bit that determines whether it is a read (R/W = 1) or a write (R/W = 0) sequence. The R/W bit is preceding the latch address and the corresponding data bits.

Control Word Format															
MSB											LSB	MSB		LSB	Bit 0
Data												Latch Address			Mode
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A2	A2	A0	R/W

There are two control word formats for read and for write operation. Data bits are only needed in write mode. Read operations require only a latch address and a R/W bit.

Due to the static CMOS design, the serial interface consumes virtually no current. The SPI is a fully separate building block and can therefore be programmed in every operational mode.

3.10.2 Read / Write Sequences

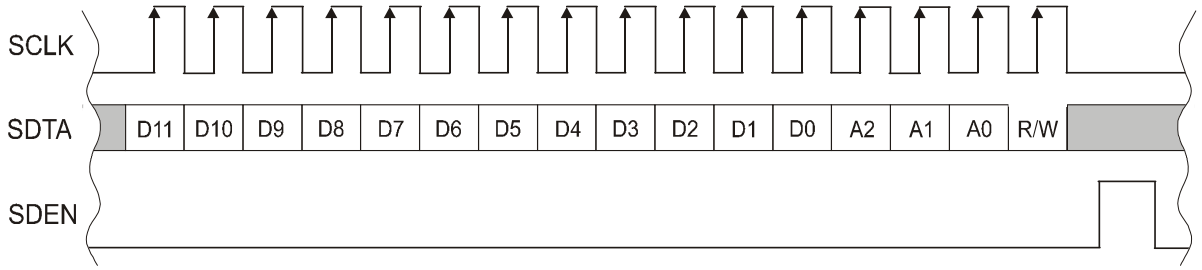


Fig. 14 Typical write sequence diagram

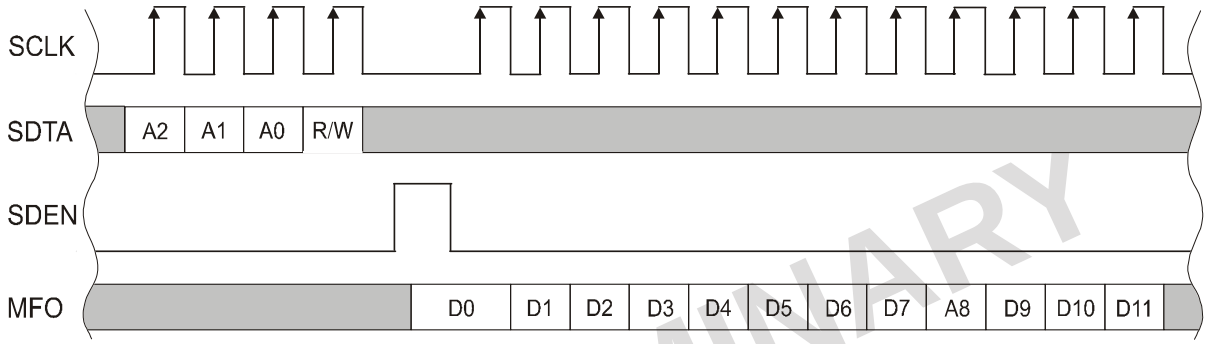


Fig. 15 Typical read sequence diagram

3.10.3 Serial Programming Interface Timing

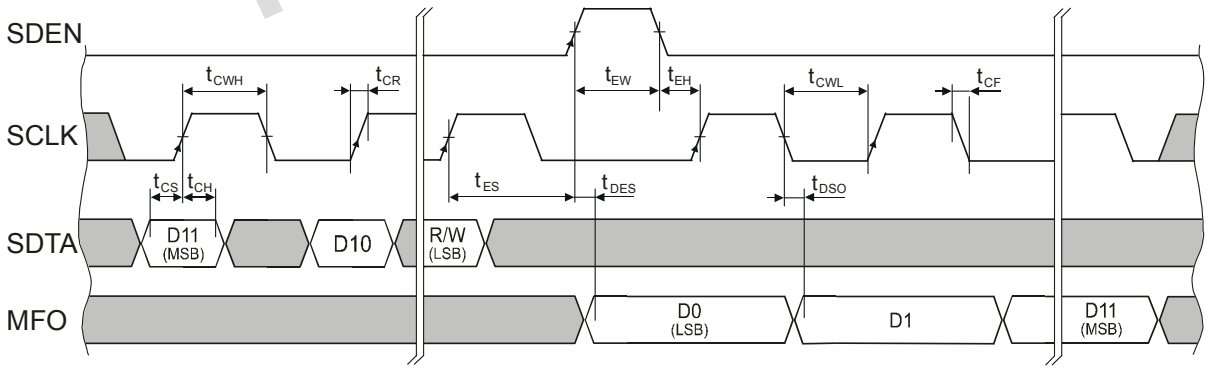


Fig. 16 SPI timing diagram

4 Register Description

The following tables are to describe the functionality of the registers.

Sec. 4.1 provides a register overview with all the control words R0 to R7. The subsequent sections. 4.1.1 to 4.1.8 show the content of the control words in more detail.

Programming the registers requires SPI mode (SPISEL = 1). Default settings are for ABC mode.

4.1 Register Overview

CONTROL WORD	DATA MSB											LSB	LATCH ADDRESS MSB		LSB
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0
R0	DTAPOL	SLCSEL	SSBSEL	DEMGAIN	IFFGAIN [1:0]		MIX2GAIN	MIX1GAIN	LNAGAIN [1:0]		OPMODE [1:0]		read/ write		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	1	0	0	0	1	1	1	1	0	1	0	0	0	0	1
R1	SHOWLD	PRESCUR	VCOBUF	VCOCUR	VCORANGE	RSSIGAIN	LDTIME [1:0]		LDERR	PFDPOL	CPCUR [1:0]		read/ write		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	1	1	1	1	0	0	0	1	0	1	0	0	0	1	0
R2	N [6:0]							A [4:0]					read/ write		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1
R3	MFO [3:0]				AGCDEL [1:0]		AGCEN	LO2DIV	N [10:7]				read/ write		

CONTROL WORD	DATA MSB											LSB	LATCH ADDRESS		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	0	0	0	0	0	1	0	0	1	0	1	1	1	0	0
R4	AGCMODE	R [10 : 0]											read/ write		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	0	0	1	0	1	0	1	0	1	1	0	0	1	0	1
R5	MODSEL	RIFF [10 : 0]											read/ write		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	1	1	1	0	1	0	0	0	0	1	0	1	1	1	0
R6	ROCUR [1 : 0]		IFFTUNE	IFFHLT	IFFPRES [7 : 0]								read/ write		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default													1	1	1
R7	RSSIH	LDRSSIL*	IFFSTATE [1 : 0]		IFFVAL [7 : 0]								read-only		

Note: * depends on bit 11 in R4, 0 = RSSIL, 1 = LD

4.1.1 Control Word R0

Name	Bits	Description		
OPMODE	[1:0]	operation mode		
		00	**shutdown**	#default
		01	**receive mode**	
		10	**reference oscillator & BIAS only**	
		11	**synthesizer only**	
LNAGAIN	[3:2]	LNA gain		
		00	**lowest gain** **(default – 20dB)**	
		01	**low gain** **(default – 6dB)**	
		10	**high gain** **(default – 2dB)**	
		11	**highest gain** **(default – 0dB)**	#default
			gain values are relative to gain at default	
MIX1GAIN	[4]	1st Mixer gain		
		0	**high gain** **(14dB)**	#default
		1	**low gain** **(0dB)**	
MIX2GAIN	[5]	2nd Mixer gain		
		0	**high gain** **(9dB)**	#default
		1	**low gain** **(-2dB)**	
IFFGAIN	[7:6]	intermediate frequency filter gain		
		00	**lowest gain** **(-14dB)**	
		01	**low gain** **(-6dB)**	
		10	**high gain** **(0dB)**	#default
		11	**highest gain** **(+6dB)**	
DEMGAIN	[8]	demodulator gain		
		0	**low gain** **(~ 12mV/kHz)**	#default
		1	**high gain** **(~ 14.5mV/kHz)**	
SSBSEL	[9]	single side band selection		
		0	**upper side band** **LO2 low-side inj. (IF1 = LO2 + IF2)**	#default
		1	**lower side band** **LO2 high-side inj. (IF1 = LO2 – IF2)**	
			Internal IF2 = 2MHz	
SLCSEL	[10]	slicer mode select		
		0	**averaging Data Slicer mode**	#default
		1	**peak detector Data Slicer mode**	
DTAPOL	[11]	data output polarity OA2		
		0	**inverted**	#default
			'1' for space at ASK or f_{min} at FSK, '0' for mark at ASK or f_{max} at FSK	
		1	**normal**	
			'0' for space at ASK or f_{min} at FSK, '1' for mark at ASK or f_{max} at FSK	

4.1.2 Control Word R1

Name	Bits	Description		
CPCUR	[1:0]	charge pump current setting		
		00	**100µA**	#default
		01	**400µA**	
		10	**400µA static down**	
		11	**400µA static up**	
PFDPOL	[2]	PFD output polarity		
		0	**negative**	
		1	**positive**	#default
LDERR	[3]	lock detector time error		
		0	**15ns**	#default
		1	**30ns**	
LDTIME	[5:4]	lock detection time		
		00	**2/f_R**	
		01	**4/f_R**	
		10	**8/f_R**	
		11	**16/f_R**	#default
		minimum time span before lock in f_R is the reference oscillator frequency f_{RO} divided by R, see section 4.1.5 (R4)		
RSSIGAIN	[6]	sensitivity of RSSI voltage		
		0	**low gain (~39mV/dB)**	
		1	**high gain (~51mV/dB)**	#default
VCORANGE	[7]	VCO range		
		0	**3V supply**	
		1	**5V supply**	#default
		VCO range setting for different VCCs.		
VCOCUR	[8]	VCO core current		
		0	**450µA**	#default
		1	**520µA**	
VCOBUF	[9]	VCO buffer current		
		0	**900µA**	#default
		1	**1040µA**	
PRESCUR	[10]	prescaler 32/33 reference current		
		0	**20µA**	#default
		1	**30µA**	
		30µA may be used for f_{RF} = 868/915MHz		
SHOWLD	[11]	function of LDRSSIL bit		
		0	**RSSIL (RSSI low flag)**	
		1	**LD (lock detection flag)**	#default
		select output data of LDRSSIL, see section 4.1.8 (R7)		

4.1.3 Control Word R2

Name	Bits	Description		
A	[4:0]	swallow counter value		
		10100	**value is 20**	#default
			swallow counter range: 0 to 31	
N	[11:5]	program counter value (bits 0 – 6)		
		000 0111 1000	**N value is 120**	#default
			N counter range: 3 to 2047	

4.1.4 Control Word R3

N	[3:0]	program counter range (bits 7 – 10)		
		000 0111 1000	**N value is 120**	#default
			N counter range: 3 to 2047	
LO2DIV	[4]	LO2 divider ratio		
		0	**divide by 4**	#default
		1	**divide by 8**	
AGCEN	[5]	AGC enable mode		
		0	**disabled**	#default
		1	**enabled**	
AGCDEL	[7:6]	AGC delay settings		
		00	**no delay**	#default
		01	**3/f_{IFF}**	
		10	**15/f_{IFF}**	
		11	**31/f_{IFF}**	
			f_{IFF} is the reference oscillator frequency f_{RO} divided by RIFF, see section 4.1.6 (R6)	
MFO	[11:8]	multi functional output		
		0000	**MFO is in Z state**	#default
		0001	**MFO is SPI read-out**	
		0010	**MFO = 0**	
		0011	**MFO = 1**	
		0100	**MFO is analog RO output**	
		0101	**MFO is IFF output**	
		1000	**MFO is lock detector output**	

4.1.5 Control Word R4

Name	Bits	Description		
R	[10:0]	reference divider range		
		000 0100 1011	**value is 75**	#default
			R counter range: 3 to 2047	
AGCMODE	[11]	AGC delay mode		
		0	**gain decrease and increase with delay**	#default
		1	**gain decrease without delay, gain increase with delay**	
			selects AGC delay mode in combination with AGCDEL bits, see section 4.1.4 (R3)	

4.1.6 Control Word R5

Name	Bits	Description		
RIFF	[10:0]	reference divider value for IFF adjustment		
		010 1010 1100	**value is 684**	#default
			IFF counter range: 4 to 2047	
MODSEL	[11]	demodulation selection		
		0	**FSK demodulation**	#default
		1	**ASK demodulation**	
			selects modulation type when chip is controlled via SPI mode	

4.1.7 Control Word R6

Name	Bits	Description		
IFFPRES	[7:0]	IFF preset value		
		0101 1011	**value is 91**	#default
			IFF DAC preset at start of automatic tuning	
IFFHLT	[8]	IFF halt		
		0	**auto tuning running**	#default
		1	**auto tuning halted**	
			suspends IFF automatic tuning	
IFFTUNE	[9]	IFF tuning		
		0	**disable and load DAC with IFFPRES**	
		1	**enable**	#default
ROCUR	[11:10]	reference Oscillator core current		
		00	**85µA**	
		01	**170µA**	
		10	**270µA**	
		11	**355µA**	#default

4.1.8 Control Word R7 (Read-only Register)

Name	Bits	Description
IFFVAL	[7:0]	IFF adjustment value
		see also IFFPRES in section 4.1.7 (R6)
IFFSTATE	[9:8]	IFF automatic tuning state
		00 filter tuned or auto-tuning disabled **01 tuning up the filter frequency** **10 tuning down the filter frequency** **11 master oscillator of filter does not work**
LDRSSIL	[10]	lock detector or RSSI low flag
		0 PLL not locked or RSSI value in lower region **1 PLL locked or RSSI value above lower region**
		depends on SHOWLD in section 4.1.2 (R1)
RSSIH	[11]	RSSI high flag
		0 RSSI value below upper region **1 RSSI value in upper region**

5 Technical Data

5.1 Absolute Maximum Ratings

Operation beyond absolute maximum ratings may cause permanent damage of the device.

Parameter	Symbol	Condition / Note	Min	Max	Unit
Supply voltage	V_{CC}		0	7.0	V
Input voltage	V_{IN}		- 0.3	V_{cc}+0.3	V
Input RF level	P_{iRF}	@ LNA input		10	dBm
Storage temperature	T_{STG}		-55	+125	°C
Junction temperature	T_J			+150	°C
Thermal Resistance	R_{thJA}			60	K/W
Power dissipation	P_{diss}			0.1	W
Electrostatic discharge	V_{ESD1}	human body model, 1)	-1.0	+1.0	kV
	V_{ESD2}	human body model, 2)	-0.75	+0.75	

1) all pins except LNAO
2) pin LNAO

5.2 Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{CC}		3.0	5.5	V
Operating temperature	T_A		-40	+105	ºC
Input low voltage (CMOS)	V_{IL}	ENRX, SEL pins, A/SCLK B/SDTA, C/SDEN		$0.3 \cdot V_{CC}$	V
Input high voltage (CMOS)	V_{IH}	ENRX, SEL pins, A/SCLK B/SDTA, C/SDEN	$0.7 \cdot V_{CC}$		V
Input frequency range	f_{RF}		300	930	MHz
IF1 range	f_{IF1}		80	190	MHz
IF2 range	f_{IF2}			2	MHz
XOSC frequency	f_{ref}	set by the crystal		10	MHz
VCO frequency	f_{LO}		400	750	MHz
Frequency offset of carrier	f_{CAR}		-100	100	kHz
Frequency deviation	Δf		±2	±50	kHz
FSK data rate	R_{FSK}	NRZ		100	kbps
ASK data rate	R_{ASK}	NRZ		100	kbps
FM bandwidth	f_m			15	kHz

5.3 Crystal Parameters

Parameter	Symbol	Condition	Min	Max	Unit
Crystal frequency	f_0	fundamental mode, AT		10	MHz
Load capacitance	C_L		10	15	pF
Static capacitance	C_0			7	pF
Series resistance	R_1			70	Ω

5.4 Serial Programming Interface (SPI)

Parameter	Symbol	Condition	Min	Max	Unit
Input High Voltage	V_{IH}		V_{CC} - 0.4		V
Input Low Voltage	V_{IL}			0.4	V
SLCK frequency	f_{SLCK}			10	MHz
SLCK period	t_{SLCK}		100		ns
SDTA to SCLK set up time	t_{CS}		20		ns
SCLK to SDTA hold time	t_{CH}		20		ns
SCLK pulse width low	t_{CWL}		50		ns
SCLK pulse width high	t_{CWH}		50		ns
SCLK to SDEN set up time	t_{ES}		30		ns
SDEN pulse width	t_{EW}		50		ns
SDEN to SCLK hold time	I		20		ns
Rising Edge of SLCK	t_{CR}			0.1 t_{SLCK}	ns
Falling Edge of SLCK	t_{CF}			0.1 t_{SLCK}	ns
SDEN to MFO data set-up time	t_{DES}			70	ns
SCLK to MFO data set-up time	t_{DSO}			50	ns
MFO max. pin load capacitance	C_{LMFO}			20	pF

5.5 DC Characteristics

all parameters under normal operating conditions and default settings, unless otherwise stated;
typical values at T_A= 23 °C and V_{CC} = 5 V
all parameters based on test circuits as shown in Fig. 17 to Fig. 19

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Currents						
Shutdown current	I_{SBY}	OPMODE=00 and ENRX=0		50	500	nA
Supply current, FSK	I_{FSK}	OPMODE=01 or ENRX=1	10	12	15	mA
Supply current, ASK	I_{ASK}	OPMODE=01 or ENRX=1	9.5	11.5	14.5	mA
Supply current, RO only	I_{RO}	OPMODE=10 and ENRX=0	0.4	0.8	1.2	mA
Supply current, Synthesizer only	I_{SYN}	OPMODE=11 and ENRX=0	3	4	5	mA
Digital Pin Characteristics						
Input low voltage CMOS, ENRX	V_{ILEN}	ENRX pin	-0.3		$0.3 \cdot V_{cc}$	V
Input high voltage CMOS, ENRX	V_{IHEN}	ENRX pin	$0.7 \cdot V_{CC}$		V_{CC}+0.3	V
Pull down current ENRX pin	I_{PDEN}	ENRX=1	3.5	5	7	µA
Low level input current ENRX pin	I_{INLEN}	ENRX=0			0.05	µA
Input low voltage CMOS	V_{IL}	Pins MODSEL, SPISEL, A/SCLK, B/SDTA, C/SDEN	-0.3		$0.3 \cdot V_{cc}$	V
Input high voltage CMOS	V_{IH}	Pins MODSEL, SPISEL, A/SCLK, B/SDTA, C/SDEN	$0.7 \cdot V_{CC}$		V_{CC}+0.3	V
Low level input leakage current	I_{IL}	Pins MODSEL, SPISEL, A/SCLK, B/SDTA, C/SDEN	-2			µA
High level input leakage current	I_{HL}	Pins MODSEL, SPISEL, A/SCLK, B/SDTA, C/SDEN			2	µA
Analog Pin Characteristics						
OA1 input offset voltage	V_{OFFOA1}	OA1	-20		20	mV
OA2 input offset voltage	V_{OFFOA2}	OA2	-20		20	mV
OA2 current sinking capability	$I_{OA2SINK}$	OA2 (DTAO pin)			2	mA
OA2 current sourcing capability	I_{OA2SRC}	OA2 (DTAO pin)			2	mA
Peak detector P pull-up current	I_{PDPPU}	PDP		235		µA
Peak detector N pull-down current	I_{PDNPD}	PDN		270		µA

5.6 AC System Characteristics

all parameters under normal operating conditions and default settings, unless otherwise stated;
typical values at T_A = 23 °C and V_{CC} = 5 V, RF at 433.92 MHz
all parameters based on test circuits as shown in Fig. 17 to Fig. 19

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Receive Characteristics						
Input sensitivity – FSK (standard)	$P_{min, FSK}$	$\Delta f = \pm 20kHz$, 4kbps NRZ, BER $\leq 3 \cdot 10^{-3}$		-107		dBm
Input sensitivity – FSK (with carrier offset)	$P_{min, FSK, offs}$	$\Delta f = \pm 20kHz$, 4kbps NRZ, ±90kHz carrier offset BER $\leq 3 \cdot 10^{-3}$		-104		dBm
Input sensitivity – ASK	$P_{min, ASK}$	100% on-off ratio 4kbps NRZ, BER $\leq 3 \cdot 10^{-3}$		-112		dBm
Maximum input signal – FSK/FM	$P_{max, FSK}$	BER $\leq 3 \cdot 10^{-3}$		0		dBm
Maximum input signal – ASK	$P_{max, ASK}$	BER $\leq 3 \cdot 10^{-3}$		-10		dBm
Spurious emission	P_{spur}				-54	dBm
Image rejection of MIX2	ΔP_{imag}			35		dB
IF Filter Parameters						
Center frequency	f_{IF}			2		MHz
3dB bandwidth	B_{3dB}			230		kHz
40dB bandwidth	B_{40dB}			1.6		MHz
RSSI Characteristics						
Low voltage	V_{LRSSI}	high gain			0.75	V
High voltage	V_{HRSSI}	high gain	2.65			V
RSSI dynamic range	DR_{RSSI}			50		dB
RSSI sensitivity, low gain	S_{RSSIL}	low gain		39		mV/dB
RSSI sensitivity, high gain	S_{RSSIH}	high gain		51		mV/dB
FSK Demodulator						
Demodulator gain, low	DG_{LOW}			12		mV/ kHz
Demodulator gain, high	DG_{HIGH}			14.5		
Maximum data rate	B_{DEM}	NRZ			100	kbps
Frequency acceptance range	BW_{DEMOD}	$\Delta f = \pm 20kHz$	150			kHz
Start-up Parameters						
Crystal start-up time	T_{XTL}			0.9		ms
Receiver start-up time	T_{RX}	depends on data slicer time constant, valid data at output			T_{XTL} + 200k · C10	
PLL Parameters						
VCO gain @ 433MHz	K_{VCO}	max for VCORANGE=0		83	100	MHz/V
VCO gain @ 868MHz	K_{VCO}	max for VCORANGE=0		105	126	MHz/V
Charge pump current	I_{CP}	depends on CPCUR	100		400	µA

6 Test Circuits

6.1 Standard FSK & ASK Reception in 8-Channel Preconfigured (ABC) Mode

6.1.1 Averaging Data Slicer Configured for Bi-Phase Codes

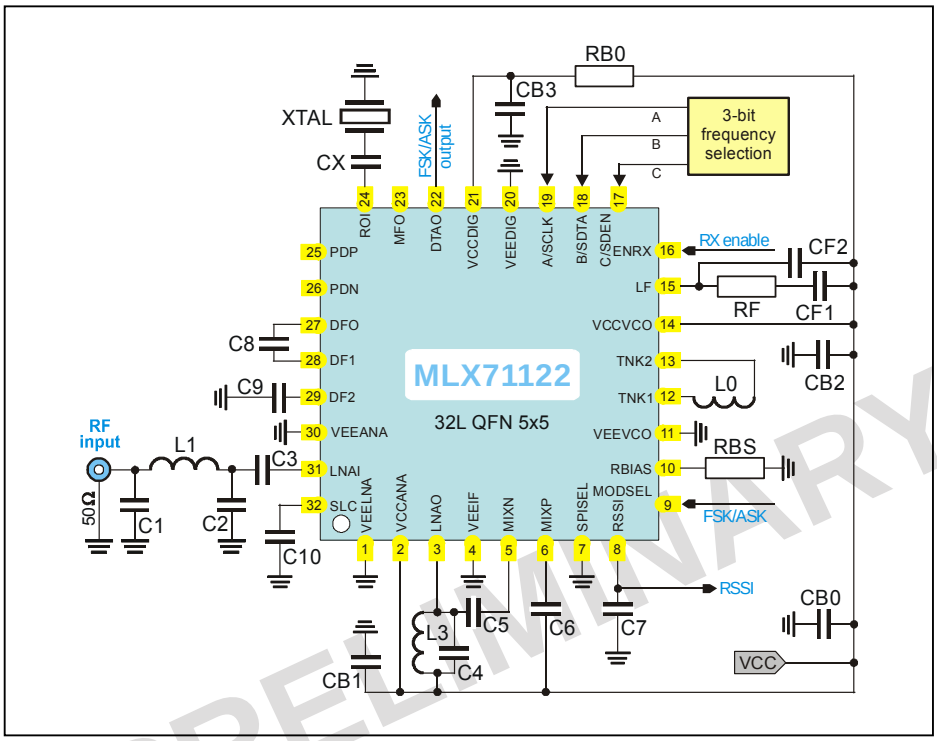


Fig. 17: Test circuit for FSK & ASK reception

6.2 Standard FSK & ASK Reception in SPI Mode

6.2.1 Averaging Data Slicer Configured for Bi-Phase Codes

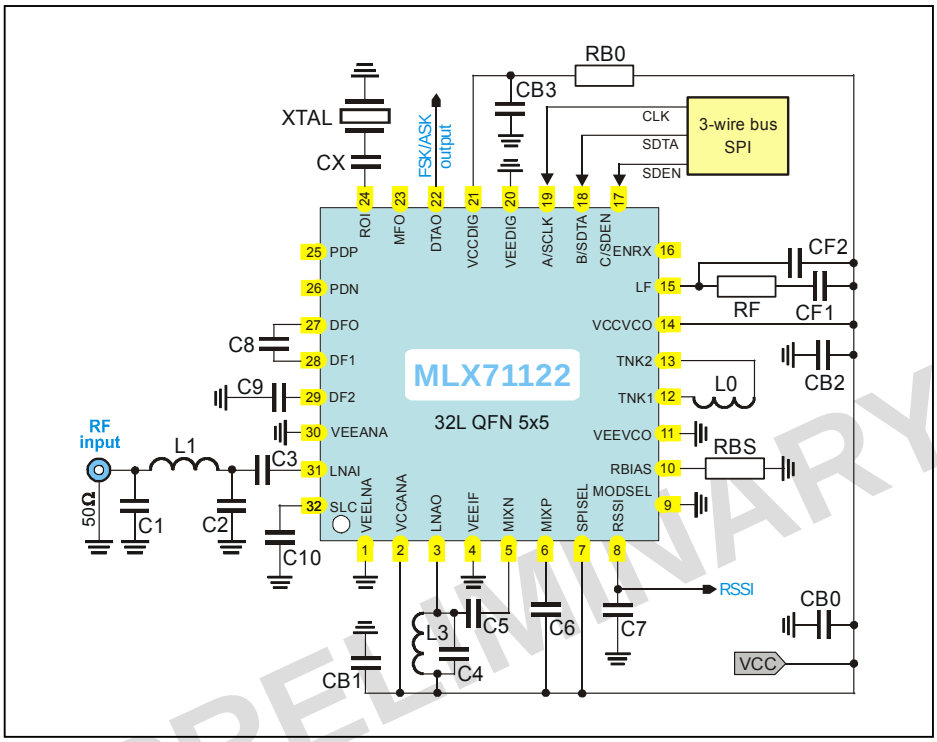


Fig. 18: Test circuit for FSK & ASK reception

6.2.2 Peak Detector Data Slicer Configured for NRZ Codes

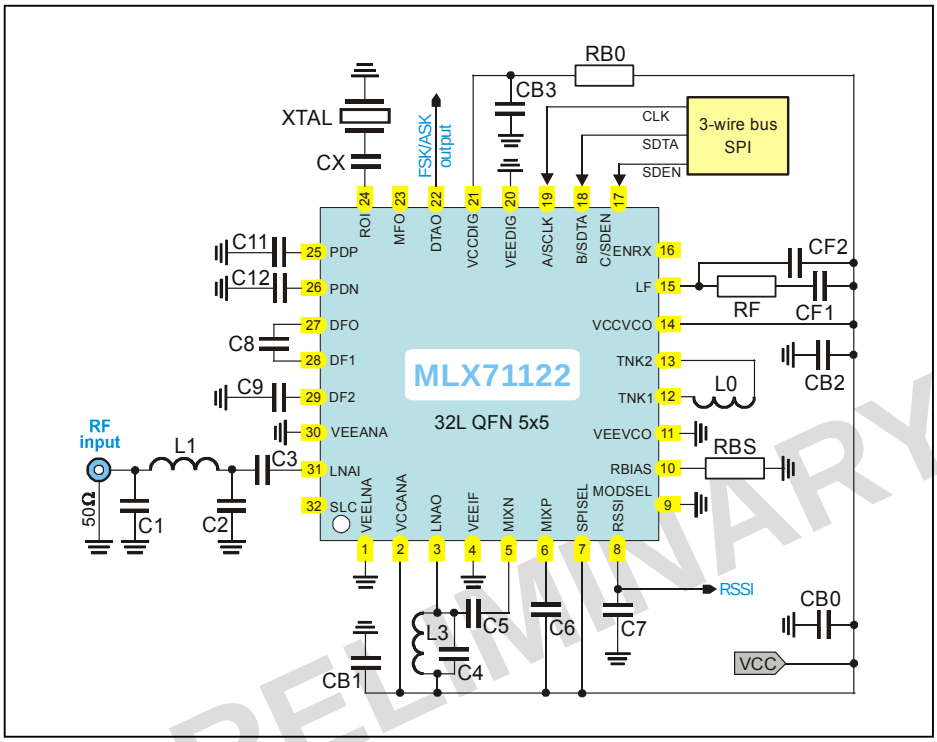


Fig. 19: Test circuit for FSK & ASK reception

6.3 Test Circuit Component List

Below table is for all test circuits shown in Figures 17 to 19.

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Value @ 868.3 MHz	Value @ 915 MHz	Tol.	Description
C1	0603	3.9 pF	4.7 pF	3.3 pF	1.5 pF	±5%	matching capacitor
C2	0603	1.5 pF	1.5 pF	1.5 pF	1.5 pF	±5%	matching capacitor
C3	0603	100 pF	100 pF	100 pF	100 pF	±5%	LNA input filtering capacitor
C4	0603	4.7 pF	3.3 pF	2.7 pF	2.2 pF	±5%	LNA output tank capacitor
C5	0603	100 pF	100 pF	100 pF	100 pF	±5%	MIX1 negative input matching capacitor
C6	0603	100 pF	100 pF	100 pF	100 pF	±5%	MIX1 negative input matching capacitor
C7	0603	1 nF	1 nF	1 nF	1 nF	±10%	RSSI output low pass capacitor, for data rate of 4 kbps NRZ
C8	0603	220 pF	220 pF	220 pF	220 pF	±10%	data low-pass filter capacitor, for data rate of 4 kbps NRZ
C9	0603	150 pF	150 pF	150 pF	150 pF	±10%	data low-pass filter capacitor, for data rate of 4 kbps NRZ
C10	0603	33 nF	33 nF	33 nF	33 nF	±10%	data slicer capacitor, for data rate of 4 kbps NRZ
		not required in Figure 19					
C11	0603	33 nF	33 nF	33 nF	33 nF	±10%	PKDET positive filtering capacitor, for data rate of 4 kbps NRZ
		not required in Figures. 17 and 18					
C12	0603	33 nF	33 nF	33 nF	33 nF	±10%	PKDET negative filtering capacitor, for data rate of 4 kbps NRZ
		not required in Figures 17 and 18					
CB0	1210	10 µF	10 µF	10 µF	10 µF	±10%	decoupling capacitor, low-noise power supply recommended
CB1	0603	470 pF	470 pF	470 pF	470 pF	±10%	decoupling capacitor
CB2	0603	33 nF	33 nF	33 nF	33 nF	±10%	decoupling capacitor
CB3	0603	33 nF	33 nF	33 nF	33 nF	±10%	decoupling capacitor
CF1	0603	2.2 nF	2.2 nF	2.2 nF	2.2 nF	±5%	loop filter capacitor
CF2	0603	220 pF	220 pF	220 pF	220 pF	±5%	loop filter capacitor
CX	0603	27 pF	27 pF	27 pF	27 pF	±5%	crystal series capacitor
RB0	0603	10 Ω	10 Ω	10 Ω	10 Ω	±5%	protection resistor
RF	0603	27 kΩ	27 kΩ	47 kΩ	47 kΩ	±5%	loop filter resistor
RBS	0603	30 kΩ	30 kΩ	30 kΩ	30 kΩ	±2%	reference bias resistor
L0	0603	33 nH	15 nH	8.2 nH	8.2 nH	±5%	VCO tank inductor
L1	0603	68 nH	47 nH	22 nH	15 nH	±5%	matching inductor
L3	0603	33 nH	22 nH	5.6 nH	5.6 nH	±5%	LNA output tank inductor
XTAL	SMD 5x3.2	10.00000 MHz ±20ppm cal., ±30ppm temp.					fundamental-mode crystal

7 Package Description

The device MLX71122 is RoHS compliant.

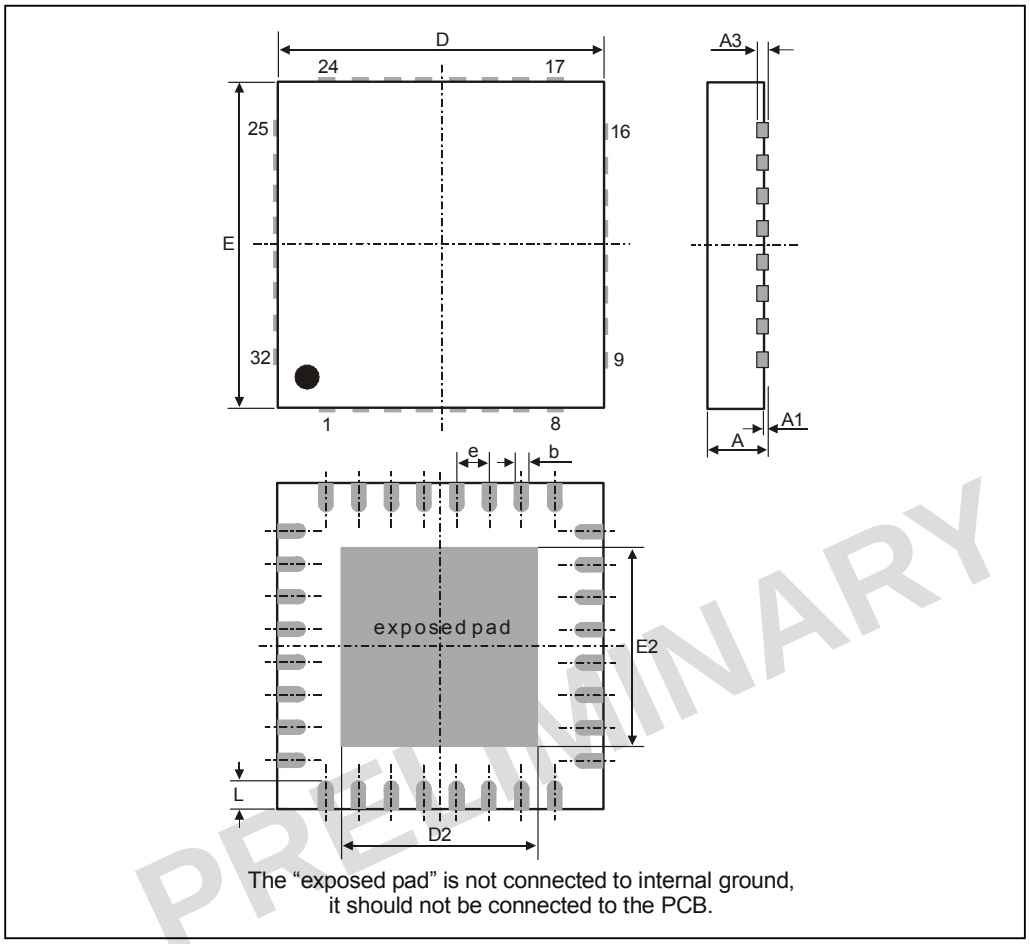


Fig. 20: 32L QFN 5x5 Quad

all Dimension in mm										
	D	**E**	**D2**	**E2**	**A**	**A1**	**A3**	**L**	**e**	**b**
min	4.75	4.75	3.00	3.00	0.80	0	0.20	0.3	0.50	0.18
max	5.25	5.25	3.25	3.25	1.00	0.05		0.5		0.30
all Dimension in inch										
min	0.187	0.187	0.118	0.118	0.0315	0	0.0079	0.0118	0.0197	0.0071
max	0.207	0.207	0.128	0.128	0.0393	0.002		0.0197		0.0118

7.1 Soldering Information

- The device MLX71122 is qualified for MSL3 with soldering peak temperature 260 deg C according to JEDEC J-STD-20

8 Reliability Information

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)"

Wave Soldering SMD's (Surface Mount Devices)

- EN60749-20
  "Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat"

Solderability SMD's (Surface Mount Devices)

- EIA/JEDEC JESD22-B102
  "Solderability"

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

9 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

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Europe, Africa:	Americas:	Asia:
Phone: +32 1367 0495	Phone: +1 603 223 2362	Phone: +32 1367 0495
E-mail: sales_europe@melexis.com	E-mail: sales_usa@melexis.com	E-mail: sales_asia@melexis.com

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