MLC852P

8-bit OTP MCU with 1120 dots LCD Driver

Features

- single chip 8-bit micro-controller
- Operating voltage: 2.4V to 5.5V
- Memory :
  - One-Time-Programmable (OTP) ROM: 64K Bytes
  - Data RAM (stack RAM included) : 3328 Bytes (0000h ~ 0CFFh)
  - LCD RAM : 144 Bytes
- 20 input/output pins:
  - Dedicated I/O pins: P0[0:3]
  - Share pin I/O:
    - P0[4]/SEG[69]
    - P0[5:7]/SEG[66:64]
    - P1[0:1]/UART(TX, RX)
    - P2[0:7]/SEG[63:56]
    - P3[0:1]/SEG[68:67]/(SDIO, SCLK)
- Half duplex UART function
- Build-in Megawin E-flash interface
- Dedicated SPK pin for tone/DAC
- LCD driver output:
  - Max 70 segment × 16 common
  - 1/16 duty 1/5 bias driving mode
  - Build-in voltage regulator and pumper to generate LCD voltage for LCD driver
  - 10 level programmable frame rate from 56.7Hz to 113.8Hz
  - 16-level adjustable VLCD from 3.5 V to 5.75 V
- One 8-bit resolution DAC output
- Programmable sample rate for voice/melody function
- Two reloadable 8-bit timers
- Two dividers

  One 14-bit divider with the clock source from sub-oscillator to generate a 2-Hz interrupt

  One 7-bit divider with the clock source from main oscillator
- Build-in dual oscillation circuit:
  - Ring oscillator up to
    5MHz at 3.6V – 5.5V
    4MHZ at 2.4V – 3.4V
    for main oscillator (Fosc)
  - 32768Hz crystal oscillator for sub-oscillator (F_{x32})
- Build-in 8-level battery-low detector circuit
- Build-in serial interface to program the OTP ROM.

MEGAWIN

Pad Description

Pad Name	I/O	Description
P0.0 ~ P0.3	I/O	Programmable I/O ports with interrupt function
SPK	O	Tone/DAC output
P1.0 ~ P1.1/(TX, RX)	I/O	1. Port 1 bit0 ~ bit1 2. UART interface
GND, VDD	P	Power pins
OSCI	I	Ring oscillator input pin. Connect to external resistor
X32I	I	32768 Hz crystal input
X32O	O	32768 Hz crystal output
/RES	I	System reset pin (low active)
COM0 ~ COM15	O	LCD common signals output pins
SEG0 ~ SEG55	O	LCD segment signals output pins
SEG69/P0.4	I/O	1. LCD segment signals output pins 2. Port 0 bit4
SEG56 ~ SEG63/P2.7 ~ P2.0	I/O	1. LCD segment signals output pins 2. Port 2 bit0 ~ bit7
SEG68 ~ SEG67/(SDIO, SCLK)/P3.0 ~P3.1	I/O	1. LCD segment signals output pins 2. e_Flash interface 3. Port 3 bit0 ~ bit1
SEG66 ~ SEG64/P0.5 ~P0.7	I/O	1. LCD segment signals output pins 2. Port 0 bit5 ~ bit7
VLCD V4 – V1	O	Outputs for VLCD bias
CUP1 – CUP4	O	Charge pump capacitor interconnection pins
VPP	I	OTP cell interface (Please refer note 2.)
SCK	I	OTP cell interface
SDA	I/O	OTP cell interface
CMD	I	OTP cell interface

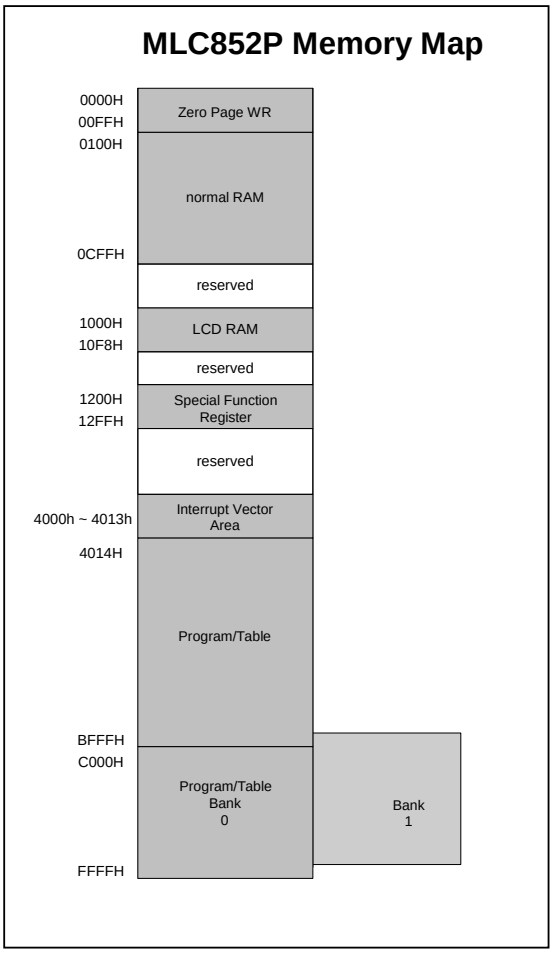
Total 112 pins

Memory Map

There are **3328 bytes** SRAM in MLC852P, addressing from 0000H to 0CFFH. They could be used as data RAM or stack RAM (0100h ~ 01FFh) by user's arrangement. The locations from 1200H to 12FFH are special function registers area.

There are **64K** bytes program/data ROM in MLC852P. It includes 32K common ROM, 4000h ~ BFFFh, and bank ROM, C000h ~ FFFFh. There are 2 banks in MLC852P. When the uC access the bank ROM, the value of BANK register decides which bank would be accessed. The default value of the BANK register is 00H after power on or reset.

The address mapping of MLC852P is shown as below.



Special Function Register (SFR)

The addresses from 1200H to 12FFH are reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, timers, system clock and other peripheral.

SFR (special function register): 00C0H ~ 00FFH (page 0 area)

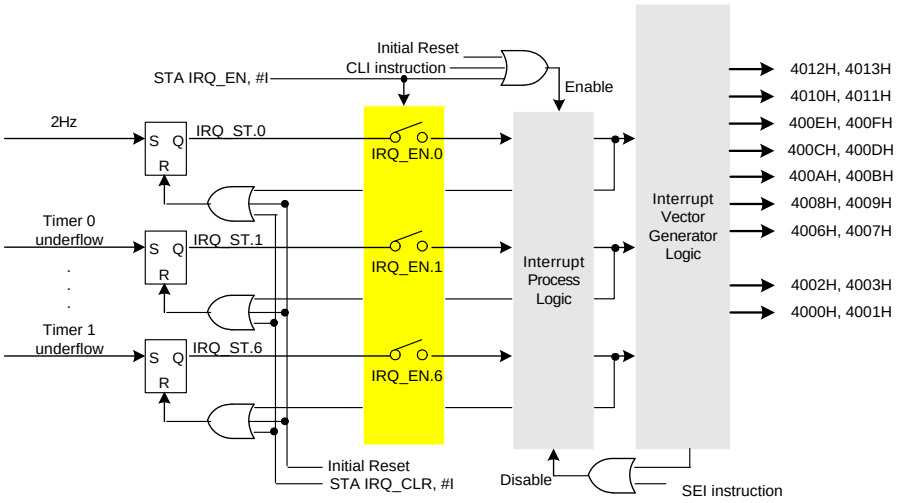
Address	Content	Default	Address	Content	Default
1200	IRQ_EN / IRQ_ST	00	1210	P1PULL	00
1201	IRQ_CLR	00	1211	P2	00
1202		00	1212	P2DIR	00
1203	DIV1x_SEL	00	1213	P2CONF	00
1204	TM0	00	1214	P2PULL	00
1205	TM0_CTL	00	1215	P3	00
1206	TM1	00	1216	P3DIR	00
1207	TM1_CTL	00	1217	P3CONF	00
1208	P0	00	1218	P3PULL	00
1209	P0DIR	00	1219	MFR_0	00
120A	P0CONF	00	121A	MFR_1	00
120B	P0PULL	00	121B	STB_COM	00
120C	P0STB	00	121C	BL_CR	00
120D	P1	00	121D	E_RW	00
120E	P1DIR	00	121E	E_buffer	00
120F	P1CONF	00	121F		

Address	Content	Default	Address	Content	Default
1220	LCD_CR	00	1230	BANK	00
1221	LCD_VC	00	1231	PWR_CR	00
1222			1232	FCPU_SR	00
1223	AUD_CTL	00	1233		
1224	CH0	00	1234	P0_latch	00
1225			1235	SET_FRAME	00
1226			1236		
1227			1237		
1228			1238		
1229			1239		
122A	UART_SETUP	00	123A		
122B	UART_CTRL	00	123B		
122C	UART_TBUF	00	123C		
122D	UART_RBUF	00	123D		
122E	UART_STS	00	123E		
122F			123F		

Interrupt Vectors

Vector Address	Item	Priority	Properties	Memo
4000H, 4001H	BRK	3	Int.	Software BRK interrupt vector
4002H, 4003H	RESET	1	Ext.	Initial reset
4004H, 4005H	-	-	-	Reserved
4006H, 4007H	2HZ	4	Int.	2Hz interrupt
4008H, 4009H	TM0x	5	Int.	Timer 0 overflow interrupt
400AH, 400BH	P0x	6	Ext.	Port P0 interrupt vector
400CH, 400DH	KEY	7	Ext	Key scan trigger
400EH, 400FH	DIV1x	8	Int.	Divider 1 selected stage overflow
4010H, 4011H	UART	9	Int.	UART receive/transmit finished interrupt
4012H, 4013H	TM1x	10	Int.	Timer 1 overflow interrupt

There are 7 interrupt sources provided in MLC852P. The flag IRQ_EN and IRQ_ST are used to control the interrupt events. When one flag of IRQ_ST is set to '1' by hardware and the corresponding bits of flag IRQ_EN has been set by software, an interrupt request is generated. When an interrupt process occurs, all of the interrupts are inhibited until the CLI or STA IRQ_EN, #I instruction is invoked. Executing the SEI instruction can also disable the interrupt requests.



Interrupt Registers

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1200H	IRQ_EN	-	TM1	UART	DIV1X	KEY	P0	TM0	2HzX	-	√

Program can enable or disable the ability of triggering IRQ through this register.

0: Disable (default “0” at initialization)

1: Enable

P0: Raising or falling edge occurs at port 0 input mode

TM0: Timer 0 underflow

2HzX: 2Hz ring edge

DIV1X: divider selected stage rising edge

UART: UART transmit or receive finished

KEY: key scan trigger

TM1: Timer 1 underflow

IRQ status flag (same address with IRQ_EN)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1200H	IRQ_ST	-	TM1	UART	DIV1X	KEY	P0	TM0	2HzX	√	-

When IRQ occurs, program can read this register to know which source triggering IRQ.

IRQ clear flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1201H	IRQ_CLR	-	TM1	UART	DIV1X	KEY	P0	TM0	2HzX	-	√

Program can clear the interrupt event by writing ‘1’ into the corresponding bit.

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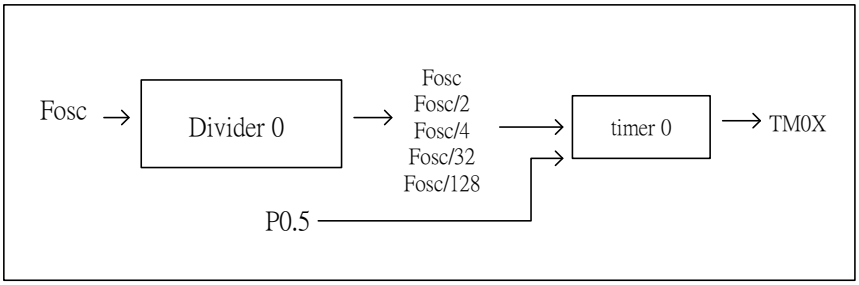
Dividers

Divider0 is a 7-bit up-counter. The clock source is from Fosc. It could be reset to 00H by POR, system reset or waked from stop mode. Certain intermediary signals of the divider 0 could be the clock source of timer0.



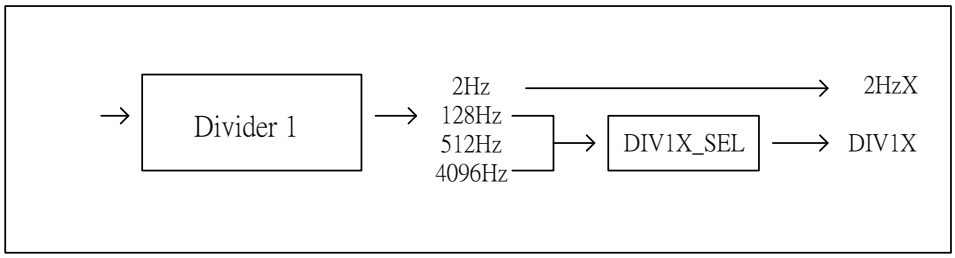
Divider1:

Divider1 is a 14-bit up-counter. The clock source is from sub-oscillator (32 KHz). It could be reset to 0000H by POR, system reset or waked from stop mode. DIV1x_sel could select the source of interrupt.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1203H	DIV1x_SEL	-	-	-	-	-	-	CKO1	CKO0	√	√

CKO1	CKO0	Selected DIV1x frequency
0	0	F_{x32}/256 (128Hz)
0	1	F_{x32}/128 (512Hz)
1	0	F_{x32}/8 (4096Hz)
1	1	unused

The default clock source is F_{x32}/256 (128Hz)



System Control Registers

Bank select

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1230H	BANK	-	-	-	-	BK3	BK2	BK1	BK0	√	√

Program can switch the memory bank through this register. When the uC access the bank ROM, the region of C000h ~ FFFFh, the value of the BANK register decides which bank would be accessed. After power on reset, this register in initialized as 00H. For more detailed information, refer to memory map description.

Power saving control

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1231H	PWR_CR	-	-	-	-	-	CKC1	CKC0	CPUOFF	-	√

CPUOFF: uC clock source (Fcpu) control bit. 1: Fcpu disabled, 0: Fcpu enabled

CKC1	CKC0	System clock control
0	0	F_{OSC} enable, F_{X32} enable (Dual mode)
0	1	unused
1	0	F_{OSC} disable, F_{X32} enable (Halt mode)
1	1	F_{OSC} disable, F_{X32} disable (Stop mode)

PWR_CR is default 00H.

Program could switch the uC operation from normal mode to the power saving modes to save power consumption through the PWR_CR register. MLC852P provides three power saving modes.

CPU OFF mode: *(PWR_CR.CKC1 = 0, PWR_CR.CKC0 = 0, PWR_CR.CPUOFF = 1)*
The clock input path of the uC is disabled. The 2 oscillators keep oscillating but the uC stops executing program. The uC can be awakened by interrupt events.

Halt mode: *(PWR_CR.CKC1 = 1, PWR_CR.CKC0 = 0)*
The main oscillator stops oscillating and the uC stops executing program. The sub-oscillator keeps oscillating though. The main oscillator and the uC can be awakened by interrupt events.

Stop mode: *(PWR_CR.CKC1 = 1, PWR_CR.CKC0 = 1)*
Both main oscillator and sub-oscillator stop oscillating. The uC can be awakened from stop mode by 3-ways: status change of P0, hardware reset and power-on reset.

FCPU selector

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1232H	FCPU_SR	-	-	-	-	-	-	CKS1	CKS0	-	√

CKS1	CKS0	Selected Fosc/x (0201H) frequency
0	0	Fosc / 1 (default)
0	1	Fosc / 2
1	0	Fosc / 4
1	1	Fosc / 8

The FCPU_SR register selects the clock source of uC among the 4 signals, Fosc, Fosc/2, Fosc/4 and Fosc/8. The default clock source is Fosc.

Timers/Counters

Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1204H	TM0	T7	T6	T5	T4	T3	T2	T1	T0	√	√
1205H	TM0_CTL	STC	-	-	-	-	TK02	TK01	TK00	√	√

STC: Start/Stop counting. 1: load the TM0 value to TM0 counter, and start down counting; 0: stop counting

Note that setting this bit to 1 will be ignored if this bit is already 1.

TK02, TK01 and TK00: select timer 0 input clock source.

TK02	TK01	TK00	Selected TM0 input clock source
0	0	0	Fosc
0	0	1	Fosc / 2
0	1	0	Fosc / 4
0	1	1	Fosc / 32
1	0	0	Fosc/128
1	0	1	P0.5
1	1	0	Un-used
1	1	1	Un-used

Note that, if P0.5 is selected as the timer clock, user must configure the pin P0.5 as an input.

Timer1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1206H	TM1	T7	T6	T5	T4	T3	T2	T1	T0	√	√
1207H	TM1_CTL	STC	-	-	-	-	TK12	TK11	TK10	√	√

STC: Start/Stop counting. 1: load the TM0 value to TM0 counter, and start down counting; 0: stop counting

Note that setting this bit to 1 will be ignored if this bit is already 1.

TK12, TK11 and TK10: select timer 1 input clock source.

TK12	TK11	TK10	Selected TM1 input clock source
0	0	0	Fosc
0	0	1	Fosc / 2
0	1	0	Fosc / 4
0	1	1	Fosc / 32
1	0	0	Fosc/128
1	0	1	P0.6
1	1	0	Un-used
1	1	1	Un-used

Note that, if P0.6 is selected as the timer clock, user must configure the pin P0.6 as an input.

I/O Ports

Port 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1208H	P0	P07	P06	P05	P04	P03	P02	P01	P00	√	√
1209H	P0DIR	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0	√	√
120AH	P0CONF	CON7	CON6	CON5	CON4	CON3	CON2	CON1	CON0	√	√
120BH	P0PULL	STR7	STR6	STR5	STR4	STR3	STR2	STR1	STR0	√	√
120CH	P0STB	STB7	STB6	STB5	STB4	STB3	STB2	STB1	STB0	√	√

Port 0 is an 8-bit I/O port. Each pin can be programmed as input or output individually.

P0 (Port 0 buffer)

When Port0.n is configured as an output pin, the Port0.n pin would output the logic content of P0.n. Whether the Port0.n is configured as an input or an output pin, reading P0.n would always read the logic value from pad.

P0DIR (Port 0 Direction)

P0DIR.n = 0: P0.n is configured as an input pin. (Default)

P0DIR.n = 1: P0.n is configured as an output pin.

P0CONF (Port 0 pull-high/CMOS/NMOS setting)

When P0DIR.n is 0 (input mode),

P0CONF.n = 0: The weak internal pull-high resistor of P0.n is enabled. (Default)

P0CONF.n = 1: The weak internal pull-high resistor of P0.n is disabled.

When P0DIR.n is 1 (output mode),

P0CONF.n = 0: P0.n is a CMOS output pin. (Default)

P0CONF.n = 1: P0.n is a NMOS output pin.

P0PULL (Port 0 pull-high resistor selection)

P0PULL.n = 0: The strong pull-high resistor of P0.n is disabled. (Default)

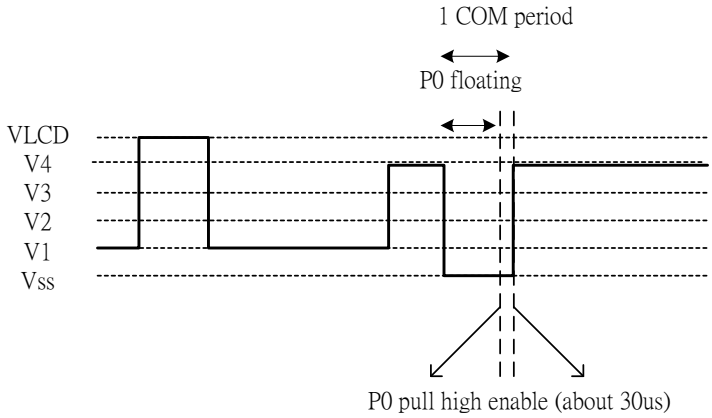
P0PULL.n = 1: The strong pull-high resistor of P0.n is enabled.

P0STB (Port 0 key strobe function enable/disable)

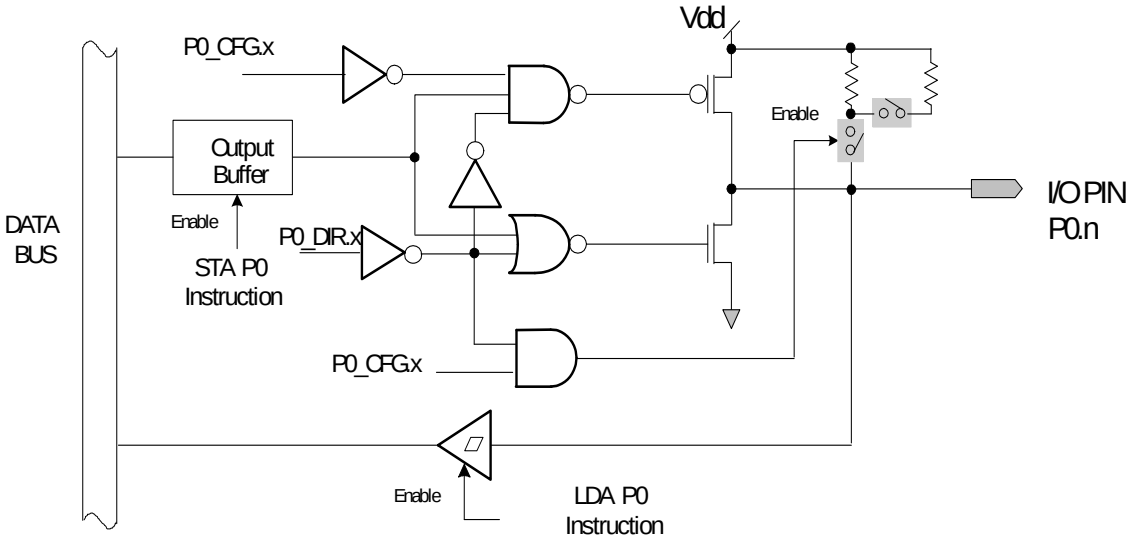
P0STB.n = 0: Disable the key strobe function of P0.n. (Default)

P0STB.n = 1: Enable the key strobe function of P0.n.

When internal pull-high register is enabled (strong or weak) and the P0STB.n is 0, the P0.n is always pulled high. When internal pull-high register is enabled and the P0STB.n is 1, P0.n is pulled high only for the last 30 microseconds of the low-active period of each LCD COM. This mechanism is to reduce the interferences on LCD COM signals when P0.n and COM.m are short-circuited.



Input/Output Pin of the P0



Port 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
120DH	P1							P11	P10	√	√
120EH	P1DIR								DIR0	√	√
120FH	P1CONF								CON0	√	√
1210H	P1PULL								STR0	√	√

Port 1 is a 2-bit I/O port. This port can be programmed as input or output. Port 1 could also be used as UART interface.

P1 (Port 1 buffer)

When Port1.n is configured as an output pin, the Port1.n pin would output the logic content of P1.n. Whether the Port1.n is configured as an input or an output pin, reading P1.n would always read the logic value from pad.

P1DIR (Port 1 Direction)

P1DIR.0 = 0: P1.0 and P1.1 are both configured as input pins. (Default)

P1DIR.0 = 1: P1.0 and P1.1 are both configured as output pins.

P1CONF (Port 1 pull-high/CMOS/NMOS setting)

When P1DIR.0 is 0 (input mode),

P1CONF.0 = 0: The weak internal pull-high resistors of P1.1 and P1.0 are both enabled. (Default)

P1CONF.0 = 1: The weak internal pull-high resistors of P1.1 and P1.0 are both disabled.

When P1DIR.0 is 1 (output mode),

P1CONF.0 = 0: P1.1 and P1.0 are both CMOS output pins. (Default)

P1CONF.0 = 1: P1.1 and P1.0 are both NMOS output pins.

P1PULL (Port 1 pull-high resistor selection)

P1PULL.n = 0: The strong pull-high resistors of P1.1 and P1.0 are both disabled. (Default)

P1PULL.n = 1: The strong pull-high resistors of P1.1 and P1.0 are both enabled.

Port 2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1211H	P2	P27	P26	P25	P24	P23	P22	P21	P20	√	√
1212H	P2DIR							DIR1	DIR0	√	√
1213H	P2CONF							CON1	CON0	√	√
1214H	P2PULL							STR1	STR0	√	√

Port 2 is an 8-bit I/O port; high nibble and low nibble can be programmed as input or output individually.

P2 (Port 2 buffer)

When Port2.n is configured as an output pin, the Port2.n pin would output the logic content of P2.n. Whether the Port2.n is configured as an input or an output pin, reading P2.n would always read the logic value from pad.

P2DIR (Port 2 Direction)

P2DIR.n = 0: P2[4n+3:4n] are configured as input pins where n = 0 and 1. (Default)

P2DIR.n = 1: P2[4n+3:4n] are configured as output pins where n = 0 and 1.

P2CONF (Port 2 pull-high/CMOS/NMOS setting)

When P2DIR.n is 0 (input mode),

P2CONF.n = 0: The weak internal pull-high resistors of P2[4n+3:4n] are enabled where n = 0 and 1. (Default)

P2CONF.n = 1: The weak internal pull-high resistors of P2[4n+3:4n] are disabled where n = 0 and 1.

When P2DIR.n is 1 (output mode),

P2CONF.n = 0: P2[4n+3:4n] are CMOS output pins where n = 0 and 1. (Default)

P2CONF.n = 1: P2[4n+3:4n] are NMOS output pins where n = 0 and 1.

P2PULL (Port 2 pull-high resistor selection)

P2PULL.n = 0: The strong pull-high resistors of P2[4n+3:4n] are disabled where n = 0 and 1. (Default)

P2PULL.n = 1: The strong pull-high resistors of P2[4n+3:4n] are enabled where n = 0 and 1.

Port 3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1215H	P3							P31	P30	√	√
1216H	P3DIR								DIR0	√	√
1217H	P3CONF								CON0	√	√
1218H	P3PULL								STR0	√	√

Port 3 is an 2-bit I/O port; this port can be programmed as input or output. Port 3 could also be used as e-flash serial interface.

P3 (Port 3 buffer)

When Port3.n is configured as an output pin, the Port3.n pin would output the logic content of P3.n. Whether the Port3.n is configured as an input or an output pin, reading P3.n would always read the logic value from pad.

P3DIR (Port 3 Direction)

P3DIR.0 = 0: P3.0 and P3.1 are both configured as input pins. (Default)

P3DIR.0 = 1: P3.0 and P3.1 are both configured as output pins.

P3CONF (Port 3 pull-high/CMOS/NMOS setting)

When P3DIR.0 is 0 (input mode),

P3CONF.0 = 0: The weak internal pull-high resistors of P3.1 and P3.0 are both enabled. (Default)

P3CONF.0 = 1: The weak internal pull-high resistors of P3.1 and P3.0 are both disabled.

When P3DIR.0 is 1 (output mode),

P3CONF.0 = 0: P3.1 and P3.0 are both CMOS output pins. (Default)

P3CONF.0 = 1: P3.1 and P3.0 are both NMOS output pins.

P3PULL (Port 3 pull-high resistor selection)

P3PULL.0 = 0: The strong pull-high resistors of P3.1 and P3.0 are both disabled. (Default)

P3PULL.0 = 1: The strong pull-high resistors of P3.1 and P3.0 are both enabled.

Port multi-function register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1219H	MFR_0	SI	P3	UART	SEG64	SEG65	SEG66	-	SEG69	√	√
121AH	MFR_1							SEG5659	SEG6063	√	√

The MFR_0 and MFR_1 could switch the functions of multi-functioned ports and LCD segments. The default values of MFR_0 and MFR_1 are both 00h.

MFR_0:

SEG69

0: SEG69 is normal LCD output

1: SEG69 is port P0.4

SEG66

0: SEG66 is normal LCD output,

1: SEG66 is port P0.5

SEG65

0: SEG65 is normal LCD output

1: SEG65 is port P0.6

SEG64

0: SEG64 is normal LCD output

1: SEG64 is port P0.7

UART

0: Port 1.0/Port1.1 are normal I/O port

1: port1.0/port1.1 are UART interface

(SI, P3)

(X, 0): SEG67/SEG68 are normal LCD output;

(0, 1): SEG67/SEG68 are serial interface SCLK/SDIO;

(1, 1): SEG67/SEG68 are port P3.1/P3.0.

MFR_1:

SEG6063

0: SEG60 to SEG63 are normal LCD output

1: SEG60 to SEG63 are port P2.3 to P2.0

SEG5659

0: SEG56 to SEG59 are normal LCD output

1: SEG59 to SEG56 are port P2.7 to P2.4

Key Strobe function

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
121BH	STB_COM					DEC3	DEC2	DEC1	DEC0	√	
1234H	P0_latch	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	√	

If any single bit of the P0STB register is set to 1, the LCD key strobe function is enabled. Under the following conditions where a P0.n pin senses logic low and its key strobe function is enabled, it would result the corresponding bit of P0_Latch would be **set**, and the current COM number+1, 1 ~ 15 ~ 0, would be latched to register STB_COM. The decoding table for STB_COM value is as follows.

0001:COM0 0010:COM1 0011:COM2 0100:COM3

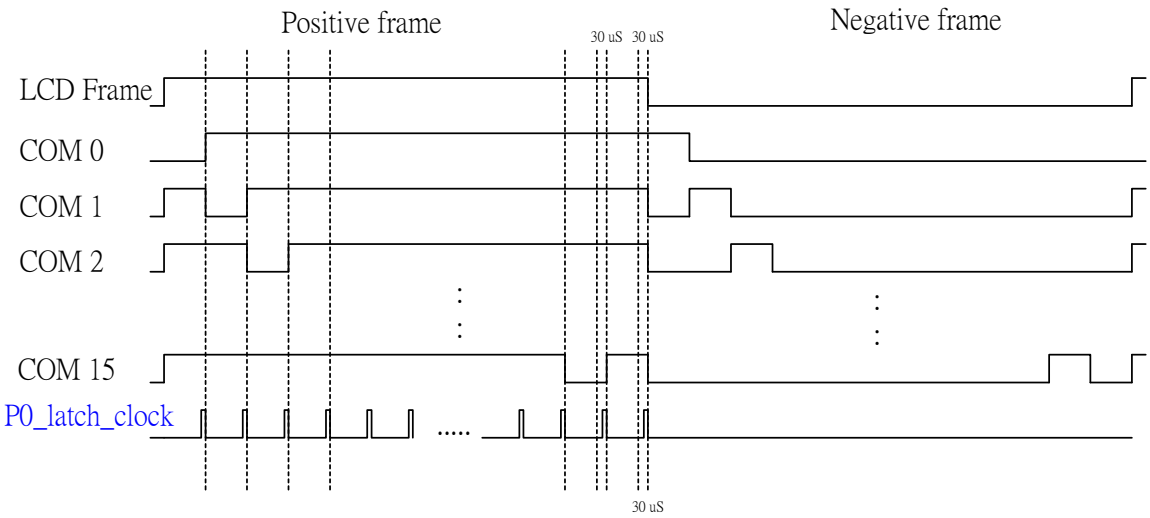
0101:COM4 0110:COM5 0111:COM6 1000:COM7

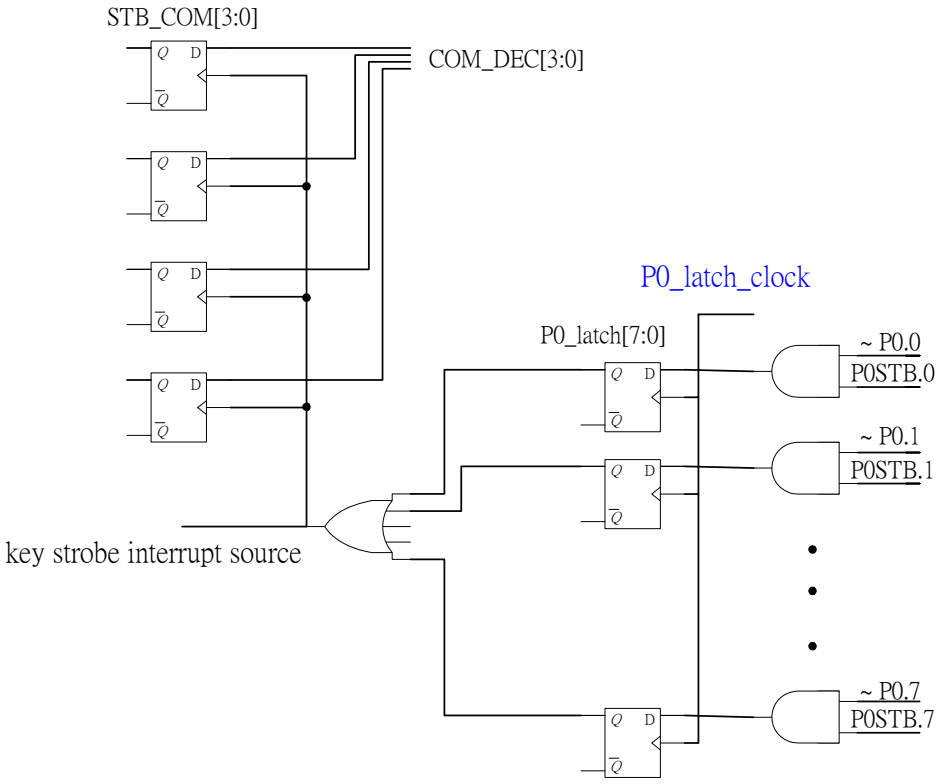
1001:COM8 1010:COM9 1011:COM10 1100:COM11
1101:COM12 1110:COM13 1111:COM14 0000:COM15

Users' program could then judge which pin of key-matrix being pressed by reading the STB_COM and P0_latch registers.

The behavior of the P0_latch register is special. At the middle of the last 30 us of each LCD COM positive-active duration, the P0_latch register would latch the port status. When the value of P0_latch is not 00h, the STB_COM register would record the index of current active LCD COM. Besides, the content of P0_latch could be accessed for once only. That is, whenever it is read, its content would be cleared to 00H by hardware.

The following figure shows the signal of P0_latch clock and the block diagrams of STB_COM and P0_latch circuit.





UART

UART control

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
122AH	UART_SETUP					Auto_cal	RX_pull	TX_opd	EN	√	√
122BH	UART_CTL	BS3	BS2	BS1	BS0	E/O	P			√	√
122CH	UART_TBUF	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0	-	√
122DH	UART_RBUF	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	√	-
122EH	UART_STS	Ring	-	-	-	Tint	Rint	V err		√	√

UART_SETUP:

EN: UART function block enable bit, 0: disable, 1: enable (default is 0)

TX_opd: TX pin open drain control bit, 0: CMOS, 1: open drain (default is 1)

RX_pull: RX pin pull high resistor control bit, 0: disable, 1: enable (default is 0)

Auto_cal: auto calibration control bit and finish bit; set by firmware and clear by hardware User can use program to set this bit to 1 to start clock calibration, then internal hardware will use main clock to generate the clock for UART. When the calibration finish, this bit will be clear by hardware.

UART_CTL:

P: Parity check bit control flag. 0: disable, 1: enable

E/O: Even/Odd parity control flag. 0: even, 1: odd

BS2, BS1, BS0: Baud selector

BS3	BS2	BS1	BS0	Baud rate
0	0	0	0	1200
0	0	0	1	2400
0	0	1	0	4800
0	0	1	1	9600
0	1	0	0	19200

UART_TBUF: UART Tx data buffer

UART_RBUF: UART Rx data buffer

UART_STS:

V err: RBUF overwrite indicator. 0: non-overwrite, 1: overwrite occurs (read and clear)

Note that, to clear this bit, users should write '1' instead of '0'.

Rint: UART Rx data completed interrupt indicator. 1: Rx completed (read and clear)

Note that, to clear this bit, users should write '1' instead of '0'.

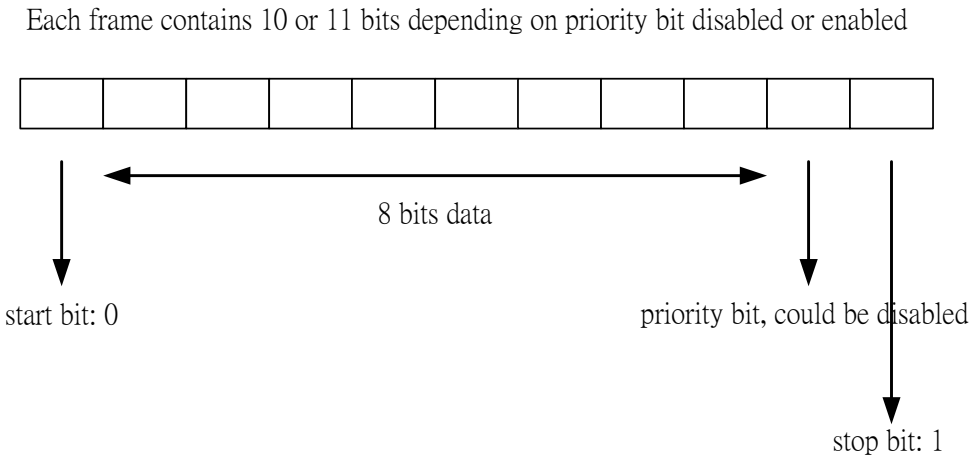
Tint: UART Tx data completed interrupt indicator. 1: Tx completed (read and clear)

Note that, to clear this bit, users should write '1' instead of '0'.

Ring: UART receiving flag. 1: UART is receiving data (read only)

The UART function of MLC852P is half duplex. User could set UART_SETUP and UART_CTRL registers to select the UART operating mode. An interrupt event will be generated when an Rx/Tx operation is completed. UART_STS records the status of the operation. UART_STS is set by hardware and cleared (all but the 'Ring' bit) by writing '1' (writing '0' has no effect) to the bits. The UART_RBUF stores the received data in an Rx operation. Writing data into UART_TBUF would start a Tx operation automatically. The UART_STS.Ring is a flag indicating that the UART module is on receiving. User should not transmit data when the Ring flag is '1'. Besides, for the half duplex limitation, if a receiving operation occurs during a transmitting operation, the both operations would error.

The following figure shows the data format of the UART module.



Battery-Low Detector

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
121CH	BL_CR	BL_I			BLSEL	BL_2	BL_1	BL_0	BL_E	√	√

BL_E: Battery-low control bit. 0: disable (default), 1:enable

BL_I: Battery-low indicator. 0: normal (default), 1: battery voltage is low (this bit is read only)

When the sub-oscillator is enabled and BL_E is set to 1, the battery-low detector is enabled for 30us every 1/1024 second. If the battery voltage is lower than the selected voltage level during the active period of the detector, the BL_I bit would be set. On the contrary, if the battery voltage is higher than the selected voltage level, the BL_I would be cleared. Moreover, when BL_E is cleared, the BL_I would be cleared, too.

Note that the battery-low detect function could be enable only when sub-oscillator is active. If battery-low detector is enabled but the sub-oscillator is disabled, the BL_I will keep the last value before the sub-oscillator stops.

BL_2, BL_1, BL_0: Battery-low level selector.

When BLSEL is 0, (BL_2, BL_1, BL_0) select the voltage level as following (greater then: 0, less then: 1)

000: 2.2V

001: 2.3V

010: 2.4V

011: 2.5V

100: 2.6V

101: 2.7V

110: 2.8V

111: 2.9V

When BLSEL is 1, (BL_2, BL_1, BL_0) select the voltage level as following (greater then: 0, less then: 1)

000: 3.3V

001: 3.45V

010: 3.6V

011: 3.75V

100: 3.9V

101: 4.05V

110: 4.2V

111: 4.35V

E_Flash interface

The MLC852P provides a 2-pin interface for Megawin e_flash series.

When port3 function is switched to e_Flash interface function, a weak pull high resistor will be connected to SDIO pin. In output mode (MLC852P sends data to E-flash), the internal output buffer of SDIO will active only at shift out period.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
121DH	E_RW	M_L					Fsel	start	RW	√	√

RW: SDIO input output control

0 (default): input mode

1: output mode

start:

This bit could be set by firmware and cleared by hardware. When the 'start' bit is set, the SCLK pin would output 8 clocks, and the data would be shifted out or shifted in (according to 'RW' bit) via the SDIO pin. After 8 bits data are shifted in or shifted out, the start bit will be cleared by hardware. Program can check whether a read/write action is finished or not according to the status of the 'start' bit.

Fsel: clock output frequency setting

0 (default): SCLK clock output frequency is Fosc

1: SCLK clock frequency is Fosc/2

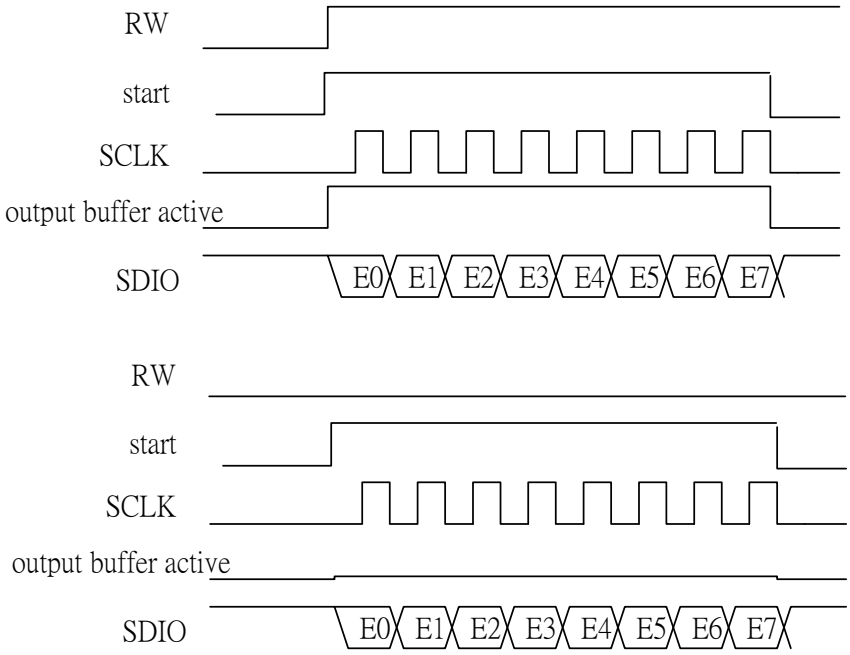
M_L:

0 (default): LSB shift in/out first

1: MSB shift in/out first

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
121EH	E_buffer	E7	E6	E5	E4	E3	E2	E1	E0	√	√

The 8-bit data in E_buffer could be shifted out, and 8-bit external data could be shifted into this register. Note that, for hardware design issue, always configure the 'M_L' bit before writing data into the E_buffer register. Otherwise, the direction of data shift would not be correct.



LCD Controller/Driver

The MLC852P can directly drive an LCD panel by 70 segment output pins and 16 common output pins, totally 70 x 16 LCD dots. LCD control register can be used to select LCD display configuration. The LCD driving mode is 1/5 bias, 1/16 duty. The frame frequency is about 64Hz.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1220H	LCD_CR	LCDON	Mask			RG_E				√	√

LCDON: LCD on/off control bit. 0: off (default), 1:on

Mask

0 (default): segments show the data in LCD ram

1: ALL segment display data '0'

RG_E: LCD regulator/pumpers control bit. 0: disable (default), 1:enable

LCD Voltage Control

The LCD voltage could be selected among 16 levels from 3.5V to 5.75V.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1221H	LCD_VC					L3	L2	L1	L0	√	√

(L3, L2, L1, L0) select the LCD voltage level as following

0000: 3.5V 0001: 3.65V 0010: 3.8V 0011: 3.95V

0100: 4.1V 0101: 4.25V 0110: 4.4V 0111: 4.55V

1000: 4.7V 1001: 4.85V 1010: 5.0V 1011: 5.15V

1100: 5.3V 1101: 5.45V 1110: 5.6V 1111: 5.75V

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1235H	SET_FRAME	Pump_1	Pump_2			Bit3	Bit2	Bit1	Bit0	√	√

(Bit3, Bit2, Bit1, Bit0) select the LCD frame rate as following

0000: 56.8Hz 0001: 60.2Hz 0010: 64Hz 0011: 68.3Hz

0100: 73.1Hz 0101: 78.8Hz 0110: 85.3Hz 0111: 93.1Hz

1000: 102.4Hz 1001: 113.7Hz

pump_1/pump_2 control the regulator on duty cycle

00: 100%

01: 44%

10: 33%

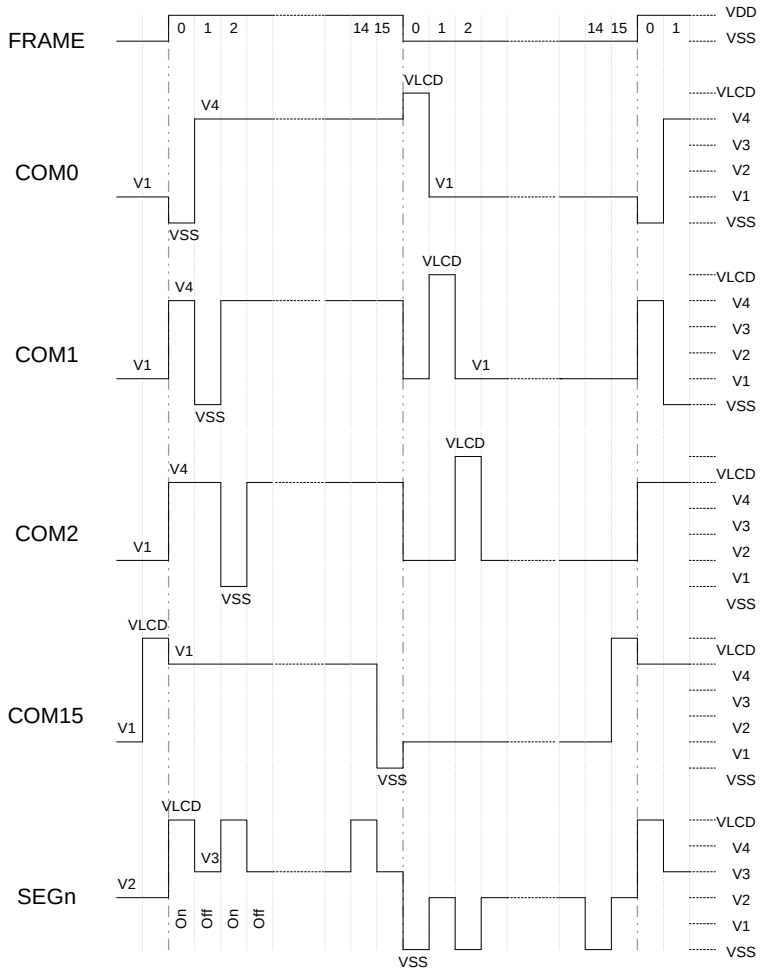
11: 57%

The smaller duty means smaller power consumption and weaker LCD driving ability.

There are 144 LCD data RAM in MLC852P. When the bit value of LCD data RAM is “1”, the corresponding LCD dot is turned on. When the bit value of LCD data RAM is “0”, the LCD dot is turned off. The contents of the LCD data RAM are sent out through the segment 0 to segment 69 pins by a direct memory access circuit. The relationship between the LCD data RAM and segment/common pins is shown below.

LCD Data RAM	Common	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1000H	COM 0	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1001H		SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
1002H		SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16
1003H		SEG31	SEG30	SEG29	SEG28	SEG27	SEG26	SEG25	SEG24
1004H		SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32
1005H		SEG47	SEG46	SEG45	SEG44	SEG43	SEG42	SEG41	SEG40
1006H		SEG55	SEG54	SEG53	SEG52	SEG51	SEG50	SEG49	SEG48
1007H		SEG63	SEG62	SEG61	SEG60	SEG59	SEG58	SEG57	SEG56
1008H		unused	unused	SEG69	SEG68	SEG67	SEG66	SEG65	SEG64
1010H	COM 1	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1011H		SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
1012H		SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16
1013H		SEG31	SEG30	SEG29	SEG28	SEG27	SEG26	SEG25	SEG24
1014H		SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32
1015H		SEG47	SEG46	SEG45	SEG44	SEG43	SEG42	SEG41	SEG40
1016H		SEG55	SEG54	SEG53	SEG52	SEG51	SEG50	SEG49	SEG48
1017H		SEG63	SEG62	SEG61	SEG60	SEG59	SEG58	SEG57	SEG56
1018H		unused	unused	SEG69	SEG68	SEG67	SEG66	SEG65	SEG64
…	…	…	…	…	…	…	…	…	…
10F0H	COM 15	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
10F1H		SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
10F2H		SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16
10F3H		SEG31	SEG30	SEG29	SEG28	SEG27	SEG26	SEG25	SEG24
10F4H		SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32
10F5H		SEG47	SEG46	SEG45	SEG44	SEG43	SEG42	SEG41	SEG40
10F6H		SEG55	SEG54	SEG53	SEG52	SEG51	SEG50	SEG49	SEG48
10F7H		SEG63	SEG62	SEG61	SEG60	SEG59	SEG58	SEG57	SEG56
10F8H		unused	unused	SEG69	SEG68	SEG67	SEG66	SEG65	SEG64

1/16 duty 1/5 bias



DAC/tone control

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1223H	AUD_CTL		CH0_MS		T_D	DAC_DRV1	DAC_DRV0	Tone_EN	DAC_EN	√	√

DAC_EN:

0 (default): DAC disabled

1: DAC enabled

Tone_EN:

0: (default) tone output disabled

1: tone enabled

DRV1	DRV0	DAC output drive current (V_{DD} = 3.0V)
0	0	1.90 mA (default)
0	1	2.60 mA
1	0	3.80 mA
1	1	5.00 mA

T_D

0 (default): pin SPK is tone output

1: pin SPK is DAC output

CH0_MS

0 (default): the channel 0 output is modulated by timer 0 underflow signal

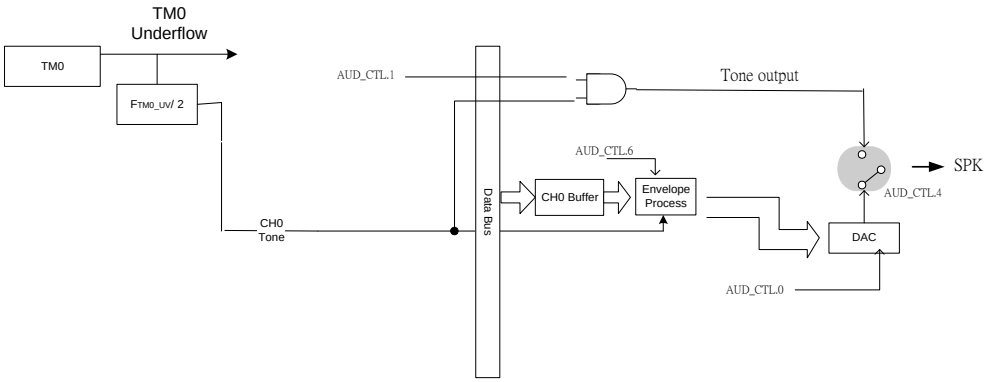
1: the channel 0 audio is not modulated

When the CH0_MS is '0', the timer0 underflow signal and the value of CH0 will be ended by hardware. When the CH0_MS is '1', the underflow signal will be replaced by VDD.

CH0 Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
1224H	CH0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	√	√

DAC data output buffer. When the data in CH0 is changed, the DAC output is changed immediately.

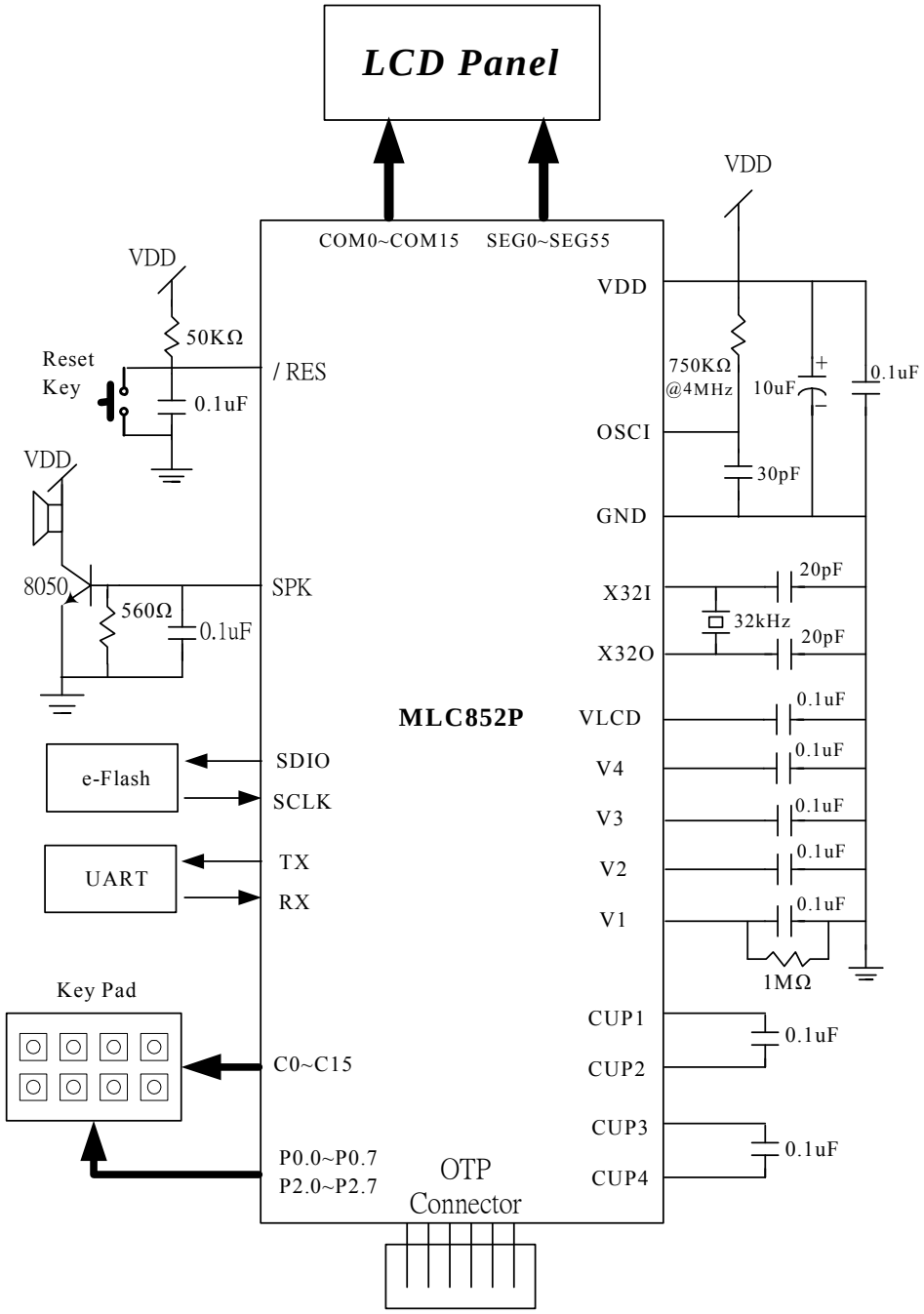


Programming Notice

The status after different reset condition is listed below:

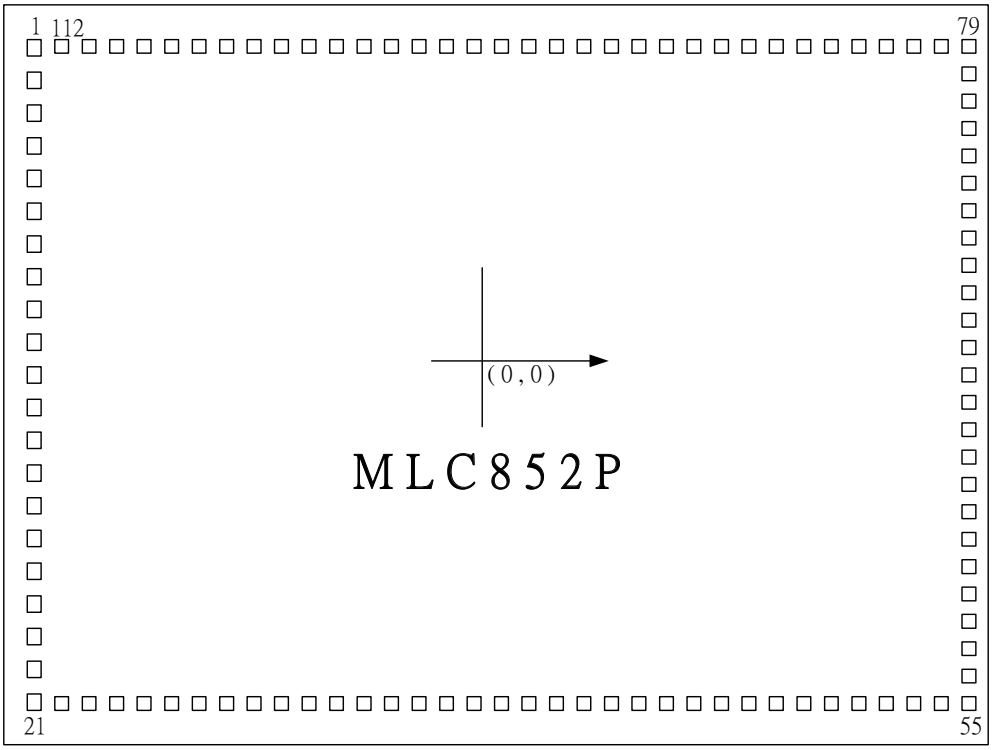
	Power on reset	CPU /RST pin reset
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

Application Circuit



Notes: Please pull VPP to Vss after finished OTP programming for better system ESD.

Pad Assignment



Pad	Name	Pad	Name	Pad	Name	Pad	Name
1	SEG8	29	CAP4	57	SEG60	85	SEG36
2	SEG7	30	V1	58	SEG59	86	SEG35
3	SEG6	31	V2	59	SEG58	87	SEG34
4	SEG5	32	V3	60	SEG57	88	SEG33
5	SEG4	33	V4	61	SEG56	89	SEG32
6	SEG3	34	VLCD	62	SEG55	90	SEG31
7	SEG2	35	VDD	63	SEG54	91	SEG30
8	SEG1	36	X32O	64	SEG53	92	SEG29
9	SEG0	37	X32I	65	SEG52	93	SEG28
10	COM15	38	RESB	66	SEG51	94	SEG27
11	COM14	39	OSCI	67	CMD	95	SEG26
12	COM13	40	VSS	68	SDA	96	SEG25
13	COM12	41	SPK	69	SCK	97	SEG24
14	COM11	42	P03	70	VPP	98	SEG23
15	COM10	43	P02	71	SEG50	99	SEG22
16	COM9	44	P01	72	SEG49	100	SEG21
17	COM8	45	P00	73	SEG48	101	SEG20
18	COM7	46	P11	74	SEG47	102	SEG19
19	COM6	47	P10	75	SEG46	103	SEG18
20	COM5	48	SEG69	76	SEG45	104	SEG17
21	COM4	49	SEG68	77	SEG44	105	SEG16
22	COM3	50	SEG67	78	SEG43	106	SEG15
23	COM2	51	SEG66	79	SEG42	107	SEG14
24	COM1	52	SEG65	80	SEG41	108	SEG13
25	COM0	53	SEG64	81	SEG40	109	SEG12
26	CAP1	54	SEG63	82	SEG39	110	SEG11
27	CAP2	55	SEG62	83	SEG38	111	SEG10
28	CAP3	56	SEG61	84	SEG37	112	SEG9

Note: 1. Substrate connected to ground

2. Bonding should start from VSS pin

Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +5.0	V
Applied Input / Output Voltage	-0.3 to +5.0	V
Power Dissipation	60	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Characteristics

(V_{DD}-V_{SS} = 3.0 V, F_{OSC} = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	-	2.4	-	5.5	V
Op. Current	I_{OP1}	Normal mode (Main clock: 4Mhz sub clock: 32768 Hz CPU clock: 1Mhz LCD on no load VDD = 3V)	-	1.3		mA
	I_{OP2}	Halt mode (Main clock: off Sub clock: 32768 Hz CPU off, 2Hz on LCD on no load VDD = 3V		25		uA
	I_{OP3}	Slow mode (Main clock: off Sub clock: 32768 Hz CPU off, 2Hz on LCD off, BLD on VDD = 3V)		6		uA
Standby Current	I_{STB}	Stop mode (No load)	-	1	3	μA
DAC output driving current	I_{DAC}	DAC_DRV = 00H	-	1.3	-	mA
		DAC_DRV = 01H	-	1.8	-	
		DAC_DRV = 02H	-	2.6	-	
		DAC_DRV = 03H	-	3.6	-	
Input High Voltage	V_{IH}	-	0.8 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.4	V
Battery-low Indicate Voltage	V_{BL1}	BL_CR.4=0, (BL_CR.3, BL_CR.2, BL_CR.1 = 111)		2.9		V
	V_{BL2}	BL_CR.4=1, (BL_CR.3, BL_CR.2, BL_CR.1 = 111)		4.35		
Port 0[3:0], P1 drive current	I_{OH}	V_{OH} = 2.4V, V_{DD} = 3.0V	-	1.8	-	mA
Port 0[3:0], P1 sink current	I_{OL0}	V_{OL} = 0.4V, V_{DD} = 3.0V	-	3.0	-	mA
Port 0[7:4], P2, P3 drive current	I_{OH}	V_{OH} = 2.4V, V_{DD} = 3.0V	-	1.8	-	mA
Port 0[7:4], P2, P3 sink current	I_{OL0}	V_{OL} = 0.4V, V_{DD} = 3.0V	-	1.5	-	mA
SEG0 ~ SEG69 drive current	I_{OH1}	V_{OH} = 2.4V, V_{LCD} = 3.0V	3	-	-	μA
SEG0 ~ SEG69 sink current	I_{OL1}	V_{OL} = 0.4V, V_{LCD} = 0.0V	1	-	-	mA
Internal Pull-high Resistor for ports	R_{PH1}	V_{IL} = 0V		50K		Ω
	R_{PH2}	V_{IL} = 0V		250K		

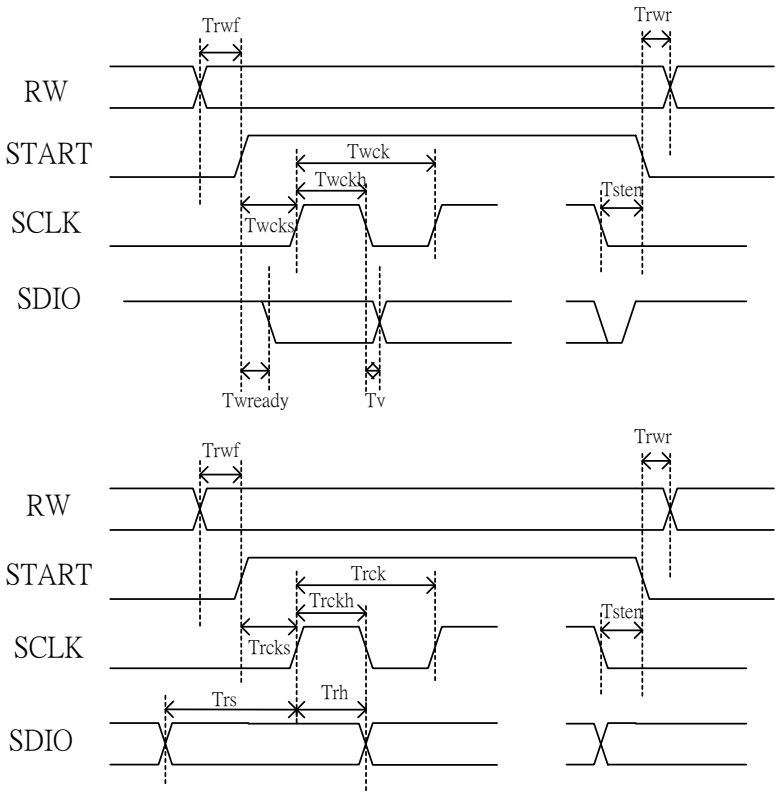
AC Characteristics

(Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CPU Op. Frequency	F_{CPU}	R=740kΩ, V_{DD} = 3.0V	-	3.4	-	MHz
Frequency Deviation by Voltage Drop for RC Oscillator	$\frac{\Delta f}{f}$	$\frac{f(4.5V) - f(2.4V)}{f(4.5V)}$	-	5	10	%
POR duration	T_{POR}	F_{OSC} = 1 MHz, Vdd=3.0V	10	15	50	mS

E_flash interface timing

Parameter	SYM.	Conditions	Min.	Typ..	Max.	Unit
RW ready to START high	Trwf		0			ns
START goes low to RW transition	Trwr		0			ns
SCLK write out clock period	Twck				250	ns
SCLK high period of each clock	Twckh		100		150	ns
START goes high to SCLK first goes high (write mode)	Twcks		125			ns
The first data ready time from START goes high	Twready				10	ns
Data valid time	Tv				10	ns
8^{th} clock goes low to start goes low	Tsten				10	ns
SCLK read in clock period	Trck			250		ns
START goes high to SCLK first goes high (read mode)	Trcks		125			ns
SCLK high period of each clock	Trckh		100		150	ns
Data setup time	Trs		10			ns
Data hold time	Trh		50			ns

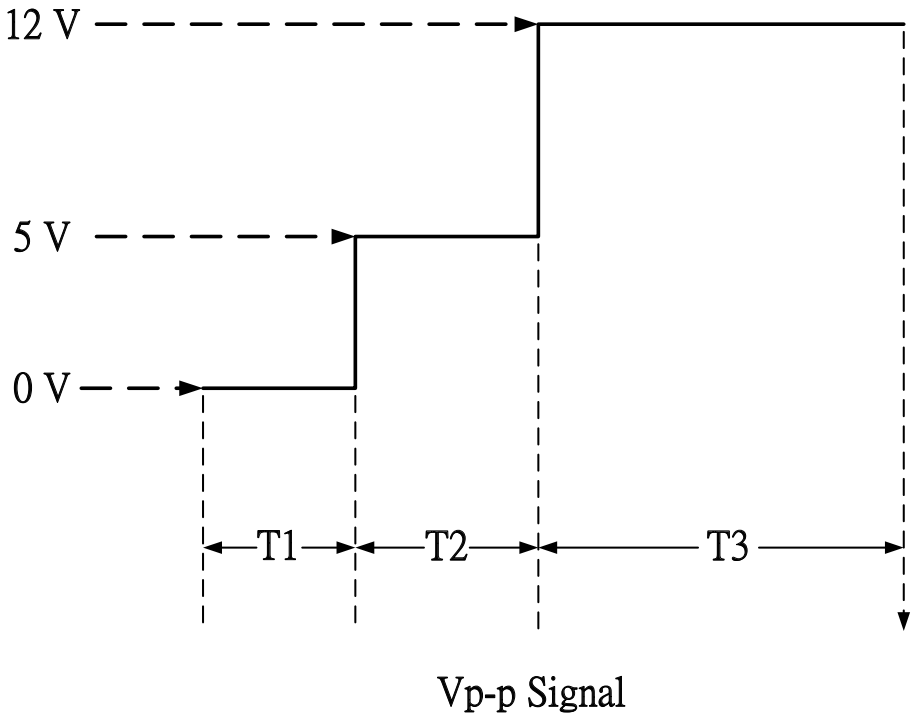


Notice:

1.SEG68/SEG67 == SDIO/SCLK == P3.0/P3.1

2.VPP Signal Explanation

The following diagram explains VPP signal.



Vp-p Signal

The voltage, waveform and timing requirments for VPP to program IC are as followed:

T1: Normal Operation timing.

T2: Reset Timing, and its purpose is to set the Address Counter of Interanl IC to zero.

T3: Duration time of programming.

Therefore, when program IC completes, VPP should be at GND state to ensure futher operations.

Version History

VERSION	DATE	PAGE	DESCRIPTION
0.2	Jul. 2007		Initial issue
0.3	Aug. 2007	P2,28,35	Modify VPP pin pull low circuit
0.4	Aug. 2007	P32	Revised DC Characteristics of LVD