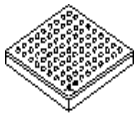
Freescale Semiconductor
Data Sheet: Advanced Information

Document Number: IMX50CEC
Rev. 0, 7/2011

RoHS

MCIMX50



Package Information
Plastic Package
Case MAPBGA 13 x 13 mm, 0.5 mm pitch
416 pin PBGA

Ordering Information
See Table 1 on page 7 for ordering information.

i.MX50 Applications Processors for Consumer Products

1 Introduction

The i.MX50 Applications Processors (i.MX50) represent Freescale Semiconductor's latest addition to a growing family of multimedia-focused products, offering high performance processing optimized for lowest power consumption.

The i.MX50 is optimized for portable multimedia applications and features Freescale's advanced implementation of the ARM Cortex-A8™ core, which operates at speed as high as 800 MHz. The i.MX50 provides a powerful display architecture, including a 2D Graphics Processing Unit (GPU) and Pixel Processing Pipeline (ePXP). In addition, i.MX508 includes a complete integration of the electrophoretic display function. The i.MX50 supports DDR2, LPDDR2, and LPDDR1 DRAM at clock rate up to 266 MHz to enable a range of performance and power trade-offs.

The flexibility of the i.MX50 architecture allows it to be used in a variety of applications. As the heart of the application chipset, the i.MX50 provides a rich set of interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, and displays.

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1.1 Product Overview

The i.MX50 is designed to enable high-tier portable applications by satisfying the performance requirements of advanced operating systems and applications.

1.1.1 Dynamic Performance Scaling

Freescale's dynamic voltage and frequency scaling (DVFS) allows the device to run at much lower voltage and frequency with ample processing capacity for tasks, such as audio decode, resulting in significant power reduction.

1.1.2 Multimedia Processing Powerhouse

The multimedia performance of the i.MX50 processor ARM Cortex-A8 core is boosted by a multi-level cache system, a NEON co-processor with SIMD media processing architecture and 32-bit single-precision floating point support, and two vector floating point co-processors. The system is further enhanced by a programmable smart DMA (SDMA) controller.

1.1.3 Powerful Display System

The i.MX50 includes support for both standard LCD displays as well as electrophoretic displays (e-paper). The display subsystem consists of the following modules:

- Electrophoretic Display Controller (EPDC) (i.MX508 only)

  The EPDC is a feature-rich, low power, and high-performance direct-drive active matrix EPD controller. It is specifically designed to drive E-INK^{TM} EPD panels, supporting a wide variety of TFT architectures. The goal of the EPDC is to provide an efficient SoC integration of this functionality for e-paper applications, allowing a significant bill of materials cost savings over an external solution while reaching much higher levels of performance and lower power. The EPDC module is defined in the context of an optimized hardware/software partitioning and works in conjunction with the ePXP (see Section 1.1.4, "Graphics Accelerators").
- Enhanced LCD Controller Interface (eLCDIF)

  The eLCDIF is a high-performance LCD controller interface that supports a rich set of modes and allows interoperability with a wide variety of LCD panels, including DOTCK/RGB and smart panels. The module also supports synchronous operation with the ePXP to allow the processed frames to be passed from the ePXP to the eLCDIF through an on-chip SRAM buffer. The eLCDIF can support up to 32-bit interfaces.

1.1.4 Graphics Accelerators

Integrated graphics accelerators offload processing from the ARM processor, enabling high performance graphic applications at minimum power.

- Pixel Processing Pipeline (ePXP)

  The ePXP is a high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma mapping, and

rotation. The ePXP is enhanced with features specifically for grayscale applications working in conjunction with the electrophoretic display controller to form a full grayscale display solution. In addition, the ePXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated LCD controller (eLCDIF).

- Graphics acceleration

  The i.MX50 provides a 2D graphics accelerator with performance up to 200 Mpix/s.

1.1.5 Multilevel Memory System

The multilevel memory system of the i.MX50 is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The i.MX50 supports many types of external memory devices, including DDR2, LPDDR2, LPDDR1, NOR Flash, PSRAM, Cellular RAM, NAND Flash (MLC and SLC) and OneNAND™, and managed NAND including eMMC up to rev 4.4.

1.1.6 Smart Speed™ Technology

The i.MX50 device has power management throughout the SOC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart Speed technology enables the designer to deliver a feature-rich product that requires levels of power that are far less than industry expectations.

1.1.7 Interface Flexibility

The i.MX50 supports connection to a variety of interfaces, including an LCD controller for displays, two high-speed USB on-the-go-capable PHYs, multiple expansion card ports (high-speed MMC/SDIO host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (for example, UART, I^2C, and I^2S serial audio).

1.1.8 Advanced Security

The i.MX50 delivers hardware-enabled security features, such as High-Assurance Boot 4 (HAB4) for signed/authenticated firmware images, basic DRM support with random private keys and AES encryption/decryption, and storage and programmability of on-chip fuses.

1.2 Features

The i.MX50 Application Processor (AP) is based on ARM Cortex-A8 platform and has the following features:

- MMU, L1 instruction cache, and L1 data cache
- Unified L2 cache
- 800 MHz target frequency of the core (including NEON, VFPv3, and L1 cache)
- NEON coprocessor (SIMD Media Processing Architecture) and Vector Floating Point (VFP-Lite) coprocessor supporting VFPv3

The memory system consists of the following components:

- Level 1 cache:
  - Instruction (32 Kbyte)
  - Data (32 Kbyte)
- Level 2 cache:
  - Unified instruction and data (256 Kbyte)
- Level 2 (internal) memory:
  - Boot ROM, including HAB (96 Kbyte)
  - Internal multimedia/shared, fast access RAM (128 Kbyte)
- External memory interfaces:
  - 16/32-bit DDR2-533, LPDDR2-533, or LPDDR1-400 up to a total of 2 GByte
  - 8-bit NAND SLC/MLC Flash with up to 100 MHz synchronous clock rate and up to 32-bit hardware ECC for 1 Kbyte block size
  - 16/32-bit NOR Flash with a dedicated 16-bit muxed-mode interface. I/O muxing logic selects EIMv2 port as primary muxing at system boot.
  - 16-bit PSRAM, Cellular RAM
  - Managed NAND, including eMMC up to rev 4.4

The i.MX50 introduces a next generation system bus fabric architecture that aggregates various sub-system buses and masters for access to system peripherals and memories. The various bus-systems and components are as follows:

- 64-bit AXI Fabric (266 MHz)—This bus-fabric is the SoC's central bus aggregation point.
  - Provides access to all slave targets in the SoC:
    - ROM (ROMCP)
    - On-chip RAM (OCRAM)
    - External DRAM (DRAM MC)
    - External static RAM (EIM)
    - Interrupt controller (TZIC)
    - Decode into the AHB MAX crossbar second level AHB fabric.
  - Provides arbitration to the following masters in the system:
    - ARM CPU complex
    - Pixel processing pipeline (ePXP)
    - Electrophoretic display controller (EPDC)
    - eLCDIF LCD display controller
    - DCP Crypto engine
    - BCH ECC engine
    - MAX AHB crossbar
    - GPU 2D
    - SDMA

  - USBOH1 (USB OTG and host controller complex)
  - FEC Ethernet controller
- MAX AHB crossbar (133 MHz)—This connects the various AHB bus sub-segments in the system and provides decode into the following slaves:
  - IP-Bus 1 (66 MHz)—This bus segment contains peripherals accessible by the ARM core and without DMA capability
  - IP-Bus 2 (66 MHz)—This bus segment contains peripherals accessible by the ARM core and without DMA capability
  - APBH DMA bridge (133 MHz)—The APBH DMA bridge is a master to the MAX for its memory-side DMA operations. The APBH bus is an AMBA APB slave bus providing peripheral access to many of the high-speed IP blocks on the i.MX50.
- IP-Bus 3 (66 MHz)—This third peripheral bus segment contains peripherals accessible by the ARM core and SDMA and as such houses peripherals with DMA capability. The IP-Bus 3 can be accessed by the ARM CPU through IP-Bus 1 and SPBA.
- Quality of service controller (QoSC)—This provides both soft and dynamic arbitration/priority control. The QoSC works in conjunction with the critical display modules such as the eLCDIF and EPDC to provide dynamic priority control, based on real-time metrics.

The i.MX50 makes use of dedicated hardware accelerators to achieve state-of-the-art multimedia performance. The use of hardware accelerators provides both high performance and low power consumption, while freeing up the CPU core for other tasks.

The i.MX50 incorporates the following hardware accelerators:

- GPU2Dv1—2D Graphics accelerator, OpenVG 1.1, 200 Mpix/s performance
- ePXP—enhanced PiXel Processing Pipeline off loading key pixel processing operations required to support both LCD and EPD display applications

The i.MX50 includes the following interfaces to external devices:

NOTE

Not all the interfaces are available simultaneously depending on I/O multiplexer configuration.

- Displays:
  - EPDC (i.MX508 Only)—Supporting direct-driver TFT backplanes beyond 2048 × 1536 at 106 Hz refresh (or 4096 × 4096 at 20 Hz)
  - eLCDIF—Supporting beyond SXGA + (1400 × 1050) at 60 Hz resolutions with up to a 32-bit display interface
  - On the i.MX508, both displays can be active simultaneously. If both displays are active, the eLCDIF only provides a 16-bit interface due to pin muxing.
- Expansion cards:
  - Four SD/MMC card
- USB:
  - One High Speed (HS) USB 2.0 OTG-capable port with integrated HS USB PHY

  - One High Speed (HS) USB 2.0 host port with integrated HS USB PHY
- Miscellaneous interfaces:
  - One-wire (OWIRE) port
  - Two I2S/SSI/AC97 ports, supporting up to 1.4 Mbps each connected to the Audio Multiplexer (AUDMUX) providing four external ports
  - Five UART RS232 ports, up to 4.0 Mbps each
  - Two eCSPI (Enhanced CSPI) ports, up to 66 Mbps each plus CSPI port, up to 16.6 Mbps
  - Three I^2C ports, supporting 400 kbps
  - Fast Ethernet controller IEEE 802.3, 10/100 Mbps
  - Key pad port (KPP)
  - Two pulse width modulators (PWM)
  - GPIO with interrupt capabilities
  - Secure JTAG controller (SJC)

The system supports efficient and smart power control and clocking:

- Supporting DVFS techniques for low power modes, including auto slow architecture
- Power gating-SRPG (state retention power gating) for ARM core and NEON
- Support for various levels of system power modes
- Flexible clock gating control scheme
- On-chip temperature monitor
- On-chip 32 kHz and 24 MHz oscillators
- A total of four PLLs with the fourth PLL providing up to eight independently controllable outputs, improving the ease of clocking control, especially for display and connectivity modules

Security functions are enabled and accelerated by the following hardware:

- Secure JTAG controller (SJC)—Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features
- Secure real-time clock (SRTC)—Tamper resistant RTC with dedicated power domain and mechanism to detect voltage and clock glitches
- Advanced high assurance boot (A-HAB)—HAB with the next embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization

1.3 Ordering Information

Table 1 provides the ordering information.

Table 1. Ordering Information

Part Number	Mask Set	Features	Ambient Temperature Range (°C)	Package[1]
MCIMX508CVK8B	N78A	Full Specification	0 to 70	13 x 13 mm, 0.5 mm pitch BGA Case: 416MAPBGA
MCIMX508CVM8B	N78A	Full Specification	0 to 70	17 x 17 mm, 0.8 mm pitch BGA Case: 400MAPBGA
MCIMX507CVM8B	N78A	No GPU	0 to 70	17 x 17 mm, 0.8 mm pitch BGA, Case: 400MAPBGA
MCIMX503CVM8B	N78A	No EPD controller	0 to 70	17 x 17 mm, 0.8 mm pitch BGA Case: 400MAPBGA
MCIMX502CVM8B	N78A	No GPU, no EPD controller	0 to 70	17 x 17 mm, 0.8 mm pitch BGA, Case: 400MAPBGA

1 Case MAPBGA is RoHS compliant, lead-free MSL (Moisture Sensitivity Level) 3.

1.4 Part Number Feature Comparison

Table 2 provides an overview of the feature differences between the i.MX50 part numbers.

Table 2. Part Number Feature Comparison

Part Number	Disabled Features	Comments
MCIMX508	None	
MCIMX507	GPU	
MCIMX503	EPDC	The i.MX503 has the same ballmap and IOMUX as the i.MX508. The EPDC pins still exist on the i.MX503, but because the EPDC block is disabled, those pins cannot be used for EPDC functionality (ALT0) and must be configured in the IOMUX with another ALT-mode setting.
MCIMX502	GPU, EPDC	The i.MX502 has the same ballmap and IOMUX as the i.MX508. The EPDC pins still exist on the i.MX502, but because the EPDC block is disabled, those pins cannot be used for EPDC functionality (ALT0) and must be configured in the IOMUX with another ALT-mode setting.

1.5 Package Feature Comparison

Table 3 provides an overview of the feature and pin differences between the i.MX50 packages.

Table 3. Package Feature Comparison

Package	Dimensions	I/O Pin Differences Versus 416MAPBGA	Notes on Package Differences
416MAPBGA	13 x 13 mm, 0.5 mm pitch	—	• USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the 416MAPBGA package substrate. • USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the 416MAPBGA package substrate.
400MAPBGA	17 x 17 mm, 0.8 mm pitch	**Deleted Pins:** DRAM_SDCLK_1 DRAM_SDCLK_1_B DRAM_A14 DRAM_SDODT1 UART2_CTS UART2_RTS	• USB_OTG_VDDA25 and USB_H1_VDDA25 are independent and NOT shorted together on the 400MAPBGA package substrate. • USB_OTG_VDDA33 and USB_H1_VDDA33 are independent and NOT shorted together on the 400MAPBGA package substrate.

2 Architectural Overview

The following sections provide an architectural overview of the i.MX50 processor system.

2.1 Block Diagram

Figure 1 shows the functional modules in the i.MX50 processor system.

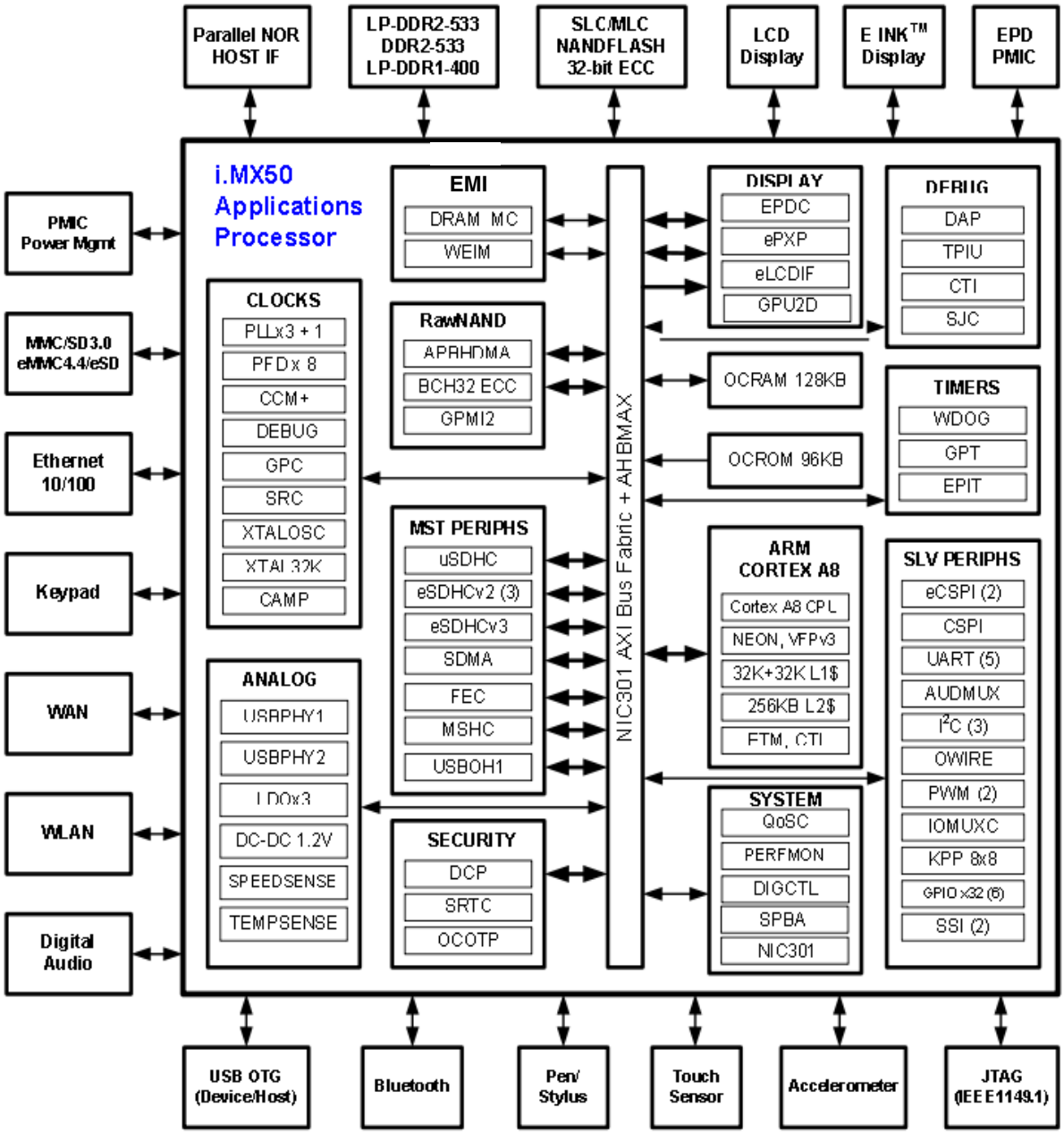


Figure 1. i.MX50 System Block Diagram

NOTE

The numbers in brackets indicate the number of module instances. For example, PWM (2) indicates two separate PWM peripherals.

3 Modules List

The i.MX50 processor contains a variety of digital and analog modules that are described in Table 4 in alphabetical order.

Table 4. i.MX50 Digital and Analog Modules

Block Mnemonic	Block Name	Subsystem	Brief Description
ARM Cortex-A8	ARM Cortex-A8 Platform	ARM	The ARM Cortex-A8 Core Platform consists of the ARM Cortex-A8 processor and its essential sub-blocks. It contains the 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, Level 2 cache controller and a 256 Kbyte L2 cache. The platform also contains an event monitor and debug modules. It also has a NEON co-processor with SIMD media processing architecture, register file with 32 × 64-bit general-purpose registers, an Integer execute pipeline (ALU, Shift, MAC), dual, single-precision floating point execute pipeline (FADD, FMUL), load/store and permute pipeline, and a non-pipelined vector floating point (VFP Lite) co-processor supporting VFPv3.
EPDC	Electrophoretic Display Controller	Display Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive active matrix EPD controller. It is specifically designed to drive E-INK™ EPD panels supporting a wide variety of TFT backplanes.
ePXP	enhanced PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations such as color-space conversion, alpha blending, gamma-mapping, and rotation. The ePXP is enhanced with features specifically for grayscale applications. In addition, the ePXP supports traditional pixel/frame processing paths for still-image and video processing applications allowing it to interface with the integrated LCD controller (eLCDIF).
eLCDIF	enhanced LCD Interface	Display Peripherals	The eLCDIF is a high-performance LCD controller interface supporting a rich set of modes allowing inter operability with a wide variety of LCD panels, including DOTCK/RGB and smart panels. The module also supports a synchronous operation with the ePXP to allow the processed frames to be passed from the ePXP to the eLCDIF through an on-chip SRAM buffer. The eLCDIF can support up to 32-bit interfaces.
AUDMUX	Digital Audio Mux	Slave Connectivity Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1 and SSI2) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has six ports (two internal and four external) with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CAMP-1	Clock Amplifier	Clocks, Resets, and Power Control	Clock Amplifier

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CCM GPC SRC	Clock Control Module Global Power Controller System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for system power management. The system includes four PLLs.
CSPI eCSPI-1 eCSPI-2	Configurable SPI, Enhanced CSPI	Slave Connectivity Peripherals	Full-duplex enhanced synchronous serial interface, with data rate up to 66.5 Mbit/s (for eCSPI, master mode). It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
DAP TPIU CTI	Debug System	System Control Peripherals	The Debug System provides real-time trace debug capability of both instructions and data. It supports a trace protocol that is an integral part of the ARM Real Time Debug solution (RealView). Real-time tracing is controlled by specifying a set of triggering and filtering resources, which include address and data comparators, three cross-system triggers (CTI), counters, and sequencers. Debug access port (DAP)—The DAP provides real-time access for the debugger without halting the core to System memory and peripheral registers. All debug configuration registers and Debugger access to JTAG scan chains.
DRAM MC	DRAM Memory Controller	External Memory Interface	The DRAM MC consists of a DRAM memory controller and PHY, supporting LPDDR2, DDR2, and LPDDR1 memories with clock frequencies up to 266 MHz with 32-bit interface. It is tightly linked with the system bus fabric and employs advanced arbitration mechanism to maximize DRAM bandwidth efficiency.
EIM	Static Memory Controller	External Memory Interface	The EIM is an external static memory and generic host interface. It supports up to a 32-bit interface (through pin-muxing) or a dedicated 16-bit muxed interface. It can be used to interface to PSRAMs (sync and async), NOR-flash or any external memory mapped peripheral.
BCH32/GPMI2	Raw NAND System with ECC	RawNAND and SSP Peripherals	The i.MX50 contains a fully hardware accelerated raw NAND flash solution supporting SLC and MLC devices. The system consists of the GPMI2 module, which is driven by the APBH DMA engine to perform the NAND flash interface function (supporting up to ONFI2.1). Coupled with the GPMI2 is the BCH32 hardware error-correction engine which is an AXI bus-master and supports up to 32-bits of correction over block sizes up to 1 Kbyte (that is, supports up to 2 Kbyte code-size).
System Fabric and QoS	System Fabric and QoS	System Peripherals	In order to aggregate the multitude of masters and memory mapped devices, the i.MX50 contains a next-generation AMBA3 AXI bus fabric. In addition, the i.MX50 contains a Quality of Service Controller IP (QoSC) which allows both soft priority control and dynamic priority elevation. Software priority control works for all masters but dynamic hardware control only works for EPDC and eLCDIF.
EPIT	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit *set and forget* timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eSDHCv3-3 (eMMC 4.4)	Ultra-High-Speed Multi-Media Card/ Secure Digital card host controller, ver. 3	Master Connectivity Peripherals	Ultra High-Speed eSDHC, enhanced to support eMMC 4.4 standard specification, for 832 Mbps. IP is backward compatible to eSDHCv2 IP. See complete features listing in eSDHCv2 entry below. Port 3 is specifically enhanced to support eMMC 4.4 specification, for double data rate (832 Mbps, 8-bit port).
eSDHCv2-1 eSDHCv2-2 eSDHCv2-4	Enhanced Multi-Media Card/ Secure Digital Host Controller, ver. 2		In Enhanced Multi-Media Card/Secure Digital Host Controller the Ports 1, 2, and 4 are compatible with the *MMC System Specification* version 4.3, full support The generic features of the eSDHCv2 module, when serving as SD/MMC host, include the following: • Can be configured either as SD/MMC controller • Supports eSD and eMMC standard, for SD/MMC embedded type cards • Conforms to *SD Host Controller Standard Specification* version 2.0, full support • Compatible with the SD Memory Card Specification version 1.1 • Compatible with the SDIO Card Specification version 1.2 • Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full/High speed mode • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416 Mbps data transfer for MMC cards using eight parallel data lines
FEC	Fast Ethernet Controller	Master Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support both 10 Mbps and 100 Mbps Ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6	General Purpose I/O Modules	Slave Connectivity Peripherals	These modules are used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit *free-running* or *set* and *forget* mode timer with a programmable prescaler and compare and capture register. A timer counter value can be captured using an external event, and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPU2Dv1	Graphics Processing Unit-2D, ver. 1	Display Peripherals	The GPU2Dv1 provides hardware acceleration for 2D graphic algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD1080 resolution.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provides serial interface for controlling peripheral devices. Data rates of up to 400 kbps are supported.
OCOTP Controller	On-chip OTP controller	Security Peripherals	The on-chip one-time -programmable (OCOTP) ROM serves the functions of hardware and software capability bits, Freescale operations and unique-ID, the customer-programmable cryptography key, and storage of various ROM and general purpose configuration bits.
IOMUXC	IOMUX Control	Slave Connectivity Peripherals	This module enables flexible I/O multiplexing. Each I/O pad has default as well as several alternate functions. The alternate functions are software configurable.
KPP	Keypad Port	Slave Connectivity Peripherals	The KPP supports an 8 × 8 external keypad matrix. The KPP features are as follows: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
OWIRE	One-Wire Interface	Slave Connectivity Peripherals	One-Wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example, Dallas DS2502.
PWM-1 PWM-2	Pulse Width Modulation	Slave Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4 x 16 data FIFO to generate sound.
RAM 128 Kbytes	Internal RAM	Internal Memory	The On-Chip Memory controller (OCRAM) module, is an interface between the system's AXI bus, to the internal (on-chip) SRAM memory module. It is used for controlling the 128 Kbyte multimedia RAM, through a 64-bit AXI bus.
ROM 96 Kbytes	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. The ROM Controller supports ROM Patching.

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	Master Connectivity Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by offloading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM Cortex-A8 and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle uni-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMI • Support of byte-swapping and CRC calculations • A library of scripts and API is available
SJC	Secure JTAG Controller	System Control Peripherals	The Secure JTAG Controller provides a mechanism for regulating JTAG access, preventing unauthorized JTAG usage while allowing JTAG access for manufacturing tests and software debugging. The i.MX50 JTAG port provides debug access to several hardware blocks including the ARM processor and the system bus, therefore, it must be accessible for initial laboratory bring-up, manufacturing tests and troubleshooting, and for software debugging by authorized entities. However, if the JTAG port is left unsecured it provides a method for executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The Secure JTAG controller provides three different security modes that can be selected through an e-fuse configuration to prevent unauthorized JTAG access.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (Shared Peripheral Bus Arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SRTC	Secure Real Time Clock	Security Peripherals	The SRTC incorporates a special System State Retention Register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC. The NVCC_SRTC can be energized separately even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR marks the event (security violation indication).

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2	I2S/SSI/AC97 Interface	Slave Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX50 processor to provide connectivity with off-chip audio peripherals. The SSI interfaces connect internally to the AUDMUX for mapping to external ports. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8 x 24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two time slots are being used simultaneously.
Temperature Monitor	Temp Sensor	Analog	The temperature sensor is an internal module to the i.MX50 that monitors the die temperature.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface, ver. 2	Slave Connectivity Peripherals	Each of the UARTv2 modules supports the following serial data transmit/receive protocols and configurations: • 7 or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable bit-rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 Mbps, which is specified by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps)
USB-OH-1	USB 2.0 High-Speed OTG-capable and Host ports	Master Connectivity Peripherals	USB-OH-1 supports USB2.0 HS/FS/LS, and contains: • One high-speed OTG-capable module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY
WDOG-1	Watch Dog	Timer Peripherals	The Watchdog (WDOG) timer module protects against system failures by providing a method of escaping from unexpected events or programming errors. The WDOG Timer supports two comparison points during each counting period. Each of the comparison points is configurable to invoke an interrupt to the ARM core, and a second point invokes an external event on the WDOG line.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module combined with an external 24 MHz crystal with load capacitors implements a crystal oscillator.

3.1 Special Signal Considerations

Table 5 lists special signal considerations for the i.MX50. The signal names are listed in alphabetical order. The package contact assignments are found in Section 5, "Package Information and Contact Assignments." The signal descriptions are defined in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM).

Table 5. Special Signal Considerations

Signal Name	Remarks
BOOT_MODE0, BOOT_MODE1	These two input pins are sampled out of reset and set the boot mode. For Internal boot, they should be set to 00. For Internal Fuse Only boot, they should be set to 10. For USB downloader, they should be set to 11. The BOOTMODE pins are in the NVCC_RESET domain and include an internal 100K pull-up resistor at start-up.
BOOT_CONFIG1[7:0], BOOT_CONFIG2[7:0], BOOT_CONFIG3[7:0]	These 24 pins are the GPIO boot override pins and may be driven at power up to select the boot mode. They are sampled 4 x CKIL clock cycles after POR is de-asserted. Consult the "System Boot" chapter of the Reference Manual for more details. Note that these are not dedicated pins: the BOOT_CONFIG pins appear over 24 pins of the EIM interface.
BT_LPB_FREQ[1:0]	If the LOW_BATT_GPIO (UART4_TXD) is asserted at power up, the BT_LPB_FREQ[1:0] pins will be sampled to determine the ARM core frequency. Consult the "System Boot" chapter of the Reference Manual for more details. Note that these are not dedicated pins: BT_LPB_FREQ0 appears on SSI_TXFS and BT_LPB_FREQ1 appears on SSI_TXC.
CHRG_DET_B	This is the USB Charger Detect pin. It is an open drain output pin that expects a 100 K pull-up. This pin is asserted low when a USB charger is detected on the OTG PHY DP and DM. This detection occurs with the application of VBUS. This pin is a raw sensor output and care must be taken to follow the system timings outlined in the USB charger specification Rev 1.1. This pin can be controlled by software control as well. If not used, this pin should be tied to ground or left floating.
CKIH	This is an input to the CAMPs (Clock Amplifiers), which include on-chip AC-coupling precluding the need for external coupling capacitors. The CAMPs are enabled by default, but the main clocks feeding the on-chip clock tree are sourced from XTAL/EXTAL by default. Optionally, the use of a low jitter external oscillators to feed CKIH (while not required) can be an advantage if low jitter or special frequency clock sources are required by modules sourced by CKIH. See CCM chapter in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for details on the respective clock trees. After initialization, the CAMPs may be disabled if not used by programming the CCR CAMPx_EN field. If disabled, the on-chip CAMP output is low and the input is irrelevant. CKIH is on the NVCC_JTAG power domain, so the input clock amplitude should not exceed NVCC_JTAG. If unused, the user should tie CKIH to GND for best practice.
CKIL/ECKIL	The user must tie a fundamental mode 32.768 K crystal across ECKIL and CKIL. The target ESR should be 50 K or less. The bias resistor for the amplifier is integrated and approximately 14 MΩ. The target load capacitance for the crystal is approximately 10 pF. The load capacitors on the board should be slightly less than double this value after taking parasitics into account. While driving in an external 32 KHz signal into ECKIL, CKIL should be left floating so that it biases. A differential amplifier senses these two pins to propagate the clock inside the i.MX508. Care must be taken to minimize external leakages on ECKIL and CKIL. If they are significant to the 14 MΩ feedback or 1 μA, then loss of oscillation margin or cessation of oscillation may result.

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
DRAM_OPEN, DRAM_OPENFB (416MAPBGA and 400MAPBGA Only)	These pins are the echo gating output and feedback pins used by the DRAM PHY to bound a window around the DQS transition. For an application using a single DRAM device, these pins should be routed so that the trace length (DRAM_OPEN + DRAM_OPENFB) = trace length (DRAM_SDCLK0 + DRAM_SDQS0). For an application using two DRAM devices, they should be routed so that the trace length (DRAM_OPEN + DRAM_OPENFB) = trace length (AVG(DRAM_SDCLK0+DRAM_SDCLK1) + AVG (DRAM_SDQS0_to_Device0 + DRAM_SDQS0_to_Device1)). This connection is required for mDDR, LPDDR2, and DDR2.
DRAM_SDODT0, DRAM_SDODT1 (416MAPBGA and 400MAPBGA Only)	These pins are the On-die termination outputs from the i.MX50. For DDR2, these pins should be connected to the DDR2 DRAM ODT pins. For LPDDR2 and mDDR, these pins should be left floating. Only SDODT0 exists on the 400MAPBGA package.
DRAM_CALIBRATION	This pin is the ZQ calibration used to calibrate DRAM Ron and ODT. For LPDDR2, this pin should be connected to ground through a 240 Ω 1% resistor. For DDR2 and LPDDR1, this pin should be connected to ground through a 300 Ω 1% resistor.
JTAG_MOD	This input has an internal 100K pull-down. Note that JTAG_MOD is referenced as SJC_MOD in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) - both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed.
JTAG_TCK	This input has an internal 100K pull-down. This pin is in the NVCC_JTAG domain.
JTAG_TDI	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
JTAG_TDO	This is a 3-state output with an internal gate keeper enable to prevent a floating condition. An external pull-up or pull-down resistor on JTAG_TDO is detrimental and should be avoided. This pin is in the NVCC_JTAG domain.
JTAG_TMS	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
JTAG_TRSTB	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
NC	These signals are No Connect (NC) and should be floated by the user.
LOW_BATT_GPIO	If the LOW_BATT_GPIO (UART4_TXD) is asserted at power up, the i.MX50 will boot up at a lower ARM clock frequency to reduce system power. The actual ARM clock frequency used when LOW_BATT_GPIO is asserted is determined by the BT_LPB_FREQ[1:0] pins (220 MHz to 55.3 MHz). The polarity of the LOW_BATT_GPIO is active high by default, but may be set to active low by setting the LOW_BATT_GPIO_LEVEL OTP bit. See the “System Boot” chapter of the Reference Manual for more details. Note that this is not a dedicated pin: LOW_BATT_GPIO appears on the UART4_TXD pin.
PMIC_STBY_REQ	This output may be driven high when the i.MX50 enters the STOP mode to notify the PMIC to enter its low power standby state. This output is in the NVCC_SRTC domain.
PMIC_ON_REQ	This output from the i.MX50 can instruct the PMIC to turn on when the i.MX50 only has NVCC_SRTC power. This may be useful for an alarm application, as it allows the i.MX50 to turn off all blocks except for the RTC and then power on again at a specified time. This output is in the NVCC_SRTC domain.
PMIC_RDY	This input may be used by a PMIC to signal to the i.MX50 that the PMIC supply outputs are at operating levels when resuming from STOP mode. The PMIC_RDY input is pinmuxed on ALT3 of the I2C3_SCL pin and is in the NVCC_MISC domain.

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
POR_B	This POWER-ON RESET input is a cold reset negative logic input that resets all modules and logic in the IC. The POR_B pin should have an external 68 K pull-up to NVCC_RESET and a 1 μF capacitor to ground. **Note:** The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.
RESET_IN_B	This warm reset negative logic input resets all modules and logic except for the following: • Test logic (JTAG, IOMUXC, DAP) • SRTC • Cold reset logic of WDOG—Some WDOG logic is only reset by POR_B. See WDOG chapter in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for details.
SSI_EXT1_CLK, SSI_EXT2_CLK	The SSI_EXT1_CLK and SSI_EXT2_CLK outputs are recommended for generating a clock output from the i.MX50. Use of the CKO1 and CKO2 clock outputs is not recommended, as the large number of combinational logic muxes on those signals will impact jitter and duty-cycle. Note that these two clock outputs do not have dedicated pins: SSI_EXT1_CLK is IOMUX ALT3 on the OWIRE pin, and SSI_EXT2_CLK is IOMUX ALT3 of the EPITO pin.
TEST_MODE	TEST_MODE is for Freescale factory use only. This signal is internally connected to an on-chip pull-down device. The user must either float this signal or tie it to GND.
USB_H1_GPANAIO, USB_OTG_GPANAIO	These signals are reserved for Freescale manufacturing use only. Users should float these outputs.
USB_H1_RREFEXT, USB_OTG_RREFEXT	These signals determine the reference current for the USB PHY bandgap reference. An external 6.04 kΩ 1% resistor to GND is required. This resistor should be connected through a short (low impedance connection) and placed away from other noisy regions. If USB_H1 is not used, the H1 RREFEXT resistor may be eliminated and the pin left floating. If USB_OTG is not used, the OTG RREFEXT resistor may be eliminated and the pin left floating.
USB_H1_VBUS, USB_OTG_VBUS	These inputs are used by the i.MX50 to detect the presence and level of USB 5 V. If either VBUS input pin is connected to an external USB connector, there is a possibility that a fast 5 V edge rate during a cable attach could trigger the VBUS input ESD protection, which could result in damage to the i.MX50 silicon. To prevent this, the system should use some circuitry to prevent the 5 V edge rate from exceeding 5.25 V / 1 μs. Freescale recommends the use of a low pass filter consisting of 100 Ω resistor in series and a 1 μF capacitor close to the i.MX50 pin. In the case when the USB interface is connected on an on-board USB device (for example, 3G modem), the corresponding USB_VBUS pin may be left floating.
VREF	This pin is the DRAM MC reference voltage input. For LPDDR2 and DDR2, this pin should be connected to ½ of NVCC_EMI_DRAM. For mDDR, this pin should be left floating. The user may generate VREF using a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 μF capacitor.
WDOG_B	This output can be used to reset the system PMIC when the i.MX50 processor is locked up. This output is in the NVCC_MISC domain.

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
WDOG_RST_B_DEB	This output may be used to drive out the internal system reset signal to the system reset controller. This is only intended for debug purposes.
XTAL/EXTAL	These pins are the 24 MHz crystal driver as well as the external 24 MHz clock input. If using these pins to directly drive a 24 MHz crystal: • The user should tie a 24 MHz fundamental-mode crystal across XTAL and EXTAL. • The crystal must be rated for a maximum drive level of 100 μW or higher. • The recommended crystal ESR (equivalent series resistance) is 80 Ω or less. If using these pins as a clock input from an external 24 MHz oscillator: • The crystal may be eliminated and EXTAL driven directly driven by the external oscillator. The clock signal level on EXTAL must swing from NVCC_SRTC to GND. • In this configuration, the XTAL pin must be floated and the COSC_EN bit (bit 12 in the CCR register in the Clock Control Module) must be cleared to put the on-chip oscillator circuit in bypass mode which allows EXTAL to be externally driven. • Note there are strict jitter requirements if using an external oscillator in a USB application: < 50 ps peak-to-peak below 1.2 MHz and < 100 ps peak-to-peak above 1.2 MHz for the USB PHY.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics of the i.MX50 processor.

NOTE

These electrical specifications are preliminary. These specifications are not fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications are published after thorough characterization and device qualifications have been completed.

4.1 Chip-Level Conditions

This section provides the chip-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX50 Chip-Level Conditions

For these characteristics, see	Topic appears …
Table 7, “Absolute Maximum Ratings”	on page 20
Table 8, “Thermal Resistance Data”	on page 20
Table 9, “i.MX50 Operating Ranges”	on page 21
Table 10, “Interface Frequency”	on page 22

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Table 9 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Peripheral core supply voltage	VCC	–0.3	1.5	V
ARM core supply voltage	VDDGP	–0.3	1.35	V
Bandgap and 480 MHz PLL supply	VDD3P0	–0.5	3.6	V
PLL digital supplies	VDD1P2	–0.3	1.35	V
PLL analog supplies	VDD1P8	–0.3	2.25	V
Efuse, 24 MHz oscillator, 32 kHz oscillator mux supply	VDD2P5	–0.5	2.85	V
Memory array supply	VDDA/VDDAL1	–0.5	1.35	V
Supply voltage (HVIO)	Supplies denoted as I/O supply	–0.5	3.6	V
Supply voltage (GPIO, LVIO)	Supplies denoted as I/O supply	–0.5	3.3	V
Input/output voltage range	V_{in}/V_{out}	–0.5	OVDD + 0.3[1]	V
USB VBUS DC Transient (t<30ms, duty cycle < 0.05%)	VBUS	 — —	 6.00 7.00	V
ESD damage immunity: Human Body Model (HBM) Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	–40	125	°C

[1] The term OVDD in this section refers to the associated supply rail of an input or output. The maximum range can be superseded by the DC tables.

4.1.2 Thermal Resistance

Table 8 provides the thermal resistance data.

Table 8. Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to case[1], 13 × 13 mm package	—	$R_{\theta JC}$	6	°C/W

[1] Rjc-x per JEDEC 51-12: The junction-to-case thermal resistance. The x indicates the case surface where T_{case} is measured and through which 100% of the junction power is forced to flow due to the cold plate heat sink fixture placed either at the top (T) or bottom (B) of the package, with no board attached to the package.

4.1.3 Operating Ranges

Table 9 provides the operating ranges of the i.MX50 processor.

Table 9. i.MX50 Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP	ARM core supply voltage 400 < f_{ARM} ≤ 800 MHz	0.95	1.05	1.15	V
	ARM core supply voltage 167 < f_{ARM} ≤ 400 MHz	0.85	0.95	1.15	V
	ARM core supply voltage 24 ≤ f_{ARM} ≤ 167 MHz	0.8	0.9	1.15	V
	ARM core supply voltage Stop mode	0.75	0.85	1.15	V
VCC	Peripheral supply voltage low performance mode (LPM). The DDR clock rate is 24 MHz.	0.9	0.95	1.275	V
	Peripheral supply voltage reduced performance mode (RPM). The DDR clock rate is 100 MHz.	1	1.05	1.275	V
	Peripheral supply voltage high performance mode (HPM). The clock frequencies are derived from AHB bus using 133 MHz and AXI bus using 266 MHz (as needed). The DDR clock rate is 200 MHz.	1.175	1.225	1.275	V
VDDA/VDDAL1	Memory arrays voltage—Run mode	1.15	1.20	1.275	V
	Memory arrays voltage—Stop mode	0.9[3]	0.95	1.275	V
VDD3P0	Bandgap and 480 MHz PLL supply	2.7	3.0	3.3	V
VDD2P5	Efuse, 24 MHz oscillator, 32 kHz oscillator mux supply	2.375	2.5	2.625	V
VDD1P2	PLL digital supplies	1.15	1.2	1.32	V
VDD1P8	PLL analog supplies	1.75	1.8	1.95	V
NVCC_JTAG	GPIO digital power supplies	1.65	1.875 or 2.775	3.1	V
NVCC_EMI_DRAM	DDR supply DDR2/LPDDR1 range	1.71	1.8	1.95	V
	DDR supply LPDDR2 range	1.14	1.2	1.3	V
VREF	DRAM Reference Voltage Input		1/2 NVCC_EMI_DRAM		
VDDO25	EMI Pad Predriver supply	2.375	2.5	2.625	V

Table 9. i.MX50 Operating Ranges (continued)

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
NVCC_NANDF NVCC_SD1 NVCC_SD2 NVCC_KEYPAD NVCC_EIM NVCC_EPDC NVCC_LCD NVCC_MISC NVCC_SPI NVCC_SSI NVCC_UART	High voltage I/O (HVIO) supplies HVIO_L HVIO_H	 1.65 2.7	 1.875 3.0	 1.95 3.3	V
NVCC_SRTC	SRTC core and I/O supply (LVIO)	1.1	1.2	1.3	V
NVCC_RESET	LVIO	1.65	1.875 or 2.775	3.1	V
USB_H1_VDDA25 USB_OTG_VDDA25[3]	USB_PHY analog supply	2.25	2.5	2.75	V
USB_H1_VDDA33 USB_OTG_VDDA33[4]	USB PHY I/O analog supply	3.0	3.3	3.6	V
VBUS	See Table 7 and Table 75 for details. This is not a power supply.	—	—	—	—
T_A	Ambient Temperature, Consumer	0	—	70	°C
T_j	Junction Temperature, Consumer	0	—	90	°C

1 Voltage at the package power supply contact must be maintained between the minimum and maximum voltages. The design must allow for supply tolerances and system voltage drops.

2 The nominal values for the supplies indicate the target setpoint for a tolerance no tighter than ± 50 mV. Use of supplies with a tighter tolerance allows reduction of the setpoint with commensurate power savings.

3 USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the 416MAPBGA package substrate.

4 USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the 416MAPBGA package substrate.

4.1.4 Operating Frequencies

Table 10 shows the interface frequency requirements.

Table 10. Interface Frequency

Parameter Description	Symbol	Min	Max	Unit
JTAG: TCK operating frequency	f_{tck}	See Table 61		MHz
CKIL: operating frequency	f_{ckil}	32.768[1]		kHz
CKIH: operating frequency	f_{ckih}	See Table 35		MHz
XTAL oscillator	f_{xtal}	22	27	MHz

1 Generated Internally or applied externally.

4.1.5 Supply Current

Table 11 shows the run mode current consumption of the i.MX50.

Table 11. E-Fuse Supply Current

Description	Symbol	Min	Typ	Max	Unit
eFuse program current[1] VDD2P5 current is required to program one eFuse bit.	$I_{program}$	—	40	55	mA

1 The current $I_{program}$ is only required during program time ($t_{program}$).

Table 12 shows the maximum supply current consumption of the i.MX50 for PMIC specification purposes.

Table 12. Maximum Supply Current Consumption

Condition	Supply	Voltage (V)	Current (mA)	Power (mW)
• T_a = 70°C • ARM core in RUN mode • ARM CLK = 800 MHz • SYS CLK = 266 MHz • AHB CLK = 133 MHz • DDR CLK = 266 MHz • All voltages operating at maximum levels • External (MHz) crystal and on-chip oscillator enabled • All modules enabled	VDDGP	1.15	628	723
	VCC	1.275	185	236
	VDDA/VDDAL1	1.275	40	51
	VDD1P2	1.3	5.92	7.70
	VDD1P8	1.95	1.53	2.99
	VDD2P5[1]	2.75	1.13	3.11
	VDD3P0	3.3	1.61	5.32
	NVCC_EMI_DRAM	1.95	8.3	16.17
	VDD_DCDCi	1.95	0.021	0.041
	USB_OTG_VDDA33 + USB_H1_VDDA33	3.6	10.8	38.8
	VDDO2P5 + USB_OTG_VDDA25 + USB_H1_VDDA25	2.75	12.45	34.239
	NVCC_RESET	3.1	0.226	0.701
	NVCC_SRTC	1.3	0.0035	0.0045
	Total			1120

1 During eFuse programming, the maximum current on VDD2P5 will exceed these values. See Table 11 for the maximum VDD2P5 current during eFuse programming.

Table 13. Stop Mode Current and Power Consumption [1]

Supply	Voltage (V)	Current (mA)	
		Typical, T_a = 25°C	Max, T_a = 25°C
VDDGP	0.85	0.057	0.198

Table 13. Stop Mode Current and Power Consumption (continued)[1]

Supply	Voltage (V)	Current (mA)	
		Typical, T_a = 25°C	Max, T_a = 25°C
VCC	0.95	0.544	1.890
VDDA/VDDAL1	0.95	0.071	0.247

1 The typical power, at Ta = 25°C, will be < 1 mW, including all supplies. Total max power, at Ta=25°C, will not exceed 2.5 mW, including all supplies.

4.1.5.1 Conditions for Stop Mode Current and Power Consumption

- ARM core in STOP mode and power gated
- VDDGP, VCC, and VDDA/VDDAL1 voltages at suspend levels
- VDD3P0, VDD2P5, VDD1P8, and VDD1P2 powered off
- USB_VDDA25 and USB_VDDA33 powered off
- All other supply voltages at nominal levels
- External (MHz) crystal and on-chip oscillator disabled
- CKIL input ON with 32 kHz signal present
- All PLLs OFF, all CCM-generated clocks OFF
- All modules disabled
- No external resistive loads that cause current

4.1.6 USB-OH-1 (OTG + 1 Host Port) Current Consumption

Table 14 shows the USB interface current consumption.

Table 14. USB Interface Current Consumption

Parameter	Conditions		Typical @ 25 °C	Max	Unit
Analog supply 3.3 V USB_H1_VDDA33 USB_OTG_VDDA33	Full speed	RX	5.5	6	mA
		TX	7	8	
	High speed	RX	5	6	
		TX	5	6	
Analog supply 2.5 V USB_H1_VDDA25 USB_OTG_VDDA25	Full speed	RX	6.5	7	mA
		TX	6.5	7	
	High speed	RX	12	13	
		TX	21	22	

Table 14. USB Interface Current Consumption (continued)

Parameter	Conditions		Typical @ 25 °C	Max	Unit
Digital supply VCC (1.2 V)	Full speed	RX	6	7	mA
		TX	6	7	
	High speed	RX	6	7	
		TX	6	7	

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

The system design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences can result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX50 processor (worst-case scenario)

4.2.1 Power-Up Sequence

Figure 2 shows the power-up sequence.

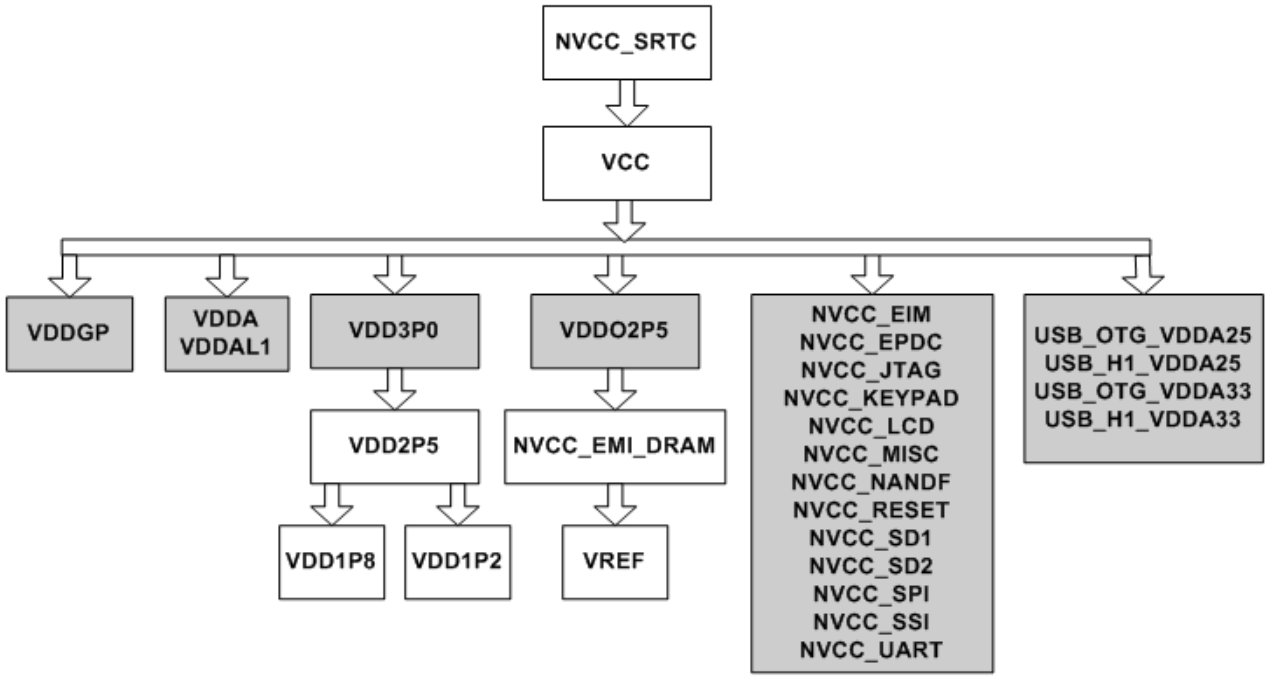


Figure 2. Power-Up Sequence

NOTE

1) The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.

2) No power-up sequence dependencies exist between the supplies shown shaded in gray.

4.2.2 Power-Down Sequence

The power-down sequence is recommended to be the opposite of the power-up sequence. In other words, the same power supply constraints exist while powering off as while powering on.

4.2.3 Resume Sequence

When the i.MX50 is resuming from STOP mode, there are some special sequencing considerations. The resume timing is determined by the following internal counters:

1. STBY_COUNT. This register is in the CCM block and may be set to a maximum of 16 x 32 kHz cycles, or 500 µsec.
2. OSCNT. This register is in the CCM block and may be set to a maximum of 256 x 32 kHz cycles, or 8 msec. This counter is intended to give the 24MHz clock time to start up and stabilize.

If the PMIC_RDY input is used and BYPASS_PMIC_VFUNCTIONAL_READY = 0, the i.MX50 will wait for STBY_COUNT cycles after PMIC_STBY_REQ negation before checking PMIC_RDY status. Once the STBY_COUNT has expired AND the PMIC_RDY signal has been asserted, the OSCNT counter begins and the 24MHz oscillator is powered up. After OSCNT expires the processor will enter RUN mode.

If the PMIC_RDY input is not used, the processor will attempt to start the 24 MHz oscillator after STBY_COUNT expires. So at a minimum, all the supplies necessary to start up the 24 MHz oscillator need to be powered before STBY_COUNT expires: NVCC_SRTC,VDD1P2, VDD1P8, VDD2P5, VDD3P0. After STBY_COUNT expires, the OSCNT counter begins and the 24 MHz oscillator is powered up. After OSCNT expires the processor will enter RUN mode, so all other supplies need to be at the appropriate operating levels before OSCNT expires.

4.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O and High-Speed General Purpose I/O (GPIO)
- Double Data Rate 2 (DDR2)
- Low Power Double Data Rate 2 (LPDDR2)
- Low Power Double Data Rate 1(LPDDR1)
- Low Voltage I/O (LVIO)
- High Voltage I/O (HVIO)
- Secure Digital Host Controllers (eSDHCv2 and eSDHCv3)
- USB-OTG and USB Host ports

NOTE

The term **OVDD** in this section refers to the associated supply rail of an input or output.

4.3.1 GPIO I/O DC Parameters

The parameters in Table 15 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 15. GPIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
High-level output voltage	Voh	Ioh=-1mA Ioh=spec'ed Drive	OVDD-0.15 0.8*OVDD	—	—	V
Low-level output voltage	Vol	Iol=1mA Iol=specified Drive	—	—	0.15 0.2*OVDD	V
High-level output current (1.1-1.3V ovdd)	I Ioh	Voh=0.8*OVDD Low Drive Medium Drive High Drive Max Drive	 -0.85 -1.7 -2.5 -3.4	—	—	 mA
Low-level output current (1.1-1.3V ovdd)	I Iol	Vol=0.2*OVDD Low Drive Medium Drive High Drive Max Drive	 0.9 1.9 2.9 3.8	—	—	 mA
High-level output current (1.65-3.1V ovdd)	I Ioh	Voh=0.8*OVDD Low Drive Medium Drive High Drive Max Drive	 -2.1 -4.2 -6.3 -8.4	—	—	 mA
Low-level output current (1.65-3.1V ovdd)	I Iol	Vol=0.2*OVDD Low Drive Medium Drive High Drive Max Drive	 2.1 4.2 6.3 8.4	—	—	 mA
High-Level DC input voltage [1]	VIH	—	0.7*OVDD	—	OVDD	V
Low-Level DC input voltage	VIL	—	0V	—	0.3*OVDD	V
Input Hysteresis	VHYS	OVDD=1.875 OVDD=2.775	0.25	0.34 0.45	—	V
Schmitt trigger VT+ [2]	VT+	—	0.5*OVDD	—	—	V
Schmitt trigger VT-	VT-	—	—	—	0.5*OVDD	V
Pull-up resistor (22 KΩ PU)	Rpu	Vi=OVDD/2	20	24	28	KΩ
Pull-up resistor (47 KΩ PU)	Rpu	Vi=OVDD/2	43	51	59	KΩ
Pull-up resistor (100 KΩ PU)	Rpu	Vi=OVDD/2	91	108	125	KΩ
Pull-down resistor (100 KΩ PD)	Rpd	Vi=OVDD/2	91	108	126	KΩ

Table 15. GPIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
Input current (no pull-up/down)	IIN	VI = 0 VI=OVDD	—	1.7	250 120	nA
Input current (22 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	161 0.12	μA
Input current (47 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	76 0.12	μA
Input current (100 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	36 0.12	μA
Input current (100 KΩ PD)	IIN	VI = 0 VI=OVDD	—	—	0.25 36	μA
External pull-up / pull-down resistor required to overdrive internal keeper	Rext	—	—	—	47	KΩ

1 To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1ns to 1s. VIL and VIH do not apply when hysteresis is enabled.

2 Hysteresis of 250 mV is guaranteed overall operating conditions when hysteresis is enabled.

4.3.2 DDR2 I/O DC Parameters

The DDR2 interface fully complies with JESD79-2E DDR2 JEDEC standard release April, 2008. The Jedec LPDDR2 specification (JESD209_2B) supersedes any specification in this document. The parameters in Table 16 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 16. DDR2 DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
High-level output voltage	Voh	—	0.9*ovdd	—	—	V
Low-level output voltage	Vol	—	—	—	0.1*ovdd	V
Output min source current[1]	Ioh(dc)	—	-7.5	—	—	mA
Output min sink current[2]	Iol(dc)	—	7.5	—	—	mA
Input reference voltage	Vref	—	0.49*ovdd	0.5*ovdd	0.51*ovdd	—
DC input high voltage (data pins)	Vihd(dc)	—	Vref+0.125	—	ovdd+0.3	V
DC input low voltage (data pins)	Vild(dc)	—	-0.3	—	Vref-0.125	V
DC input voltage[3] (clk pins)	Vin(dc)	—	-0.3	—	ovdd+0.3	V
DC differential input voltage[4]	Vid(dc)	—	0.25	—	ovdd+0.6	V
Termination voltage[5]	Vtt	—	Vref-0.04	Vref	Vref+0.04	—
Input current[6] (no pull-up/down)	Iin	VI = 0 VI=ovdd	—	0.07 2	5 360	nA
Tri-state I/O supply current[6]	Icc-ovdd	VI = ovdd or 0	—	2.3	480	nA
Tri-state 2.5V predrivers supply current[6]	Icc-vdd2p5	VI = ovdd or 0	—	6.4	750	nA
Tri-state core supply current[6]	Icc-vddi	VI = ovdd or 0	—	3.1	720	nA

1 ovdd=1.7 V; Vout=1.42 V. (Vout-ovdd)/Ioh must be less than 21 Ω for values of Vout between ovdd and ovdd-0.28 V.

2 ovdd=1.7 V; Vout=280 mV. Vout/Iol must be less than 21 Ω for values of Vout between 0 V and 280 mV.

3 Vin(dc) specifies the allowable dc excursion of each differential input.

4 Vid(dc) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “pure” input level and Vcp is the “complementary” input level. the minimum value is equal to Vih(dc) -Vil(dc).

5 Vtt is expected to track ovdd/2.

6 Typ condition: typ model, 1.8 V, and 25 °C. Max condition: BCS model, 1.9 V, and 125 °C. Min condition: WCS model, 1.7 V, and -40 °C.

4.3.3 Low Power DDR2 I/O DC Parameters

The LPDDR2 interface fully complies with JEDEC standard release April, 2008. The parameters in Table 17 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 17. LPDDR2 I/O DC Electrical Parameters

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
High-level output voltage	Voh	—	0.9*ovdd	—	—	V
Low-level output voltage	Vol	—	—	—	0.1*ovdd	V
Input reference voltage	Vref	—	0.49*ovdd	0.5*ovdd	0.51*ovdd	—
DC input high voltage	Vih(dc)	—	Vref+0.13	—	ovdd	V
DC input low voltage	Vil(dc)	—	ovss	—	Vref-0.13	V

Table 17. LPDDR2 I/O DC Electrical Parameters (continued)

Differential input logic high[1]	Vih(diff)	—	0.26	—	—	V
Differential input logic low[1]	Vil(diff)	—	—	—	-0.26	V
Input current (no pull-up/down)	Iin	VI = 0 VI=ovdd	—	0.02 1.5	12.8 290	nA
Tri-state I/O supply current[2]	Icc-ovdd	VI = ovdd or 0	—	1.85	400	nA
Tri-state 2.5 V predrivers supply current[2]	Icc-vdd2p5	VI = ovdd or 0	—	5	700	nA
Tri-state core supply current[2]	Icc-vddi	VI = ovdd or 0	—	3	700	nA
Pullup/Pulldown impedance mismatch[2]	—	—	-15	—	+15	%
240 Ω unit calibration resolution	—	—	—	—	10	Ω

1 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

2 Typ condition: typ model, 1.2V, and 25 °C. Max condition: BCS model, 1.3V, and 125 °C. Min condition: WCS model, 1.14V, and -40 °C.

4.3.4 Low Power DDR1 I/O DC Parameters

The LPDDR1 interface fully complies with JEDEC standard release April, 2008. The parameters in Table 18 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 18. LPDDR1 Mode DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
High-level output voltage	Voh	Ioh=-0.1mA	0.9*ovdd	—	—	V
Low-level output voltage	Vol	Iol=0.1mA	—	—	0.1*ovdd	V
DC input high voltage (data pins)	Vihd(dc)	—	0.7*ovdd	—	ovdd+0.3	V
DC input low voltage (data pins)	Vild(dc)	—	-0.3	—	0.3*ovdd	V
DC input voltage[1] (clk pins)	Vin(dc)	—	-0.3	—	ovdd+0.3	V
DC input differential voltage[2]	Vid(dc)	—	0.4*ovdd	—	ovdd+0.6	V
Input current[3] (no pull-up/down)	Iin	VI = 0 VI=ovdd	—	0.07 2	5 360	nA
Tri-state I/O supply current[3]	Icc-ovdd	VI = ovdd or 0	—	2.3	480	nA
Tri-state 2.5V predrivers supply current[3]	Icc-vdd2p5	VI = ovdd or 0	—	5.3	680	nA
Tri-state core supply current[3]	Icc-vddi	VI = ovdd or 0	—	3.1	720	nA

1 Vin(dc) specifies the allowable dc excursion of each differential input.

2 Vid(dc) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “pure” input level and Vcp is the “complementary” input level. the minimum value is equal to Vih(dc) -Vil(dc).

3 Typ condition: typ model, 1.8 V, and 25 °C. Max condition: BCS model, 1.9 V, and 105 °C. Min condition: WCS model, 1.7 V, and -20 °C.

4.3.5 Low Voltage I/O (LVIO) DC Parameters

The parameters in Table 19 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 19. LVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
High-level output voltage	Voh	Ioh=-1mA Ioh=spec’ed Drive	OVDD-0.15 0.8*OVDD	—	—	V
Low-level output voltage	Vol	Iol=1mA Iol=specified Drive	—	—	0.15 0.2*OVDD	V
High-level output current	I Ioh	Voh=0.8*OVDD Low Drive Medium Drive High Drive Max Drive	 -2.1 -4.2 -6.3 -8.4	—	—	 mA
Low-level output current	I Iol	Vol=0.2*OVDD Low Drive Medium Drive High Drive Max Drive	 2.1 4.2 6.3 8.4	—	—	 mA
High-Level DC input voltage [1]	VIH	—	0.7*OVDD	—	OVDD	V
Low-Level DC input voltage	VIL	—	0V	—	0.3*OVDD	V

Table 19. LVIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
Input Hysteresis	VHYS	OVDD=1.875 OVDD=2.775	0.35	0.62 1.27	—	V
Schmitt trigger VT+ [2]	VT+	—	0.5*OVDD	—	—	V
Schmitt trigger VT-	VT-	—	—	—	0.5*OVDD	V
Pull-up resistor (22 KΩ PU)	Rpu	Vi=OVDD/2	20	24	28	KΩ
Pull-up resistor (47 KΩ PU)	Rpu	Vi=OVDD/2	43	51	59	KΩ
Pull-up resistor (100 KΩ PU)	Rpu	Vi=OVDD/2	91	108	125	KΩ
Pull-down resistor (100 KΩ PD)	Rpd	Vi=OVDD/2	91	108	126	KΩ
Input current (no pull-up/down)	IIN	VI = 0 VI=OVDD	—	1.7	250 120	nA
Input current (22 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	161 0.12	μA
Input current (47 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	76 0.12	μA
Input current (100 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	36 0.12	μA
Input current (100 KΩ PD)	IIN	VI = 0 VI=OVDD	—	—	0.25 36	μA
External pull-up / pull-down resistor required to overdrive internal keeper	Rext	—	—	—	47	KΩ

[1] To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.

[2] Hysteresis of 350 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.3.6 High Voltage I/O (HVIO) DC Parameters

Table 20 shows the HVIO DC electrical operating conditions. The parameters are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 20. HVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
High-level output voltage	Voh	Ioh=-1mA Ioh=spec'ed Drive	OVDD-0.15 0.8*OVDD	—	—	V
Low-level output voltage	Vol	Iol=1mA Iol=specified Drive	—	—	0.15 0.2*OVDD	V
High-level output current, low voltage mode	Ioh_lv	Voh=0.8*OVDD Low Drive Medium Drive High Drive	 -2.2 -4.4 -6.6	—	—	 mA

Table 20. HVIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
High-level output current, high voltage mode	Ioh_hv	Vol=0.8*OVDD Low Drive Medium Drive High Drive	 -5.1 -10.2 -15.3	—	—	 mA
Low-level output current, low voltage mode	Iol_lv	Voh=0.2*OVDD Low Drive Medium Drive High Drive	 2.2 4.4 6.6	—	—	 mA
Low-level output current, high voltage mode	Iol_hv	Voh=0.2*OVDD Low Drive Medium Drive High Drive	5.1 10.2 15.3	—	—	 mA
High-Level DC input voltage[1]	VIH	—	0.7*OVDD	—	OVDD	V
Low-Level DC input voltage	VIL	—	0V	—	0.3*OVDD	V
Input Hysteresis	VHYS	OVDD=1.875 OVDD=3.0	0.25	0.36 0.80	—	V
Schmitt trigger VT+[2]	VT+	—	0.5*OVDD	—	—	V
Schmitt trigger VT-	VT-	—	—	—	0.5*OVDD	V
Pull-up resistor (22 KΩ PU)	Rpu	Vi=OVDD/2	22	29	71	KΩ
Pull-up resistor (47 KΩ PU)	Rpu	Vi=OVDD/2	43	59	148	KΩ
Pull-up resistor (100 KΩ PU)	Rpu	Vi=OVDD/2	46	62	156	KΩ
Pull-down resistor (100 KΩ PD)	Rpd	Vi=OVDD/2	53	77	256	KΩ
Input current (no pull-up/down)	IIN	VI = 0 VI=OVDD	—	2.8	470 50	nA
Input current (22 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	153 0.05	μA
Input current (47 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	77 0.05	μA
Input current (100 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	73 0.05	μA
Input current (100 KΩ PD)	IIN	VI = 0 VI=OVDD	—	—	0.47 63	μA
High-level output current, high voltage mode	Ioh_hv	Vol=0.8*OVDD Low Drive Medium Drive High Drive	 -5.1 -10.2 -15.3	—	—	 mA
External pull-up / pull-down resistor required to overdrive internal keeper	Rext	—	—	—	2.5	KΩ

[1] To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.

[2] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.4 Output Buffer Impedance Characteristics

This section defines the I/O impedance parameters of the i.MX50 processor.

4.4.1 GPIO Output Buffer Impedance

Table 21 shows the GPIO output buffer impedance of the i.MX50 processor.

Table 21. GPIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min	Typ		Max	Unit
				OVDD 2.775 V	OVDD 1.875V		
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output driver impedance	Rpd	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

4.4.2 LVIO Output Buffer Impedance

Table 22 shows the LVIO output buffer impedance of the i.MX50 processor.

Table 22. LVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min	Typ		Max	Unit
				OVDD 2.775 V	OVDD 1.875V		
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output driver impedance	Rpd	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

4.4.3 HVIO Output Buffer Impedance

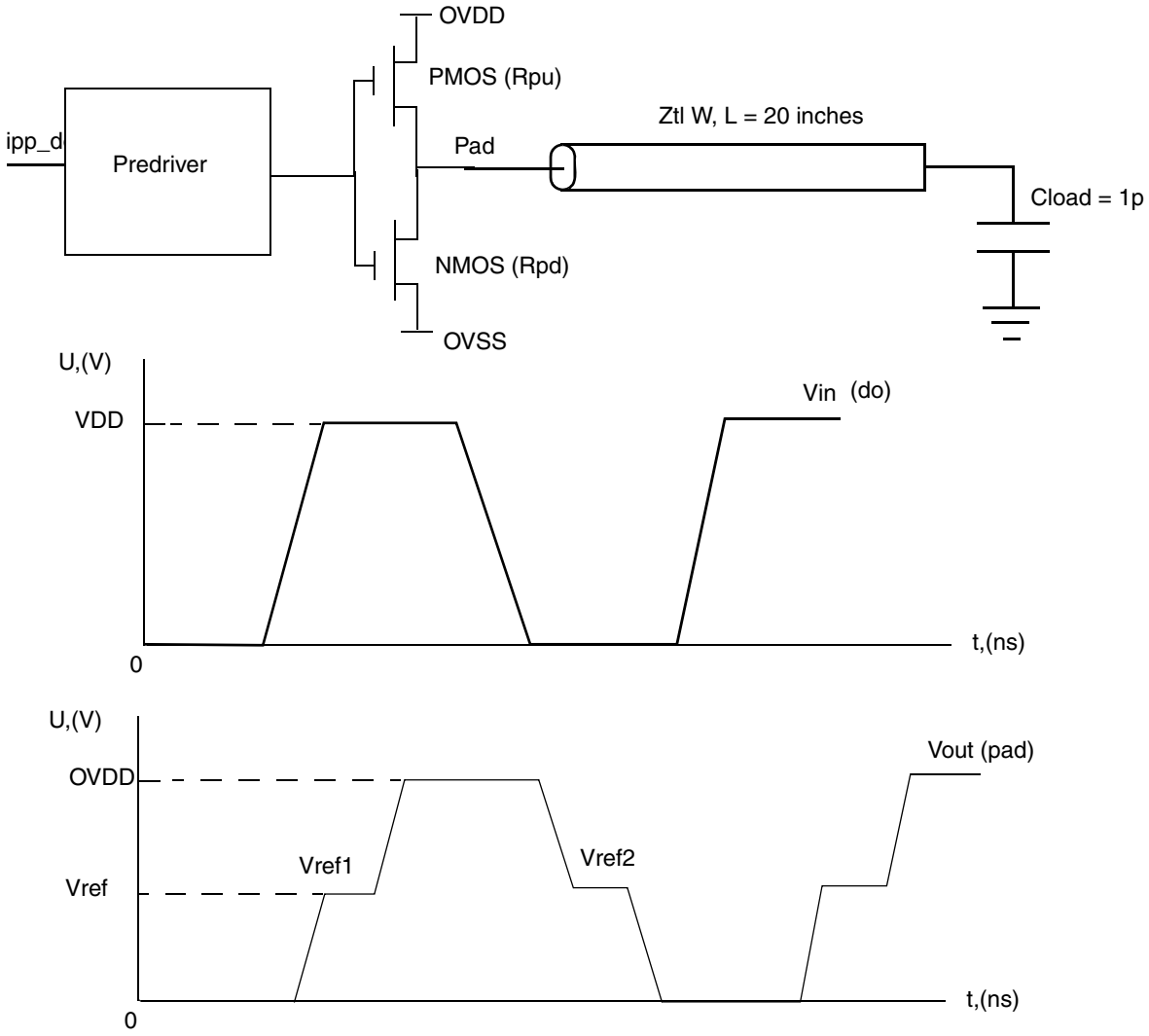
Table 23 shows the HVIO output buffer impedance of the i.MX50 processor.

Table 23. HVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min		Typ		Max		Unit
			OVDD 1.95 V	OVDD 3.3 V	OVDD 1.875 V	OVDD 3.30V	OVDD 1.65 V	OVDD 2.68 V	
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω	113.5 56.2 37.8	103.8 51.9 35.1	130.6 66 45.9	133 69.2 41	219.4 109.7 73.1	212.2 111.1 71.8	Ω
Output driver impedance	Rpd	Low drive strength, Ztl =1 50 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω	78.5 39.7 26.8	70 34.5 23	113.6 56.8 38.3	102 50 33.3	230.8 115.4 76.9	179.5 89.8 60.7	Ω

NOTE

Output driver impedance is measured with *long* transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 3).



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 3. Impedance Matching Load for Measurement

4.5 I/O AC Parameters

The load circuit and output transition time waveforms are shown in Figure 4 and Figure 5. The AC electrical characteristics for slow and fast I/O are presented in the Table 24 and Table 25, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUX control registers.

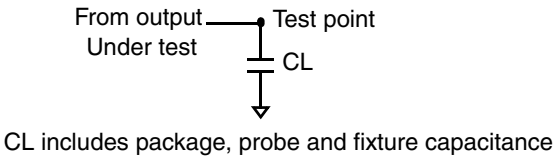


Figure 4. Load Circuit for Output

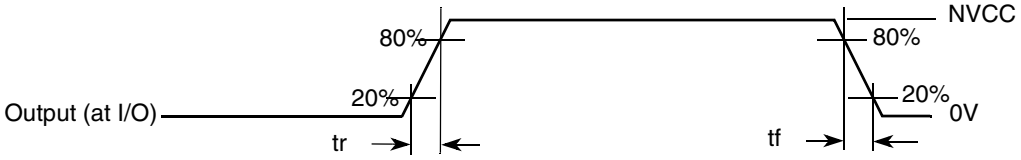


Figure 5. Output Transition Time Waveform

4.5.1 GPIO I/O Slow AC Parameters

Table 24 shows the AC parameters for GPIO slow I/O.

Table 24. GPIO I/O Slow AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF			1.91/1.52 3.07/2.65	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			2.22/1.81 3.81/3.42	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.88/2.42 5.43/5.02	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.94/4.50 10.55/9.70	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.5/0.65 0.32/0.37			V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.43/0.54 0.26/0.41			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.34/0.41 0.18/0.2			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.20/0.22 0.09/0.1			V/ns
Output Pad di/dt (Max Drive)	tdit				30	mA/ns

Table 24. GPIO I/O Slow AC Parameters (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad di/dt (High Drive)	tdit				23	mA/ns
Output Pad di/dt (Medium drive)	tdit				15	mA/ns
Output Pad di/dt (Low drive)	tdit				7	mA/ns
Input Transition Times[2]	trm				25	ns

[1] tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

[2] Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.2 GPIO I/O Fast AC Parameters

Table 25 shows the AC parameters for GPIO fast I/O.

Table 25. GPIO I/O Fast AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF			1.45/1.24 2.76/2.54	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			1.81/1.59 3.57/3.33	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.54/2.29 5.25/5.01	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.82/4.50 10.54/9.95	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.69/0.78 0.36/0.39			V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.55/0.62 0.28/0.30			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.39/0.44 0.19/0.20			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.21/0.22 0.09/0.1			V/ns
Output pad di/dt (Max drive)	tdit	—	—	—	70	mA/ns
Output pad di/dt (High drive)	tdit	—	—	—	53	mA/ns
Output pad di/dt (Medium drive)	tdit	—	—	—	35	mA/ns
Output pad di/dt (Low drive)	tdit	—	—	—	18	mA/ns
Input transition times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.3 LVIO I/O Slow AC Parameters

Table 24 shows the AC parameters for LVIO slow I/O.

Table 26. LVIO I/O Slow AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF			1.97/1.57 3.12/2.70	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			2.29/1.87 3.79/3.44	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.93/2.48 5.42/4.98	ns

Table 26. LVIO I/O Slow AC Parameters (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.92/4.57 10.64/9.85	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.50/0.63 0.32/0.37			V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.43/0.53 0.26/0.29			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.34/0.40 0.18/0.20			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.20/0.22 0.09/0.10			V/ns
Output Pad di/dt (Max Drive)	tdit				30	mA/ns
Output Pad di/dt (High Drive)	tdit				24	mA/ns
Output Pad di/dt (Medium drive)	tdit				16	mA/ns
Output Pad di/dt (Low drive)	tdit				8	mA/ns
Input Transition Times[2]	trm				25	ns

[1] tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

[2] Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.4 LVIO I/O Fast AC Parameters

Table 27 shows the AC parameters for LVIO fast I/O.

Table 27. LVIO I/O Fast AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF			1.44/1.27 2.78/2.56	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			1.80/1.61 3.59/3.34	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.55/2.28 5.32/5.01	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.74/4.59 10.59/10.21	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.69/0.78 0.36/0.39			V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.55/0.61 0.28/0.30			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.39/0.44 0.19/0.20			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.21/0.22 0.09/0.10			V/ns
Output pad di/dt (Max drive)	tdit	—	—	—	70	mA/ns
Output pad di/dt (High drive)	tdit	—	—	—	54	mA/ns
Output pad di/dt (Medium drive)	tdit	—	—	—	35	mA/ns
Output pad di/dt (Low drive)	tdit	—	—	—	18	mA/ns
Input transition times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.5 HVIO I/O Low Voltage (1.8 V) AC Parameters

Table 24 shows the AC parameters for HVIO I/O Low Voltage (1.8 V).

Table 28. HVIO I/O Low Voltage (1.8 V) AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			1.82/1.97 3.39/3.57	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.48/2.62 4.95/5.14	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.57/4.77 9.60/9.91	ns

Table 28. HVIO I/O Low Voltage (1.8 V) AC Parameters (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Slew Rate (High Drive)[1]	tr, tf	15 pF 35 pF	0.54/0.50 0.29/0.28			V/ns
Output Pad Slew Rate (Medium Drive)	tr, tf	15 pF 35 pF	0.40/0.38 0.20/0.19			V/ns
Output Pad Slew Rate (Low Drive)	tr, tf	15 pF 35 pF	0.22/0.21 0.10/0.10			V/ns
Output Pad di/dt (High Drive)	tdit				34	mA/ns
Output Pad di/dt (Medium drive)	tdit				22	mA/ns
Output Pad di/dt (Low drive)	tdit				11	mA/ns
Input Transition Times[2]	trm				25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.6 HVIO I/O High Voltage (3.0 V) AC Parameters

Table 29 shows the AC parameters for HVIO I/O High Voltage (3.0 V).

Table 29. HVIO I/O High Voltage (3.0 V) AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (High Drive)	tpr	15 pF 35 pF			2.16/1.79 3.75/3.28	ns
Output Pad Transition Times (Medium Drive)	tpr	15 pF 35 pF			2.81/2.40 5.06/4.58	ns
Output Pad Transition Times (Low Drive)	tpr	15 pF 35 pF			4.69/4.15 8.91/8.51	ns
Output Pad Slew Rate (High Drive)[1]	tps	15 pF 35 pF	0.75/0.90 0.43/0.49			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.57/0.67 0.32/0.35			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.34/0.39 0.18/0.19			V/ns
Output pad di/dt (High drive)	tdit	—	—	—	55	mA/ns
Output pad di/dt (Medium drive)	tdit	—	—	—	36	mA/ns
Output pad di/dt (Low drive)	tdit	—	—	—	16	mA/ns
Input transition times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.7 DDR2 I/O AC Parameters

Table 30 shows the AC parameters for DDR2 I/O.

Table 30. DDR2 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vih(ac)	Vref+0.25	-	V
AC input logic low	Vil(ac)	-	Vref-0.25	
AC differential input voltage[1]	Vid(ac)	0.5	ovdd	
AC Input differential cross point voltage[2]	Vix(ac)	0.5*ovdd -0.175	0.5*ovdd + 0.175	
AC output differential cross point voltage [3]	Vox(ac)	0.5*ovdd -0.125	0.5*ovdd+ 0.125	
Output propagation delay high to low	t_{POHLD}		3.5	ns
Output propagation delay low to high	t_{POLHD}		3.5	
Input propagation delay high to low	t_{PIHLD}		1.5	
Input propagation delay low to high	t_{PILHD}		1.5	
Single output slew rate	tsr	0.4	2	V/ns

[1]Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac)

[2]The typical value of Vix(ac) is expected to be about 0.5*OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

[3]The typical value of Vox(ac) is expected to be about 0.5*OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross.

4.5.8 LPDDR1 I/O AC Parameters

Table 31 shows the AC parameters for LPDDR1 I/O.

Table 31. LPDDR1 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vihd(ac)	0.8*ovdd	ovdd+0.3	V
AC input logic low	Vild(ac)	-0.3	0.2*ovdd	
AC input differential voltage[1]	Vid(ac)	0.6*ovdd	ovdd+0.6	
AC input differential crosspoint voltage[2]	Vix(ac)	0.4*ovdd	0.6*ovdd	
Output propagation delay high to low	tPOHLD		2.5	ns
Output propagation delay low to high	tPOLHD		2.5	
Input propagation delay high to low	tPIHLD		1.5	
Input propagation delay low to high	tPILHD		1.5	
Single output slew rate	tsr	0.3	2.5	V/ns

[1]Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac)

[2]The typical value of Vix(ac) is expected to be about 0.5*ovdd. and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

4.5.9 LPDDR2 I/O AC Parameters

Table 32 shows the AC parameters for LPDDR2 I/O.

Table 32. LPDDR2 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vih(ac)	Vref+0.22	ovdd	V
AC input logic low	Vil(ac)	ovss	Vref-0.22	
AC differential input high voltage[1]	Vidh(ac)	0.44	-	
AC differential input low voltage	Vidhl(ac)	-	0.44	
AC input differential cross point voltage (relative to ovdd / 2)[2]	Vix(ac)	-0.12	0.12	
Over/undershoot peak	Vpeak		0.35	ns
Over/undershoot area (above OVDD or below OVSS)	Varea		0.6 (at 266 MHz)	V*ns
Output propagation delay high to low	tPOHLD		3.5	ns
Output propagation delay low to high	tPOLHD		3.5	
Input propagation delay high to low	tPIHLD		1.5	
Input propagation delay low to high	tPILHD		1.5	

Table 32. LPDDR2 I/O AC Parameters (continued)

Parameter	Symbol	Min	Max	Unit
Single output slew rate (Driver impedance =40Ω+/-30%)	tsr	1.5	3.5	V/ns
Single output slew rate (Driver impedance =60Ω+/-30%	tsr	1	2.5	V/ns

[1]Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the "true" input signal and Vcp is the "complementary" input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
[2]The typical value of Vix(ac) is expected to be about 0.5*OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.6 System Modules Timing

This section contains the timing and electrical parameters for the modules in the i.MX50 processor.

4.6.1 Reset Timings Parameters

Figure 6 shows the reset timing and Table 33 lists the timing parameters.

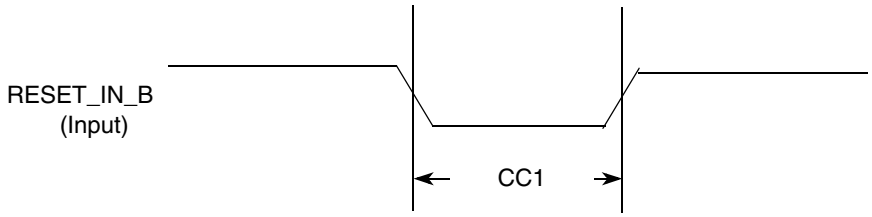


Figure 6. Reset Timing Diagram

Table 33. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of RESET_IN_B assertion to be qualified as valid (input slope = 5 ns)	50	—	ns

4.6.2 WDOG Reset Timing Parameters

Figure 7 shows the WDOG reset timing and Table 34 lists the timing parameters.

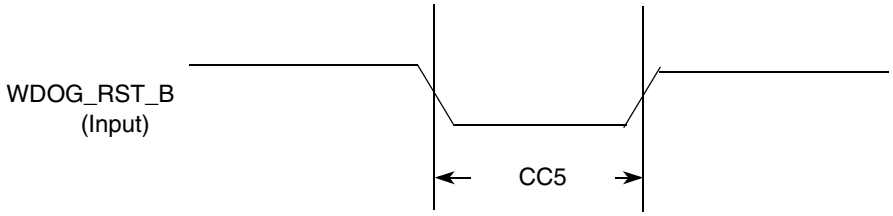


Figure 7. WDOG_RST_B Timing Diagram

Table 34. WDOG_RST_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC5	Duration of WDOG_RST_B Assertion	1	—	T_{CKIL}

NOTE

CKIL is approximately 32 kHz. T_{CKIL} is one period or approximately 30 µs.

4.6.3 Clock Amplifier Parameters (CKIH)

The input to clock amplifier (CAMP) is internally ac-coupled allowing direct interface to a square wave or sinusoidal frequency source. No external series capacitors are required.

Table 35 shows the electrical parameters of CAMP.

Table 35. CAMP Electrical Parameters (CKIH)

Parameter	Min	Typ	Max	Unit
Input frequency	8.0	—	40.0	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VCC[1] – 0.25)	—	3	V
Sinusoidal input amplitude	0.4 [2]	—	VDD	Vp-p
Output duty cycle	45	50	55	%

1 VCC is the supply voltage of CAMP.

2 This value of the sinusoidal input is determined during characterization.

4.6.4 DPLL Electrical Parameters

Table 36 shows the electrical parameters of digital phase-locked loop (DPLL).

Table 36. DPLL Electrical Parameters

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Reference clock frequency range[1]	—	10	—	100	MHz
Reference clock frequency range after pre-divider	—	10	—	40	MHz
Output clock frequency range (dpdck_2)	—	300	—	1025	MHz
Pre-division factor[2]	—	1	—	16	—
Multiplication factor integer part	—	5	—	15	—
Multiplication factor numerator[3]	Should be less than denominator	–67108862	—	67108862	—
Multiplication factor denominator[2]	—	1	—	67108863	—
Output duty cycle	—	48.5	50	51.5	%

Table 36. DPLL Electrical Parameters (continued)

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Frequency lock time[4] (FOL mode or non-integer MF)	—	—	—	398	T_{dpdref}
Phase lock time	—	—	—	100	µs
Frequency jitter[5] (peak value)	—	—	0.02	0.04	T_{dck}
Phase jitter (peak value)	FPL mode, integer and fractional MF	—	2.0	3.5	ns
Power dissipation	f_{dck} = 300 MHz @ avdd = 1.8 V, dvdd = 1.2 V f_{dck} = 650 MHz @ avdd = 1.8 V, dvdd = 1.2 V	—	—	0.65 (avdd) 0.92 (dvdd) 1.98 (avdd) 1.8 (dvdd)	mW

1 Device input range cannot exceed the electrical specifications of the CAMP, see Table 35.

2 The values specified here are internal to DPLL. Inside the DPLL, a 1 is added to the value specified by the user. Therefore, the user has to enter a value 1 less than the desired value at the inputs of DPLL for PDF and MFD.

3 The maximum total multiplication factor (MFI + MFN/MFD) allowed is 15. Therefore, if the MFI value is 15, MFN value must be zero.

4 T_{dpdref} is the time period of the reference clock after predivider. According to the specification, the maximum lock time in FOL mode is 398 cycles of divided reference clock when DPLL starts after full reset.

5 T_{dck} is the time period of the output clock, dpdck_2.

4.6.5 General Purpose Media Interface (GPMI) Parameters

The i.MX50 GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following paragraphs.

4.6.5.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 8, Figure 9, Figure 10 and Figure 11 depict the relative timing between GPMI signals at the module level for different

operations under Asynchronous mode. Table 37 describes the timing parameters (NF1–NF17) that are shown in the figures.

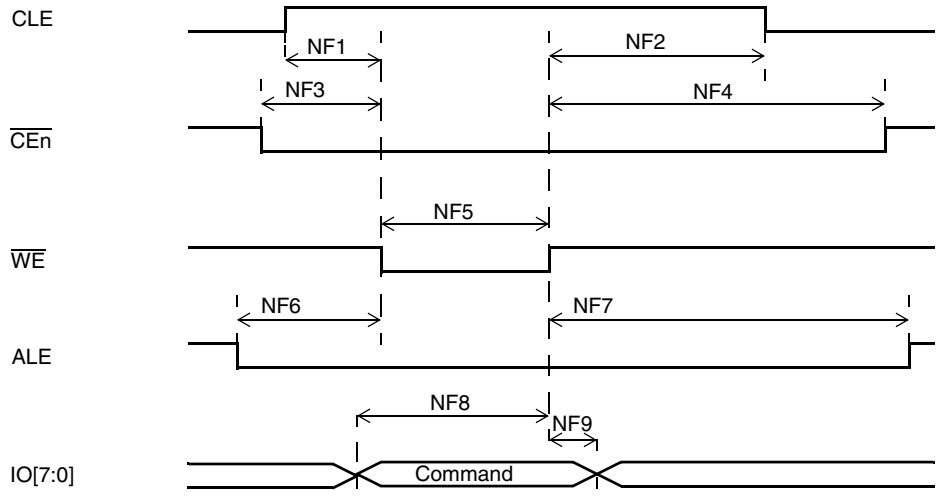


Figure 8. Command Latch Cycle Timing Diagram

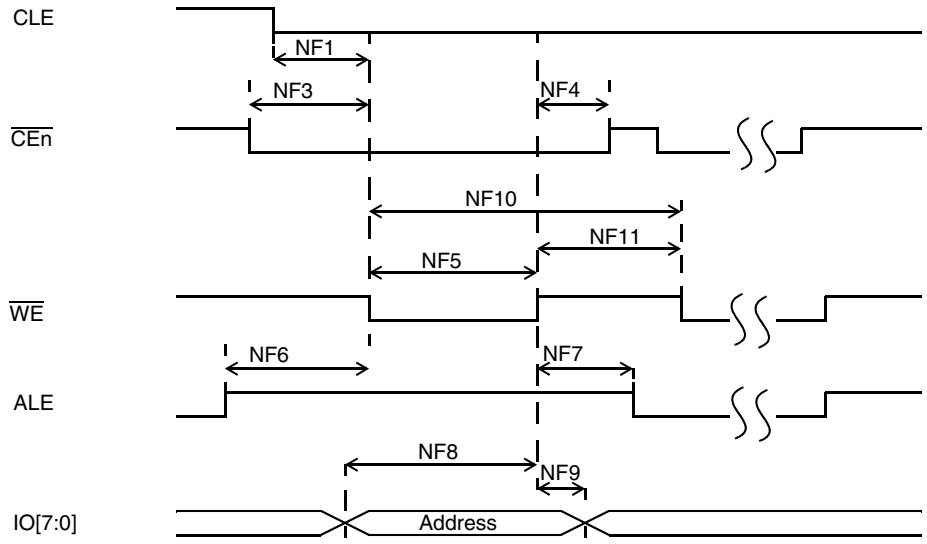


Figure 9. Address Latch Cycle Timing Diagram

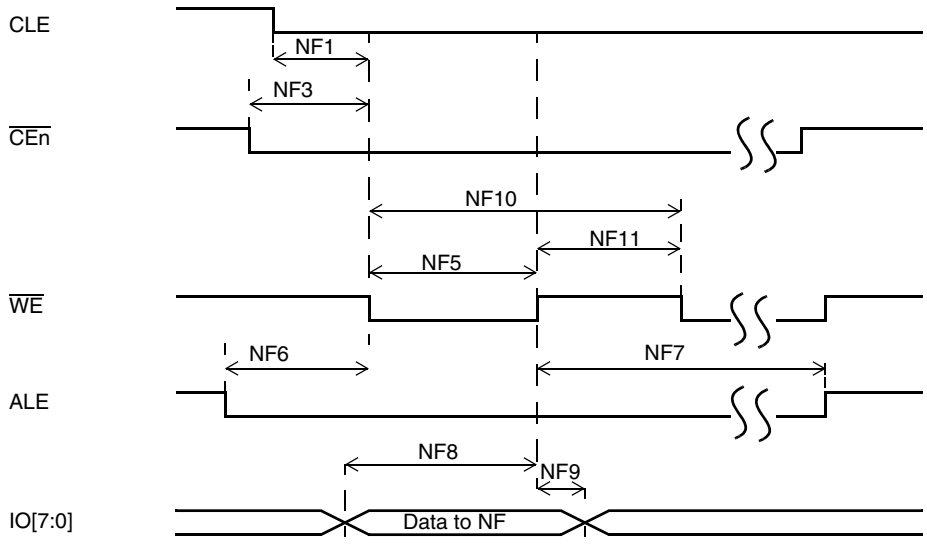


Figure 10. Write Data Latch Cycle Timing Diagram

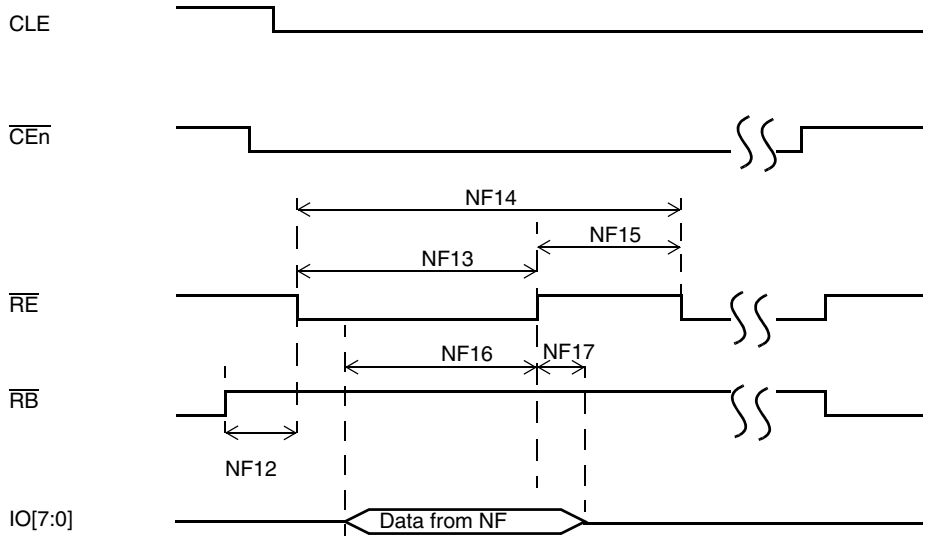


Figure 11. Read Data Latch Cycle Timing Diagram

Table 37. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T[2] = GPMI Clock Cycle[3]		Example Timing for GPMI Clock ≈ 100MHz T = 10ns		Unit
			Min.	Max.	Min.	Max.	
NF1	CLE setup time	tCLS	(AS+1)*T	—	10	—	ns
NF2	CLE hold time	tCLH	(DH+1)*T	—	20	—	ns
NF3	$\overline{\text{CEn}}$ setup time	tCS	(AS+1)*T	—	10	—	ns
NF4	$\overline{\text{CE}}$ hold time	tCH	(DH+1)*T	—	20	—	ns

Table 37. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T[2] = GPMI Clock Cycle[3]		Example Timing for GPMI Clock ≈ 100MHz T = 10ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{WE}$ pulse width	tWP	DS*T		10		ns
NF6	ALE setup time	tALS	(AS+1)*T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1)*T	—	20	—	ns
NF8	Data setup time	tDS	DS*T	—	10	—	ns
NF9	Data hold time	tDH	DH*T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH)*T		20		ns
NF11	$\overline{WE}$ hold time	tWH	DH*T		10		ns
NF12	Ready to $\overline{RE}$ low	tRR	(AS+1)*T	—	10	—	ns
NF13	$\overline{RE}$ pulse width	tRP	DS*T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH)*T	—	20	—	ns
NF15	$\overline{RE}$ high hold time	tREH	DH*T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

1 GPMI's Async Mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers' setting. In the above table, we use AS/DS/DH representing these settings each.

2 T represents for the GPMI clock period.

3 AS minimum value could be 0, while DS/DH minimum value is 1.

4.6.5.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

The following diagrams show the write and read timing of Source Synchronous Mode.

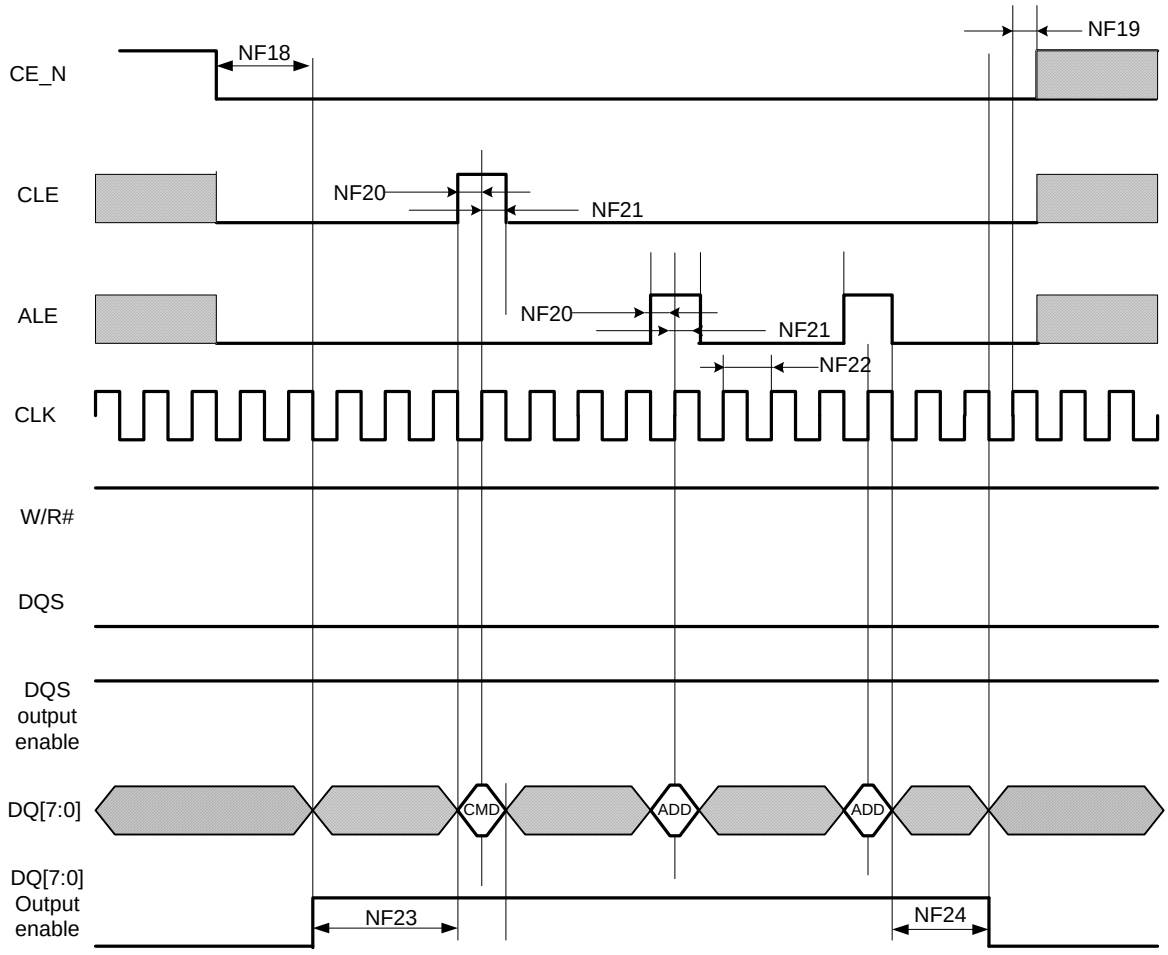


Figure 12. Source Synchronous Mode Command and Address Timing Diagram

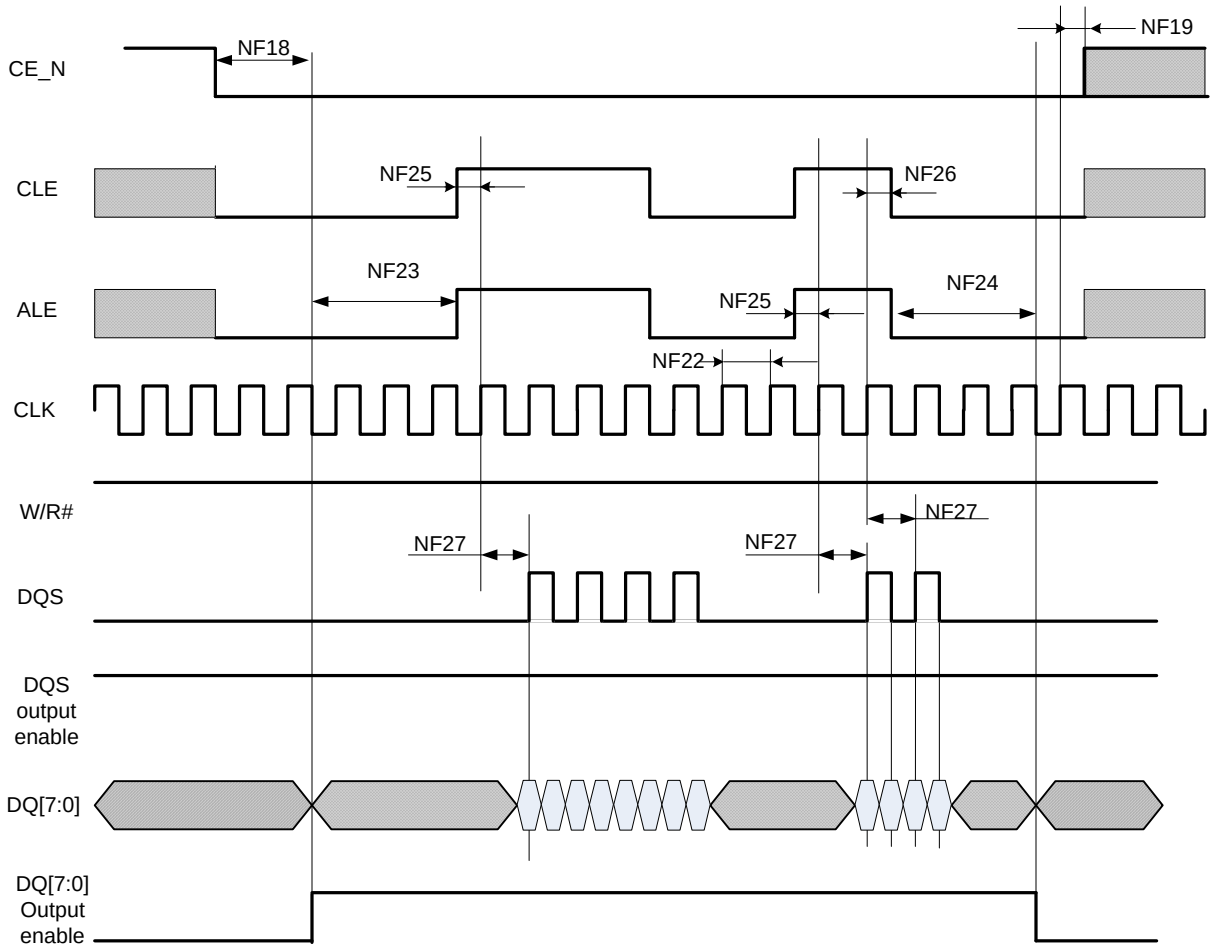


Figure 13. Source Synchronous Mode Data Write Timing Diagram

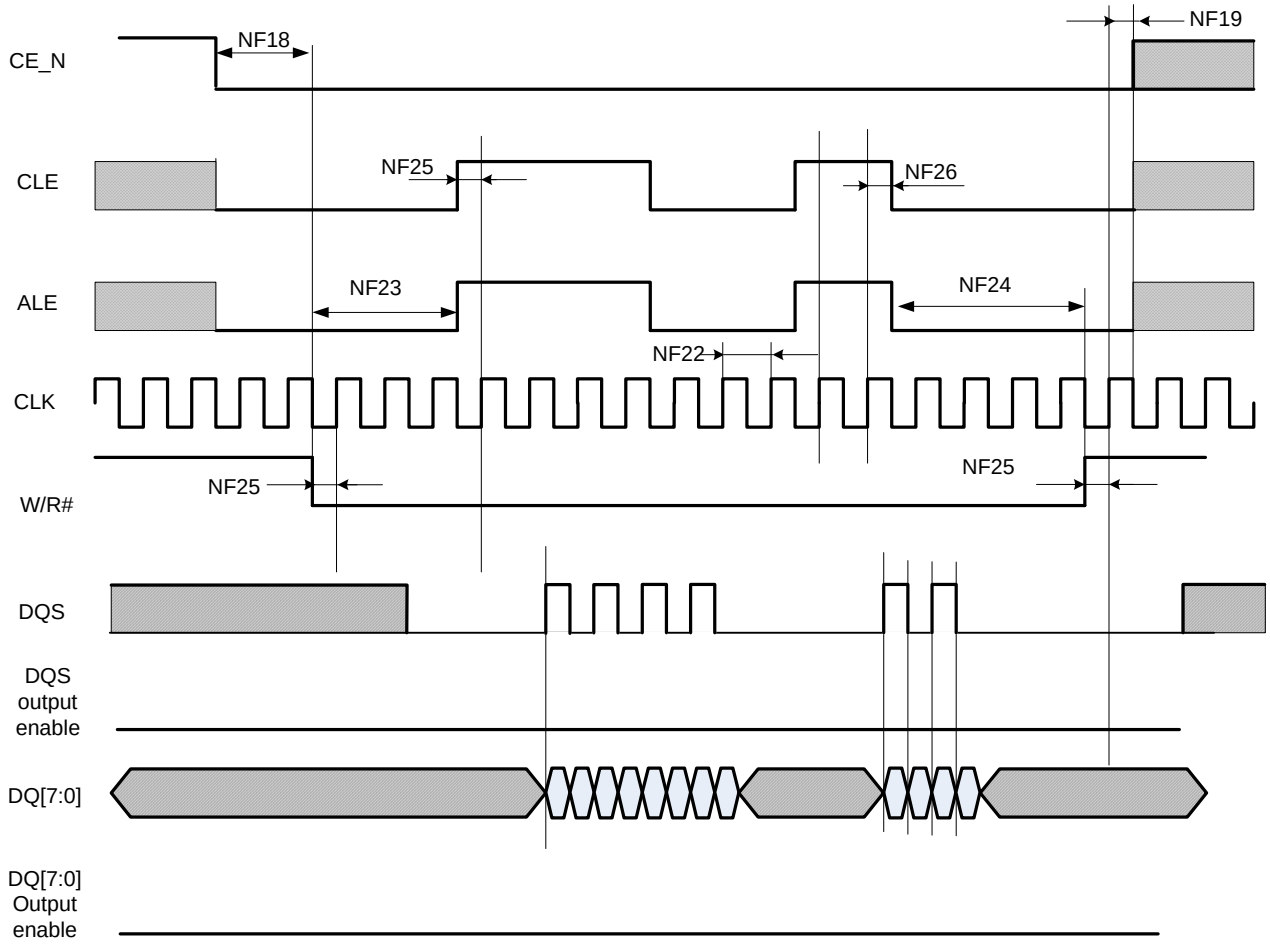


Figure 14. Source Synchronous Mode Data Read Timing Diagram

Table 38. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY*tCK	—	ns
NF19	CE# hold time	tCH	0.5 *tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5*tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5*tCK	—	ns
NF22	clock period	tCK	5	—	ns
NF23	preamble delay	tPRE	PRE_DELAY*tCK	—	ns

Table 38. Source Synchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF24	postamble delay	tPOST	POST_DELAY*tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5*tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5*tCK	—	ns
NF27	Data input to first DQS latching transition	tDQSS	tCK	—	ns

1 GPMI's sync mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' setting. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY representing these settings each.

4.6.5.3 Samsung Toggle Mode AC Timing

4.6.5.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. Please refer to the above chapter for details.

4.6.5.3.2 Read and Write Timing

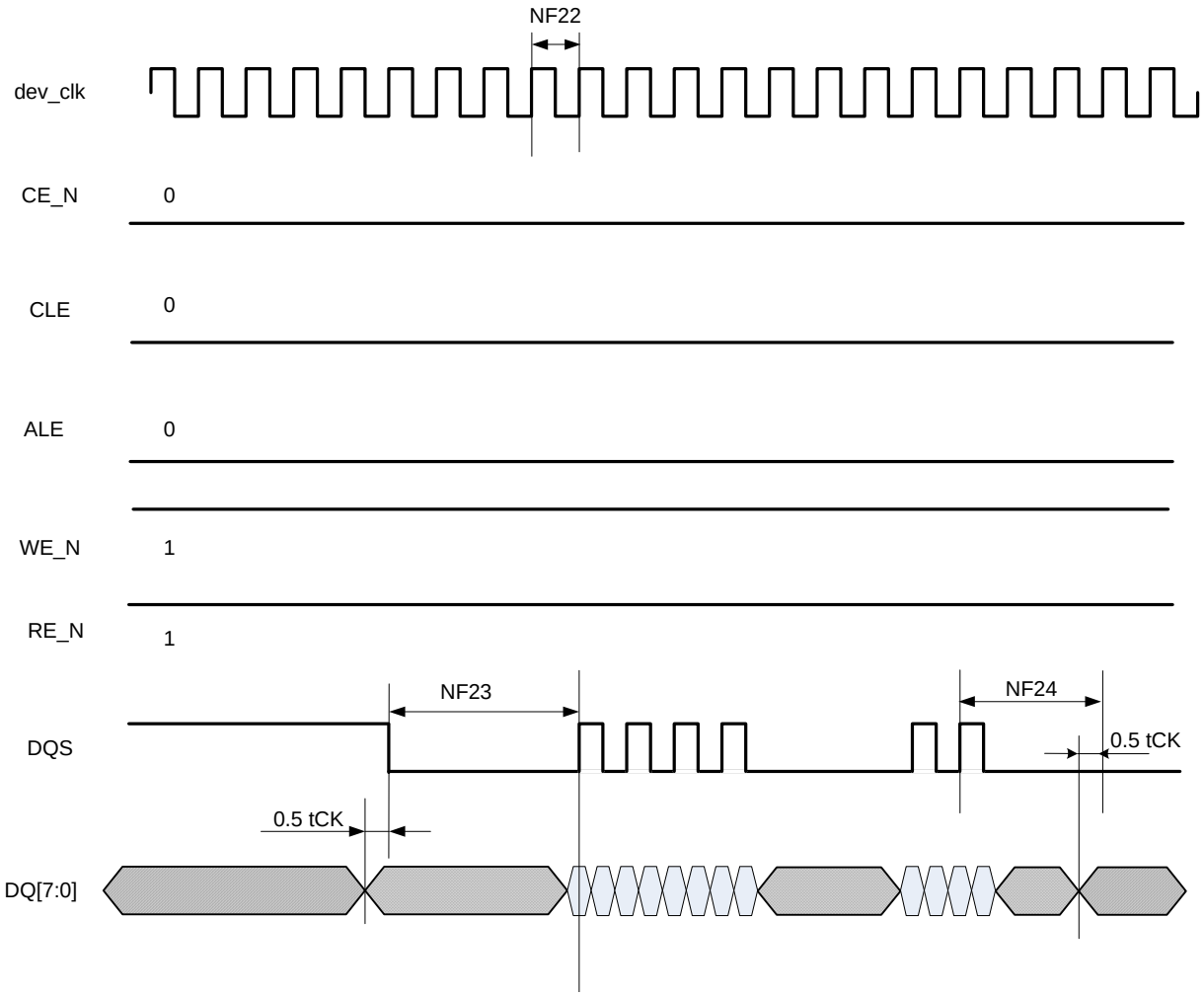


Figure 15. Samsung Toggle Mode Data Write Timing

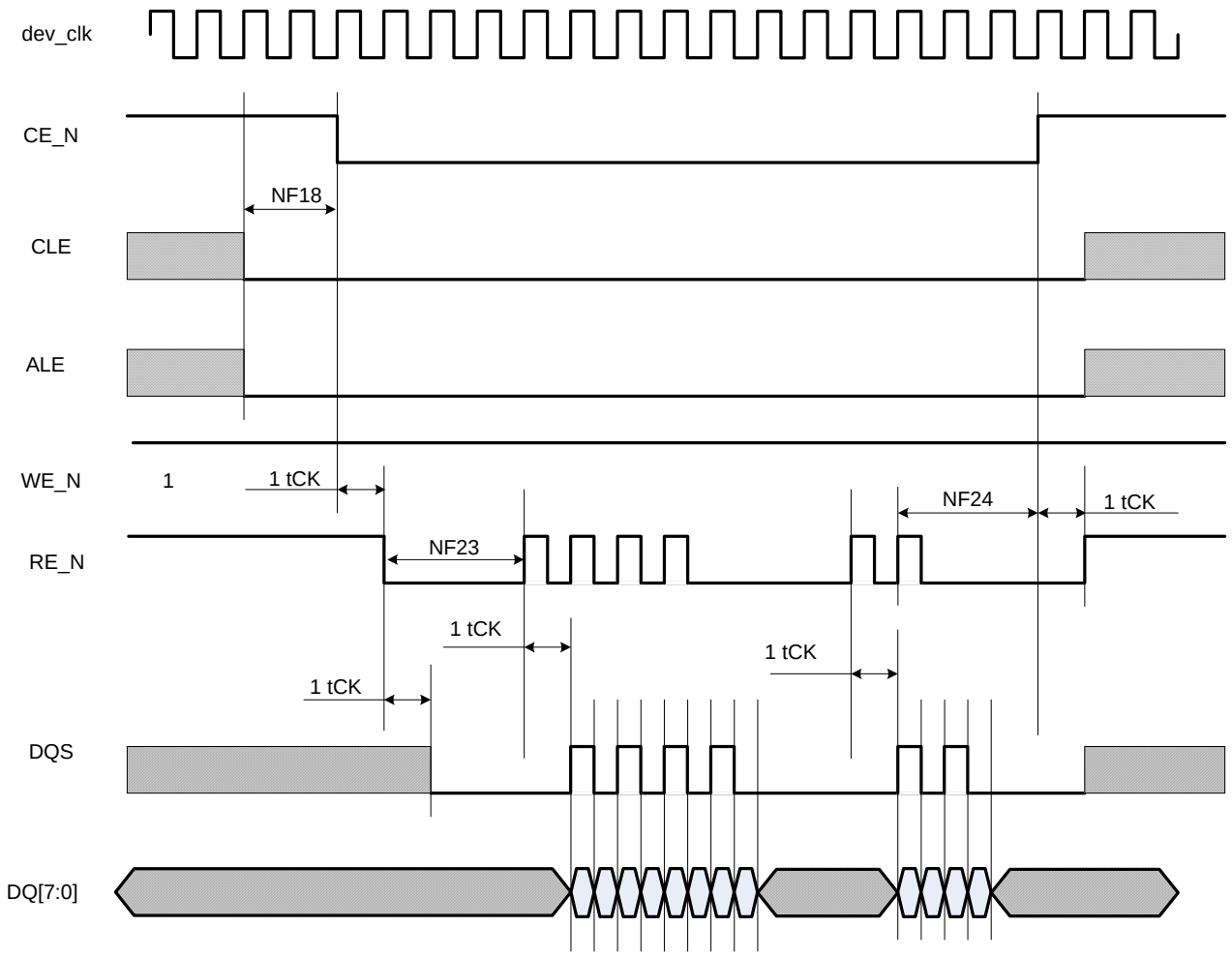


Figure 16. Samsung Toggle Mode Data Read Timing

Table 39. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY*tCK	—	ns
NF19	CE# hold time	tCH	0.5 *tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5*tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5*tCK	—	ns
NF22	clock period	tCK	7.5	—	ns

Table 39. Samsung Toggle Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF23	preamble delay	tPRE	(PRE_DELAY+1)*tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY*tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5*tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5*tCK	—	ns

[1] GPMI's sync mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' setting. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY representing these settings each.

4.7 External Interface Module (EIM)

The following sections provide information on the EIM.

4.7.1 General EIM Timing

Figure 17, Figure 18, and Table 40 specify the timings related to the EIM module. All EIM output control signals may be asserted and de-asserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

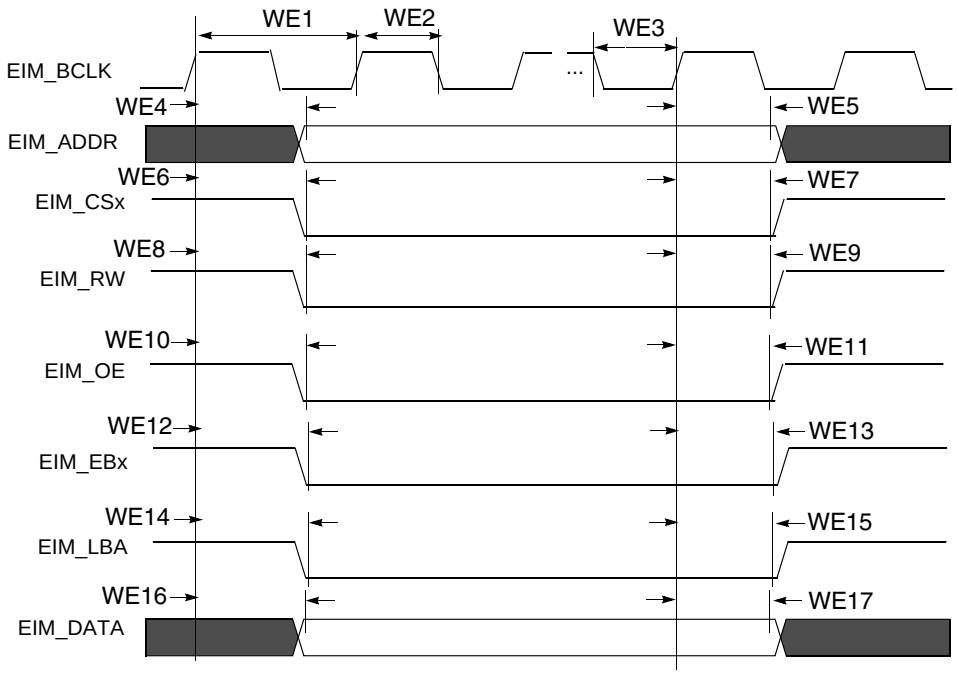


Figure 17. EIM Outputs Timing Diagram

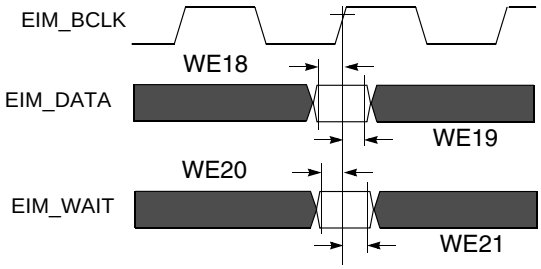


Figure 18. EIM Inputs Timing Diagram

Table 40. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2t	—	3t	—	4t	—
WE2	EIM_BCLK Low Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE3	EIM_BCLK High Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE4	Clock rise to address valid[3]	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE5	Clock rise to address invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE6	Clock rise to EIM_CSx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE7	Clock rise to EIM_CSx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE8	Clock rise to EIM_RW valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE9	Clock rise to EIM_RW invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE10	Clock rise to EIM_OE valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE11	Clock rise to EIM_OE invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE12	Clock rise to EIM_EBx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE13	Clock rise to EIM_EBx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE14	Clock rise to EIM_LBA valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE15	Clock rise to EIM_LBA invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE16	Clock rise to Output Data valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE17	Clock rise to Output Data Invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE18	Input Data setup time to Clock rise	2	—	2	—	2	—	2	—
WE19	Input Data hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—
WE20	EIM_WAIT setup time to Clock rise	2	—	2	—	2	—	2	—
WE21	EIM_WAIT hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—

1 *t* is axi_clk cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed EIM_BCLK frequency is 66.5 MHz. As a result, if BCD = 0, axi_clk must be ≤ 66.5 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a EIM_BCLK of 66.5 MHz. When the clock branch to EIM is decreased to 66.5 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for a detailed clock tree description.

2 EIM_BCLK parameters are being measured from the 50% point that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

3 For signal measurements *High* is defined as 80% of signal value and *Low* is defined as 20% of signal value.

4.7.2 Examples of EIM Accesses

Figure 19, Figure 20, Figure 21, Figure 22, Figure 23, and Figure 24 give a few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

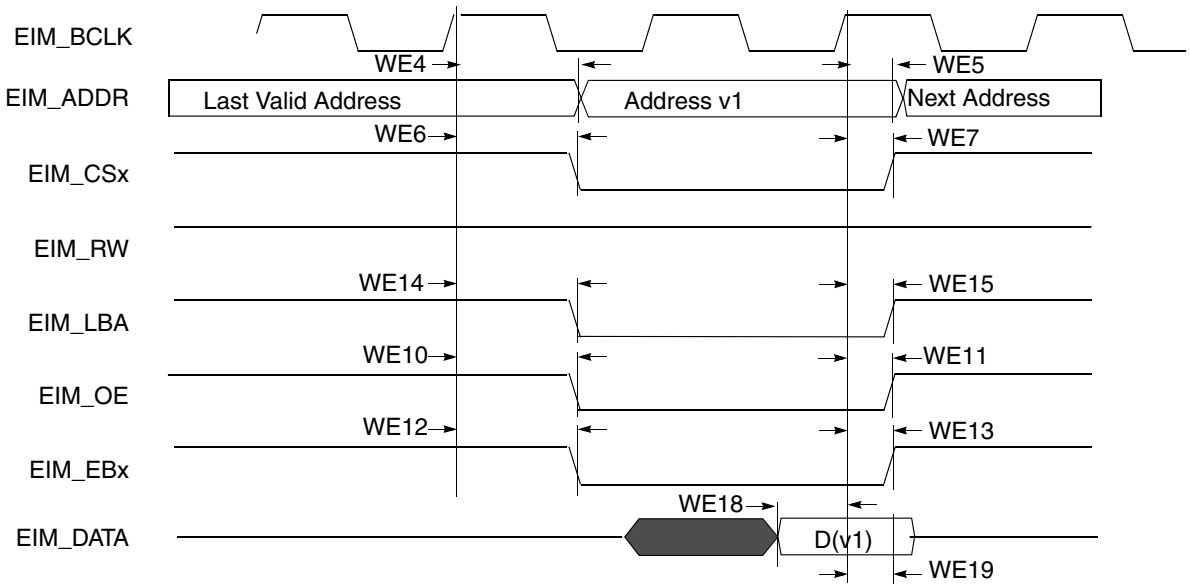


Figure 19. Synchronous Memory Read Access, WSC=1

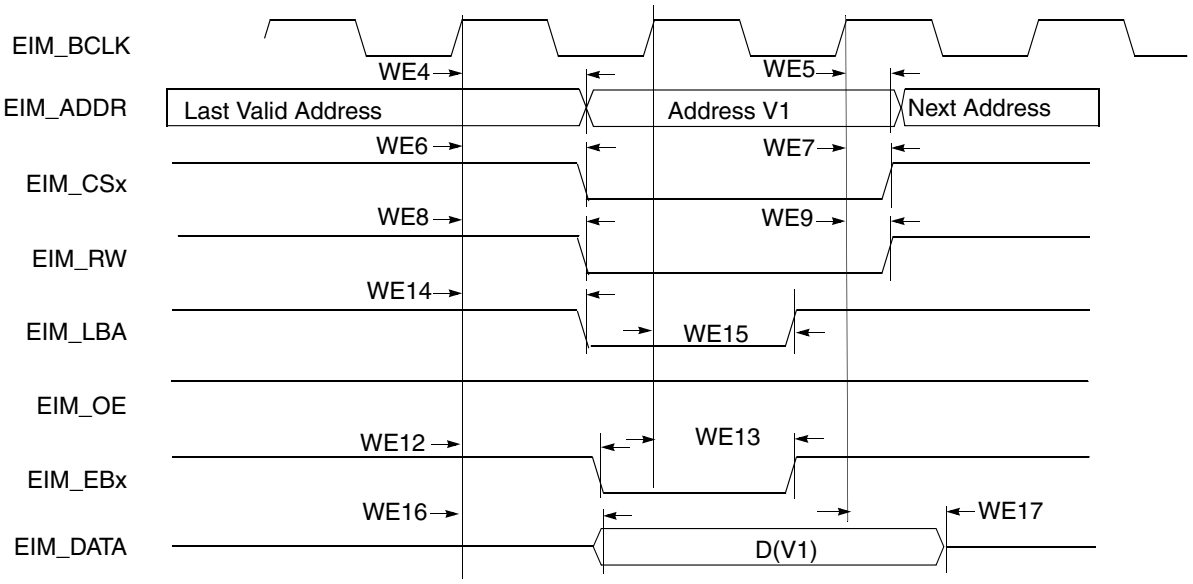


Figure 20. Synchronous Memory, Write Access, WSC=1, WBEA=1, WBEN=1, and WADVN=0

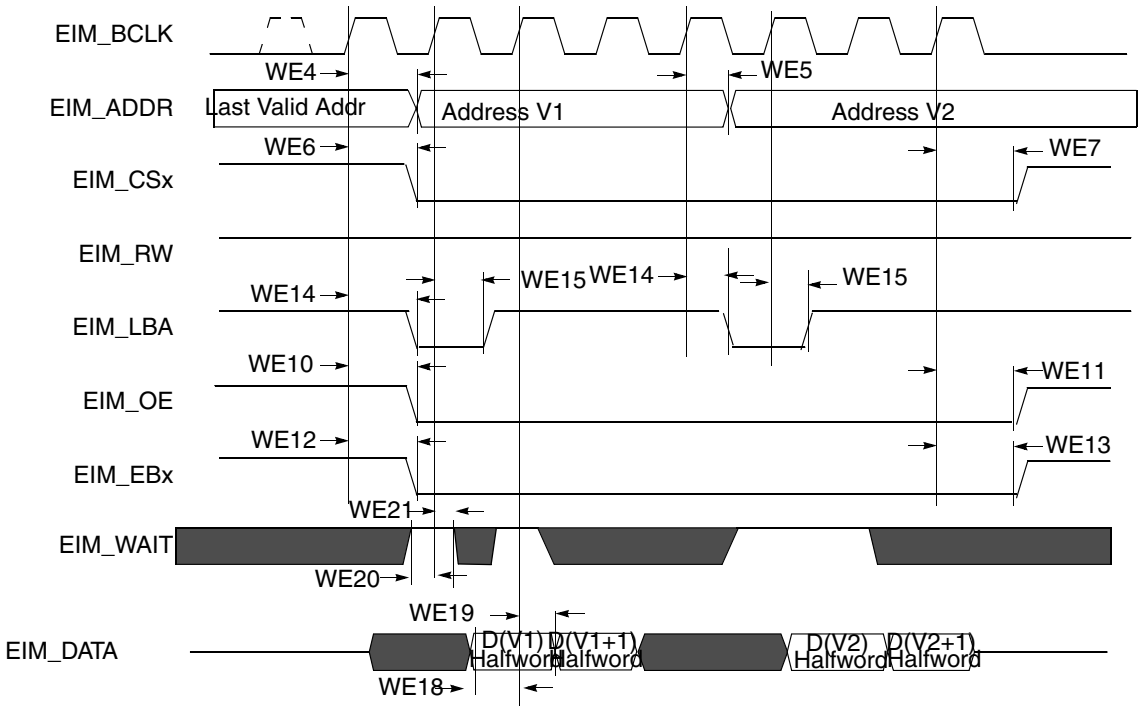


Figure 21. Synchronous 16-Bit Memory, Two Non-Sequential 32-Bit Read Accesses, WSC=2, SRD=1, BCD=0

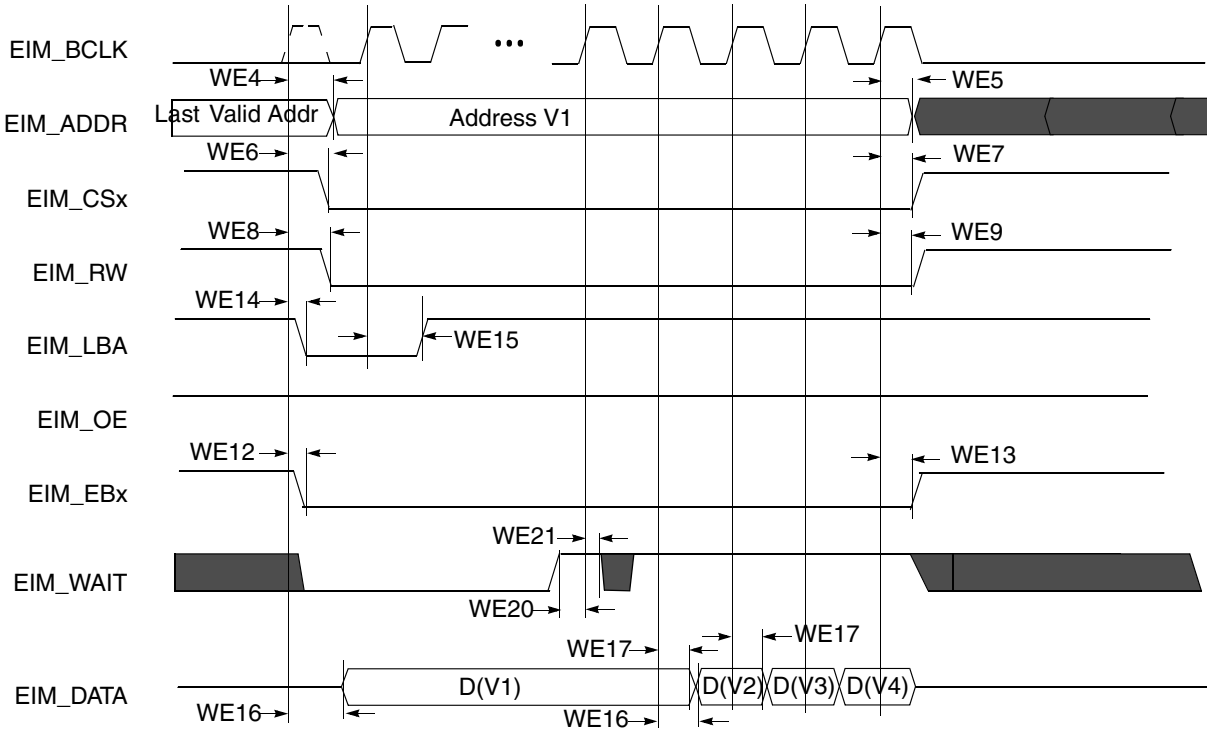


Figure 22. Synchronous Memory, Burst Write, BCS=1, WSC=4, SRD=1, and BCD=0

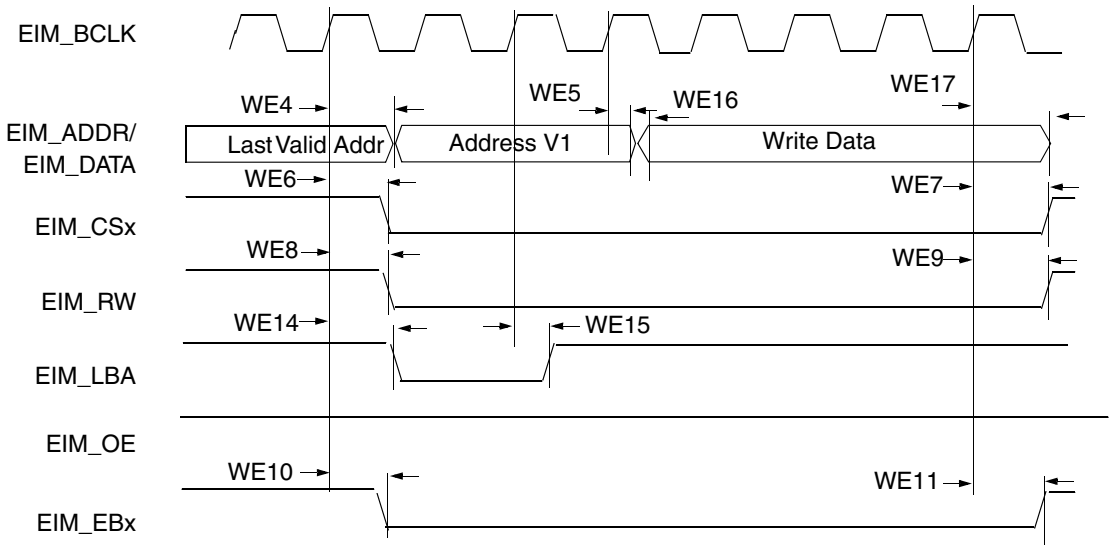


Figure 23. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=1, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode, the 16 MSBs are driven on the data bus.

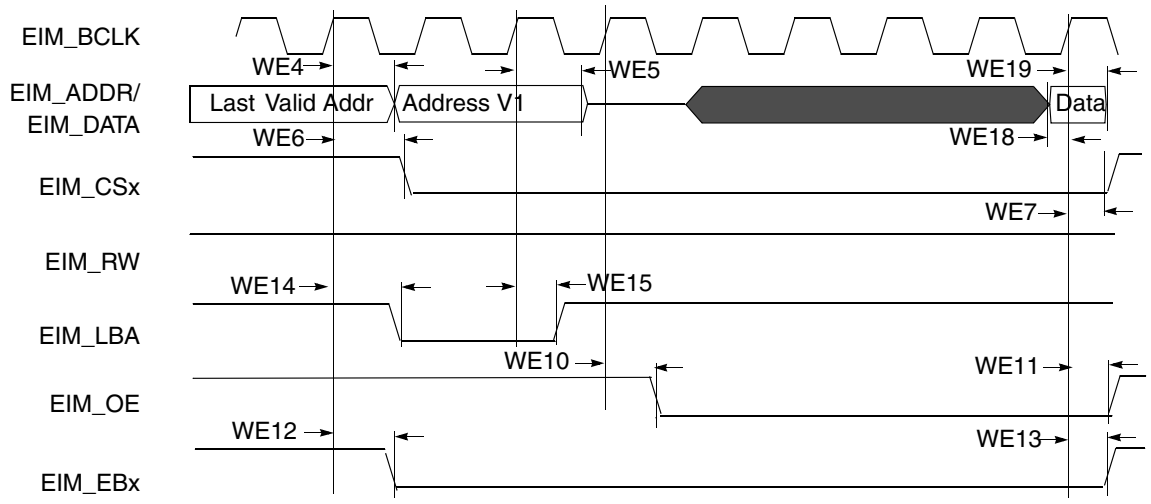


Figure 24. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=2

Figure 25, Figure 26, Figure 27, and Table 41 help to determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

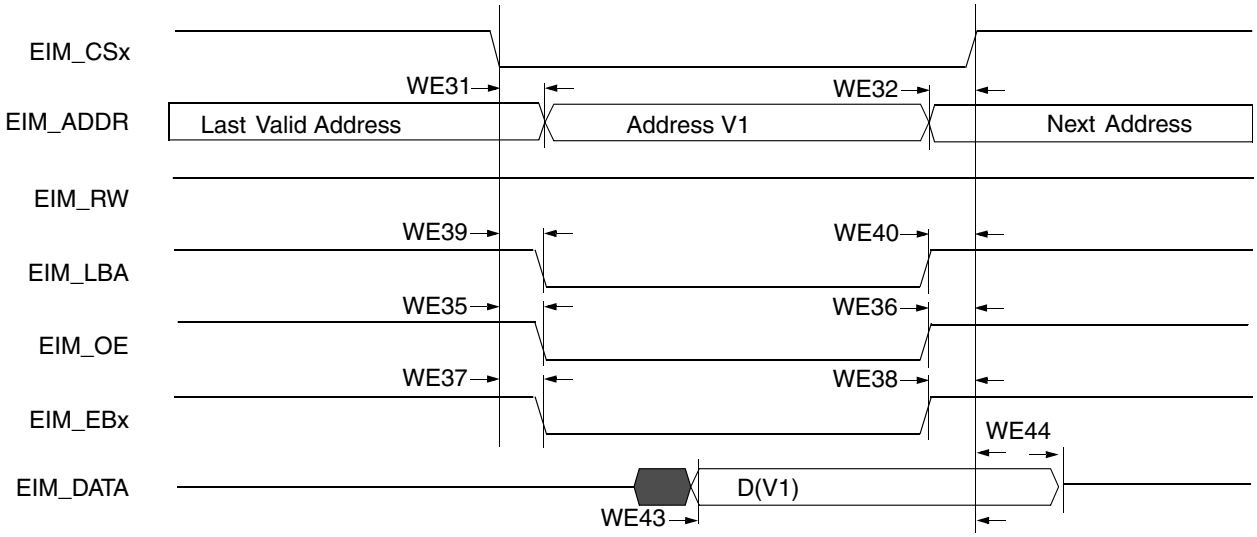


Figure 25. Asynchronous Memory Read Access

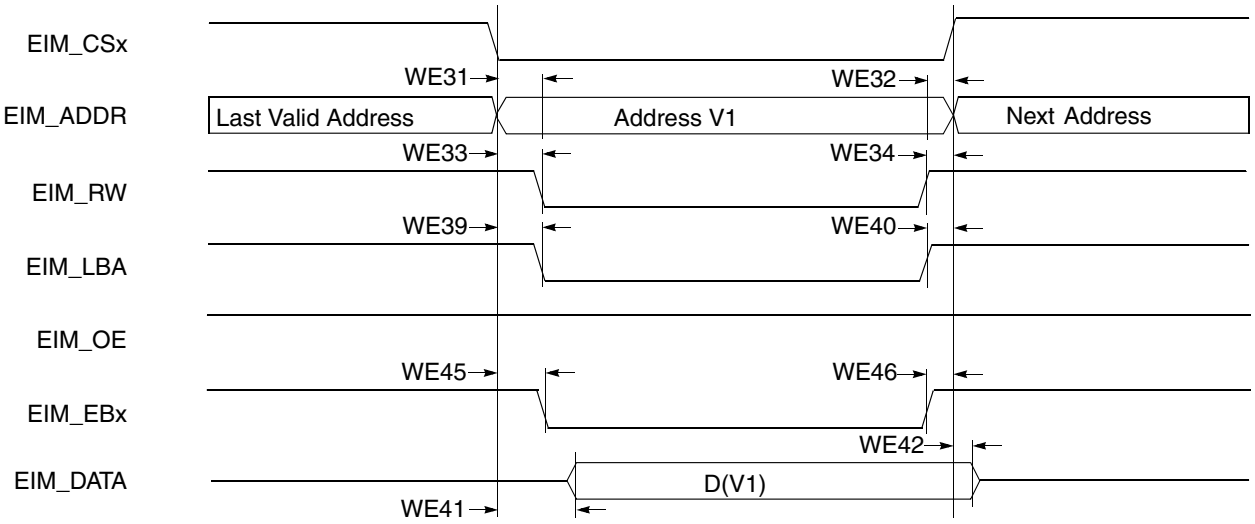


Figure 26. Asynchronous Memory Write Access

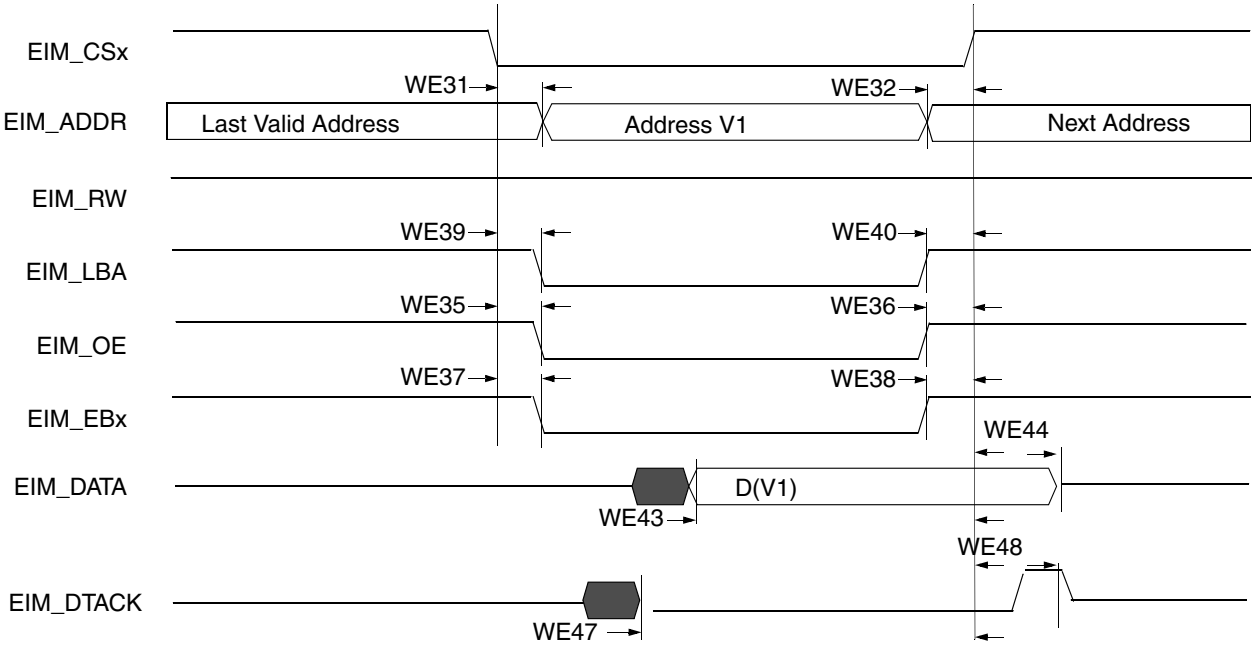


Figure 27. DTACK Read Access

Table 41. EIM Asynchronous Timing Parameters Table Relative Chip Select

ID	Parameter	Determination by Synchronous Measured Parameters [1]	Min	Max	Unit
WE31	EIM_CSx valid to Address valid	WE4 – WE6 – CSA[2]	—	3 – CSA	ns
WE32	Address invalid to EIM_CSx invalid	WE7 – WE5 – CSN[3]	—	3 – CSN	ns
WE33	EIM_CSx valid to EIM_RW valid	WE8 – WE6 + (WEA – CSA)	—	3 + (WEA – CSA)	ns

Table 41. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

ID	Parameter	Determination by Synchronous Measured Parameters [1]	Min	Max	Unit
WE34	EIM_RW invalid to EIM_CSx invalid	WE7 – WE9 + (WEN – CSN)	—	3 – (WEN_CSN)	ns
WE35	EIM_CSx valid to EIM_OE valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE36	EIM_OE invalid to EIM_CSx invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	EIM_CSx valid to EIM_EBx valid (Read access)	WE12 – WE6 + (RBEA – CSA)	—	3 + (RBEA[4] – CSA)	ns
WE38	EIM_EBx invalid to EIM_CSx invalid (Read access)	WE7 – WE13 + (RBEN – CSN)	—	3 – (RBEN[5] – CSN)	ns
WE39	EIM_CSx valid to EIM_LBA valid	WE14 – WE6 + (ADV – CSA)	—	3 + (ADVA – CSA)	ns
WE40	EIM_LBA invalid to EIM_CSx invalid (ADVL is asserted)	WE7 – WE15 – CSN	—	3 – CSN	ns
WE41	EIM_CSx valid to Output Data valid	WE16 – WE6 – WCSA	—	3 – WCSA	ns
WE42	Output Data invalid to EIM_CSx invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data valid to EIM_CSx invalid	MAXCO + MAXDI	MAXCO[6] + MAXDI[7]	—	ns
WE44	EIM_CSx invalid to Input Data invalid	0	0	—	ns
WE45	EIM_CSx valid to EIM_EBx valid (Write access)	WE12 – WE6 + (WBEA – CSA)	—	3 + (WBEA – CSA)	ns
WE46	EIM_EBx invalid to EIM_CSx invalid (Write access)	WE7 – WE13 + (WBEN – CSN)	—	–3 + (WBEN – CSN)	ns
WE47	EIM_DTACK valid to EIM_CSx invalid	MAXCO + MAXDTI	MAXCO[6] + MAXDTI[8]	—	ns
WE48	EIM_CSx invalid to EIM_DTACK invalid	0	0	—	ns

1 Parameters WE4–WE21 value, see in the Table 41.

2 EIM_CSx Assertion. This bit field determines when EIM_CSx signal is asserted during read/write cycles.

3 EIM_CSx Negation. This bit field determines when EIM_CSx signal is negated during read/write cycles.

4 EIM_EBx Assertion. This bit field determines when EIM_EBx signal is asserted during read cycles.

5 EIM_EBx Negation. This bit field determines when EIM_EBx signal is negated during read cycles.

6 Output maximum delay from internal driving the FFs to chip outputs. The maximum delay between all memory controls (EIM_ADDR, EIM_CSx, EIM_OE, EIM_RW, EIM_EBx, and EIM_LBA).

7 Maximum delay from chip input data to internal FFs. The maximum delay between all data input pins.

8 DTACK maximum delay from chip input data to internal FF.

4.8 DRAM Timing Parameters

This section includes descriptions of the electrical specifications of DRAM MC module which interfaces external DDR2, LPDDR1, and LPDDR2 memory devices.

4.8.1 DRAM Command & Address Output Timing—DDR2 and LPDDR1

The following diagrams and tables specify the timings related to the address and command pins, which interfaces DDR2 and LPDDR1 memory devices.

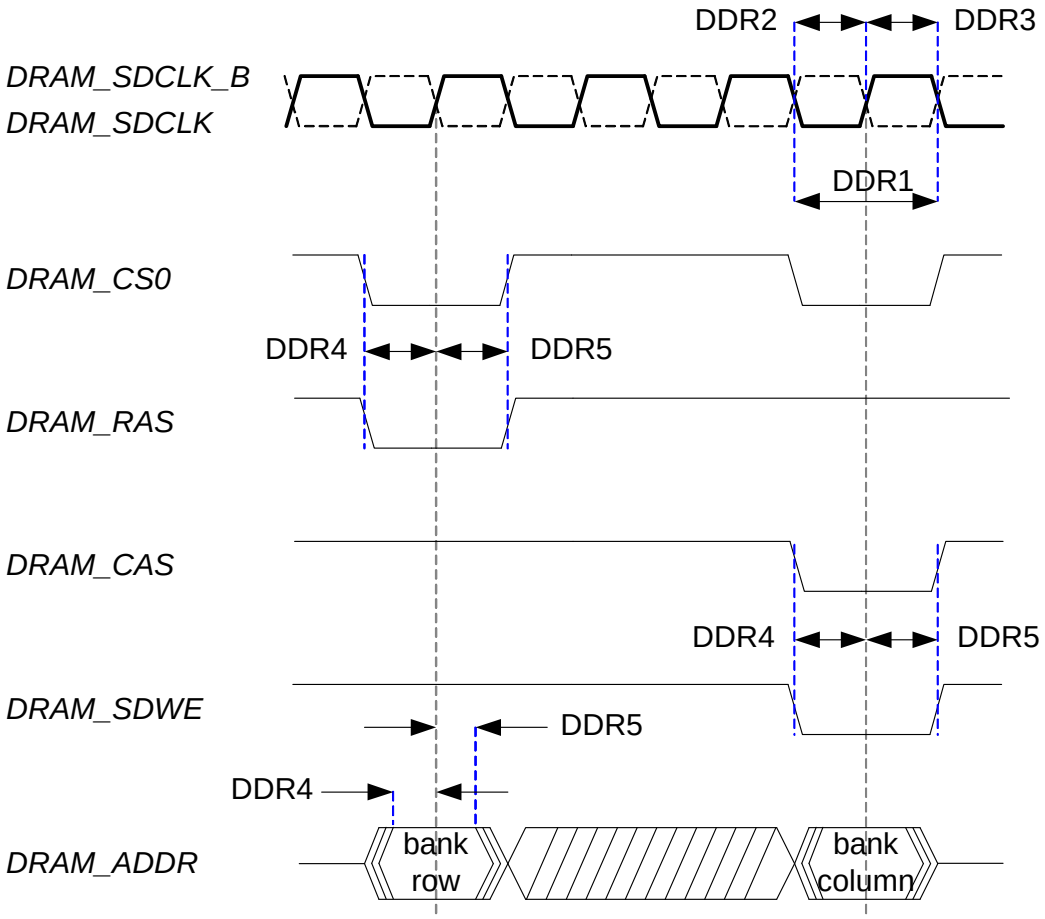


Figure 28. DRAM Command/Address Output Timing—DDR2 and LPDDR1

Table 42. EMI Command/Address AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR1	CK cycle time	tCK	3.75	—	ns
DDR2	CK high level width	tCH	0.48 tCK	0.52 tCK	ns

Table 42. EMI Command/Address AC Timing (continued)

ID	Description	Symbol	Min	Max	Unit
DDR3	CK low level width	tCL	0.48 tCK	0.52 tCK	ns
DDR4	Address and control output setup time	tIS	0.5 tCK - 0.3	—	ns
DDR5	Address and control output hold time	tIH	0.5 tCK - 0.3	—	ns

4.8.2 DRAM Command and Address Output Timing—LPDDR2

The following diagrams and tables specify the timings related to the address and command pins, which interface LPDDR2 memory devices.

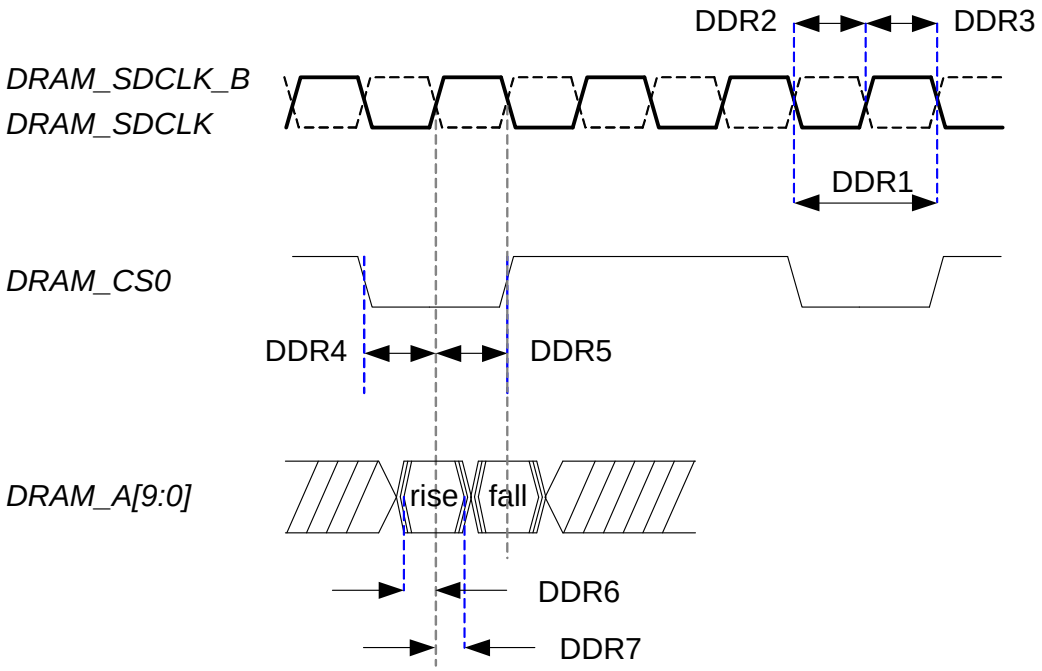


Figure 29. DRAM Command/Address Output Timing—LPDDR2

Table 43. EMI Command/Address AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR1	CK cycle time	tCK	3.75	—	ns
DDR2	CK high level width	tCH	0.48 tCK	0.52 tCK	ns
DDR3	CK low level width	tCL	0.48 tCK	0.52 tCK	ns
DDR4	Control output setup time	tIS	0.5 tCK - 0.3	—	ns

Table 43. EMI Command/Address AC Timing (continued)

ID	Description	Symbol	Min	Max	Unit
DDR5	Control output hold time	tIH	0.5 tCK - 0.3	—	ns
DDR6 CK >= 200 MHz	Address output setup time	tIS	0.5 tCK - 1.3	—	ns
DDR7 CK >= 200 MHz	Address output hold time	tIH	0.5 tCK - 1.3	—	ns
DDR6 CK < 200 MHz	Address output setup time	tIS	1	—	ns
DDR7 CK < 200 MHz	Address output hold time	tIH	1	—	ns

NOTE

DDR6 and DDR7 can be adjusted by the parameter -DLL_WR_DELAY-;

The ideal case is that SDCLK is center aligned to the DRAM_A[9:0] data valid window;

For this table, HW_DRAM_PHY23[14:8] (DLL_WR_DELAY) = 0x10;

4.8.3 DRAM Data Output Timing

The DRAM data output timing is defined for all DDR types: DDR2, LPDDR1, and LPDDR2.

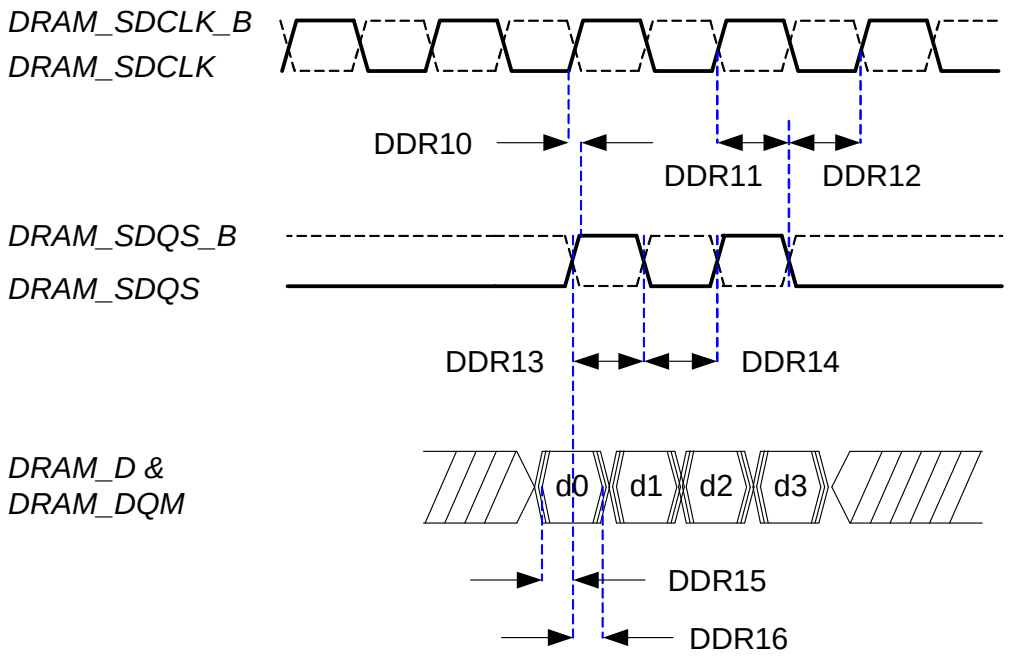


Figure 30. DRAM Data Output Timing

Table 44. DDR Output AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR10	Positive DQS latching edge to associated CK edge	tDQSS	-0.3	0.3	ns
DDR11	DQS falling edge from CK rising edge—hold time	tDSH	0.5 tCK - 0.3	0.5 tCK + 0.3	ns
DDR12	DQS falling edge to CK rising edge—setup time	tDSS	0.5 tCK - 0.3	0.5 tCK + 0.3	ns
DDR13	DQS output high pulse width	tDQSH	0.48 tCK	0.52 tCK	ns
DDR14	DQS output low pulse width	tDQSL	0.48 tCK	0.52 tCK	ns
DDR15 CK >= 200 MHz	DQ & DQM output setup time relative to DQS	tDS	0.5 tCK - 1.3	—	ns
DDR16 CK >= 200 MHz	DQ & DQM output hold time relative to DQS	tDH	0.5 tCK - 1.3	—	ns
DDR15 CK < 200 MHz	DQ & DQM output setup time relative to DQS	tDS	1	—	ns
DDR16 CK < 200 MHz	DQ & DQM output hold time relative to DQS	tDH	1	—	ns

NOTE

The DDR15,16 could be adjusted by the parameter “DLL_WR_DELAY”;

The ideal case is that SDQS is center aligned to the DRAM_D data valid window;

For this table, HW_DRAM_PHY15[14:8] (DLL_WR_DELAY) = 0x10;

4.8.4 DRAM Data Input Timing

DRAM Data input timing is defined for all DDR types: DDR2, LPDDR1, and LPDDR2.

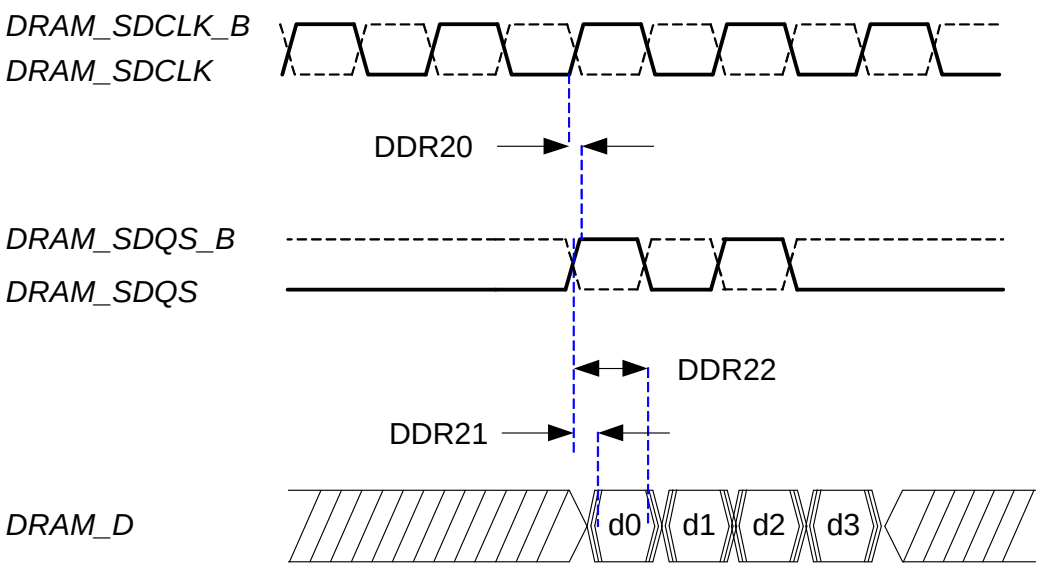


Figure 31. DRAM Data Input Timing

Table 45. DDR2 Input AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR20	Positive DQS latching edge to associated CK edge	tDQSCK	-0.5 tCK	—	ns
DDR21	DQS to DQ input skew	tDQSQ	—	0.65	ns
DDR22	DQS to DQ input hold time	tQH	0.45 tCK -0.85	—	ns

NOTE

The timing parameter DDR20(tDQSCK) is not strictly required by this DRAM MC design.

4.9 External Peripheral Interfaces

The following sections provide information on external peripheral interfaces.

4.9.1 AUDMUX Timing Parameters

The AUDMUX provides programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module.

4.9.2 CSPI and eCSPI Timing Parameters

This section describes the timing parameters of the CSPI and eCSPI modules. The CSPI and eCSPI have separate timing parameters for master and slave modes. The nomenclature used with the CSPI/eCSPI modules and the respective routing of these signals is shown in Table 46.

Table 46. CSPI Nomenclature and Routing

Module	I/O Access
eCSPI1	GPIO, KPP, DISP0_DAT, CSI0_DAT, and EIM_D through IOMUX
eCSPI2	DISP0_DAT, CSI0_DAT, and EIM through IOMUX
CSPI	DISP0_DAT, EIM_A/D, SD1, and SD2 through IOMUX

4.9.2.1 CSPI Master Mode Timing

Figure 32 depicts the timing of CSPI in master mode and Table 47 lists the CSPI master mode timing characteristics.

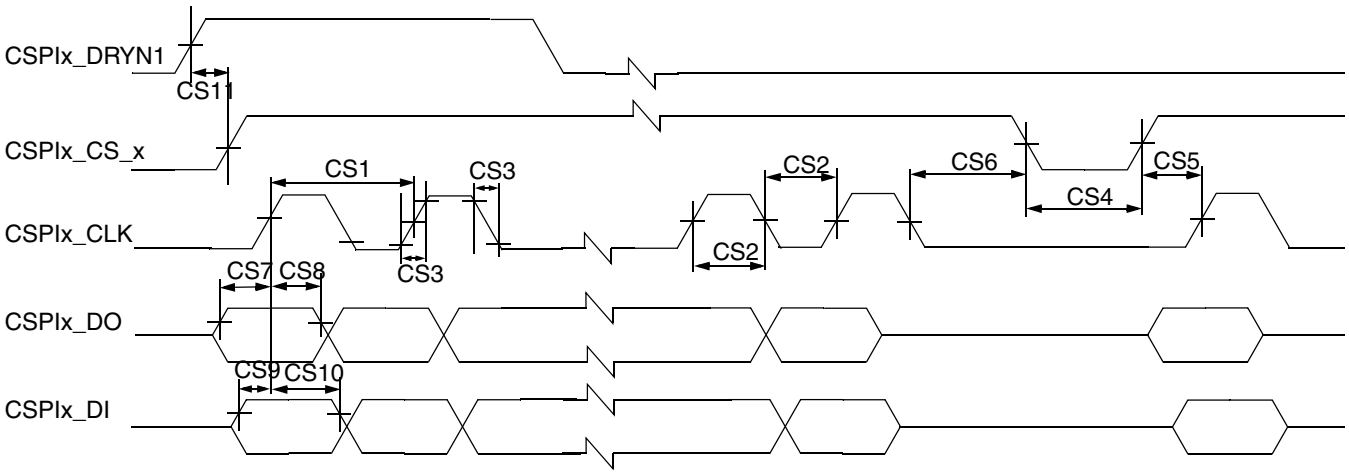


Figure 32. CSPI Master Mode Timing Diagram

Table 47. CSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	CSPIx_CLK Cycle Time	t_{clk}	60	—	ns
CS2	CSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	CSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	CSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	CSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	CSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	CSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	CSPIx_DO Hold Time	t_{Hmosi}	5	—	ns

Table 47. CSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS9	CSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	CSPIx_DI Hold Time	t_{Hmiso}	5	—	ns
CS11	CSPIx_DRYN Setup Time	t_{SDRY}	5	—	ns

4.9.2.2 CSPI Slave Mode Timing

Figure 33 depicts the timing of CSPI in slave mode. Table 48 lists the CSPI slave mode timing characteristics.

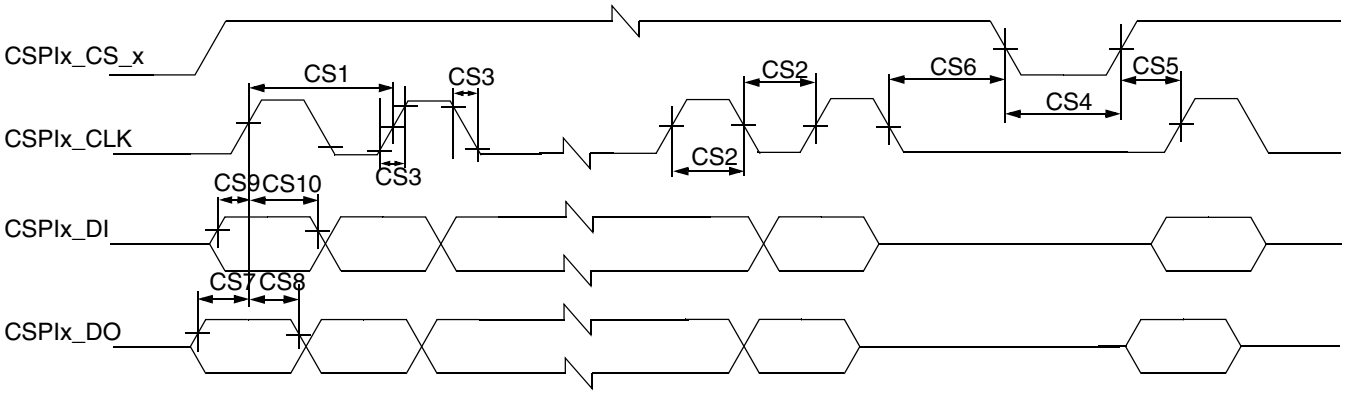


Figure 33. CSPI Slave Mode Timing Diagram

Table 48. CSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	CSPIx_CLK Cycle Time	t_{clk}	60	—	ns
CS2	CSPIx_CLK High or Low Time	t_{SW}	15	—	ns
CS3	CSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	CSPIx_CS_x pulse width	t_{CSLH}	30	—	ns
CS5	CSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	CSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	CSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	CSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	CSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	CSPIx_DI Hold Time	t_{Hmiso}	5	—	ns

4.9.2.3 eCSPI Master Mode Timing

Figure 34 depicts the timing of eCSPI in master mode and Table 49 lists the eCSPI master mode timing characteristics.

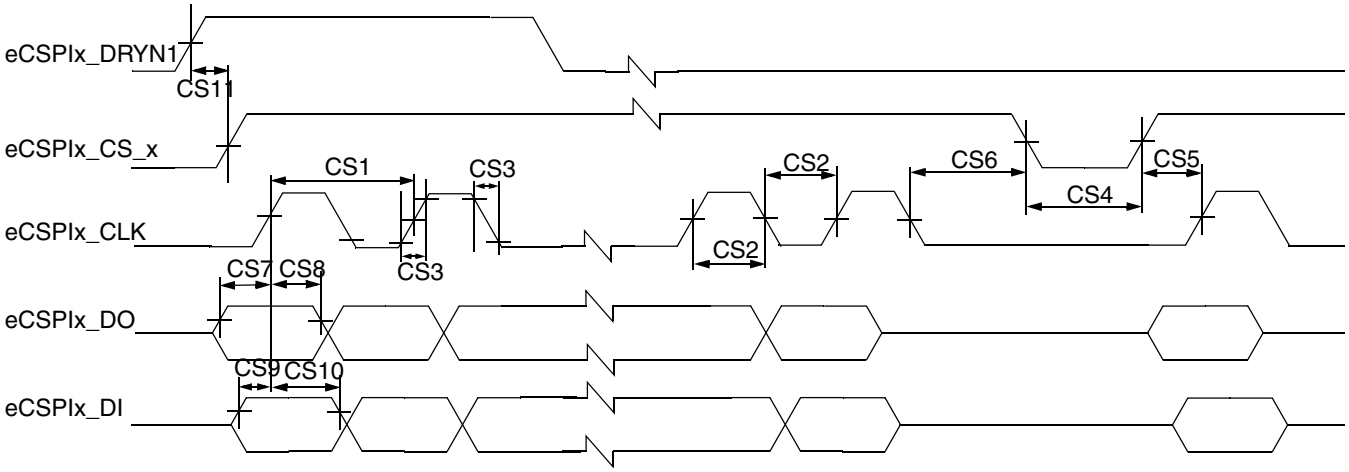


Figure 34. eCSPI Master Mode Timing Diagram

Table 49. eCSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns
CS11	eCSPIx_DRYN Setup Time	t_{SDRY}	5	—	ns

4.9.2.4 eCSPI Slave Mode Timing

Figure 35 depicts the timing of eCSPI in slave mode and Table 50 lists the eCSPI slave mode timing characteristics.

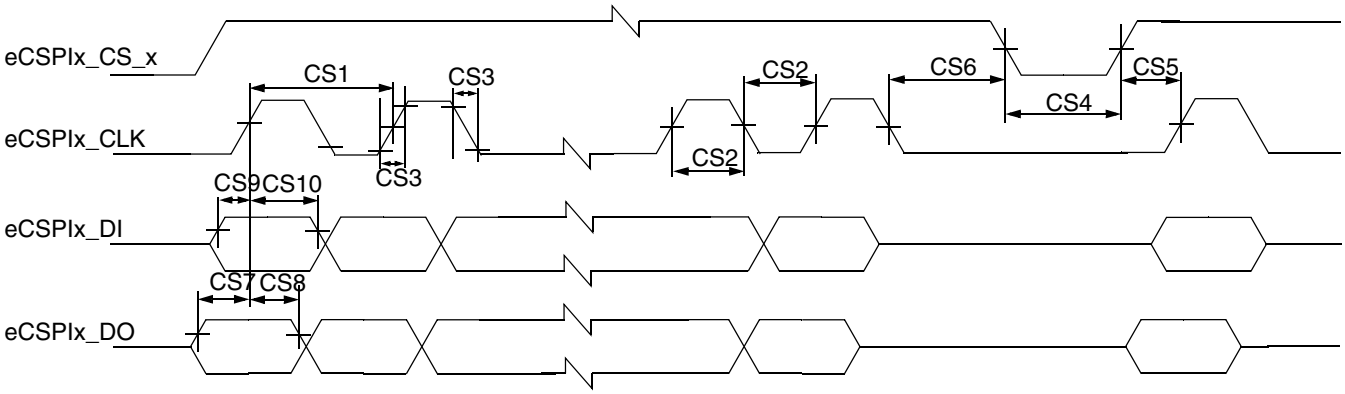


Figure 35. eCSPI Slave Mode Timing Diagram

Table 50. eCSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns

4.9.3 Enhanced Secured Digital Host Controller (eSDHCv2/v3) and uSDHC AC Timing

This section describes the electrical information of the eSDHCv2/v3 and the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Date Rate) timing.

4.9.3.1 SD/eMMC4.3 (Single Data Rate) eSDHCv3 and uSDHC AC Timing

Figure 36 depicts the timing of SD/eMMC4.3, and Table 51 lists the SD/eMMC4.3 timing characteristics.

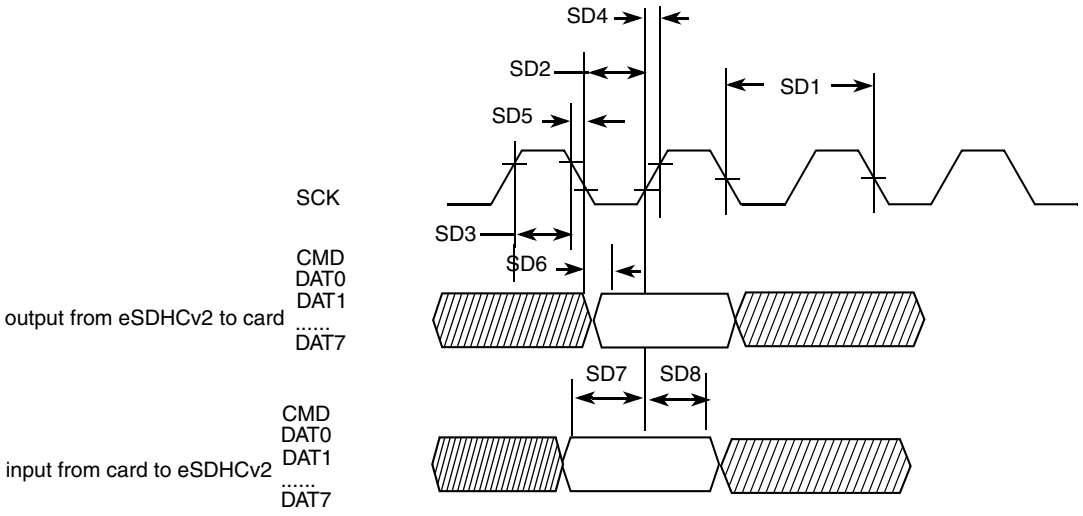


Figure 36. SD/eMMC4.3 Timing

Table 51. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
	Card Input Clock				
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns

Table 51. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC Output Delay	t_{OD}	–2	2	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	2.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.9.3.2 eMMC4.4 (Dual Data Rate) eSDHCv3 and uSDHC AC Timing

Figure 37 depicts the timing of eMMC4.4, and Table 52 lists the eMMC4.4 timing characteristics. Be aware that only DAT0-7 is sampled on both edges of clock (not applicable to CMD).

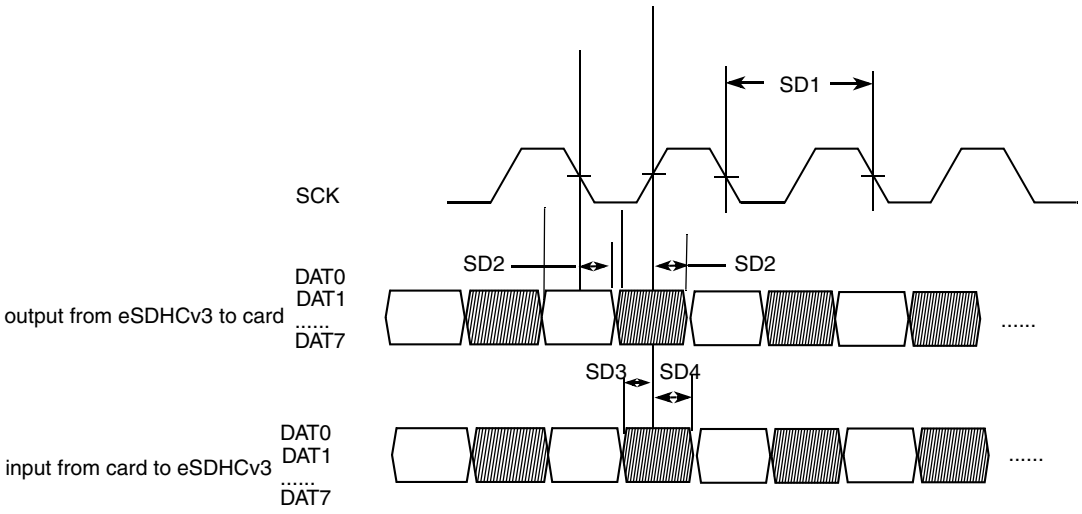


Figure 37. eMMC4.4 Timing

Table 52. eMMC4.4 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}	0	52	MHz
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					

Table 52. eMMC4.4 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD2	eSDHC Output Delay	t_{OD}	–5	5	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD3	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD4	eSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.9.4 FEC AC Timing Parameters

This section describes the AC timing specifications of the FEC. The i.MX50 FEC supports 10/100 Mbps RMII with MII serial management interface. The RMII and serial management signals are compatible with transceivers operating at a voltage of 3.3 V.

4.9.4.1 RMII Async Inputs Signal Timing (FEC_COL)

Table 53 lists RMII asynchronous inputs signal timing information. Figure 38 shows MII asynchronous input timings listed in Table 53.

Table 53. RMII Async Inputs Signal Timing

Num	Characteristics	Min	Max	Unit
M9	FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

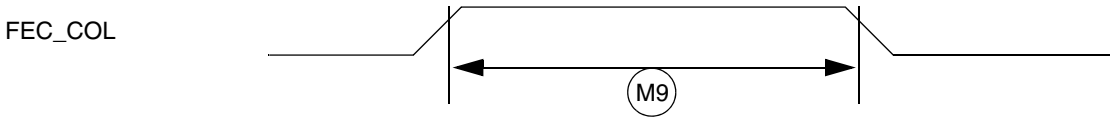


Figure 38. MII Async Inputs Timing Diagram

4.9.4.2 RMII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 54 lists RMII serial management channel timings. Figure 39 shows RMII serial management channel timings listed in Table 54. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 RMII specification. However, the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 54. RMII Transmit Signal Timing

ID	Characteristics	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns

Table 54. RMII Transmit Signal Timing (continued)

ID	Characteristics	Min	Max	Unit
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

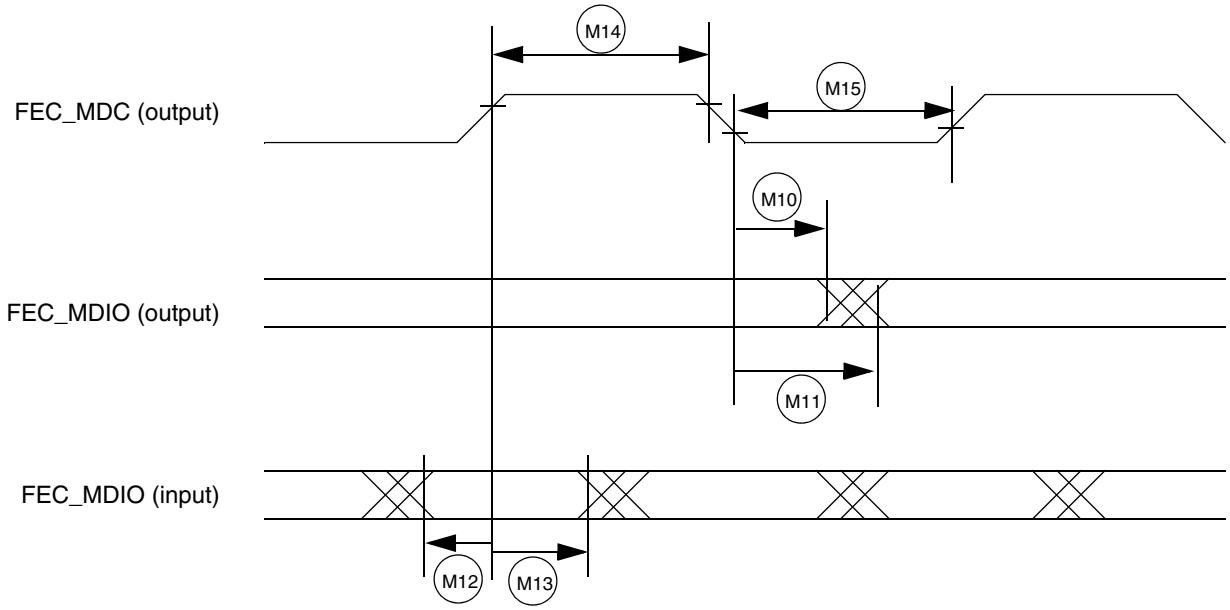


Figure 39. RMII Serial Management Channel Timing Diagram

4.9.4.3 RMII Mode Timing

In RMII mode, FEC_TX_CLK is used as the REF_CLK which is a 50 MHz ± 50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII, and other signals under RMII mode include FEC_TX_EN, FEC_TXD[1:0], FEC_RXD[1:0] and optional FEC_RX_ER.

The RMII mode timings are shown in Table 55 and Figure 40.

Table 55. RMII Signal Timing

No.	Characteristics	Min	Max	Unit
M16	REF_CLK(FEC_TX_CLK) pulse width high	35%	65%	REF_CLK period
M17	REF_CLK(FEC_TX_CLK) pulse width low	35%	65%	REF_CLK period
M18	REF_CLK to FEC_TXD[1:0], FEC_TX_EN invalid	2	—	ns
M19	REF_CLK to FEC_TXD[1:0], FEC_TX_EN valid	—	16	ns
M20	FEC_RXD[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup	4	—	ns
M21	REF_CLK to FEC_RXD[1:0], FEC_RX_DV, FEC_RX_ER hold	2	—	ns

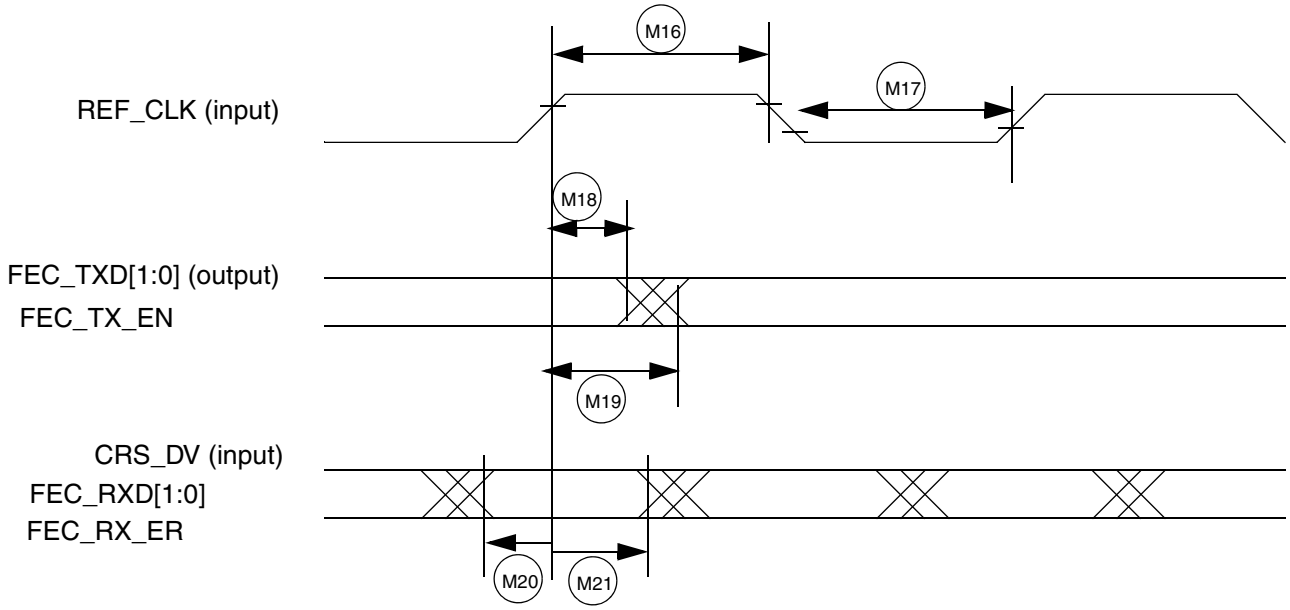


Figure 40. RMII Mode Signal Timing Diagram

4.9.5 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 41 depicts the timing of I²C module, and Table 56 lists the I²C module timing characteristics.

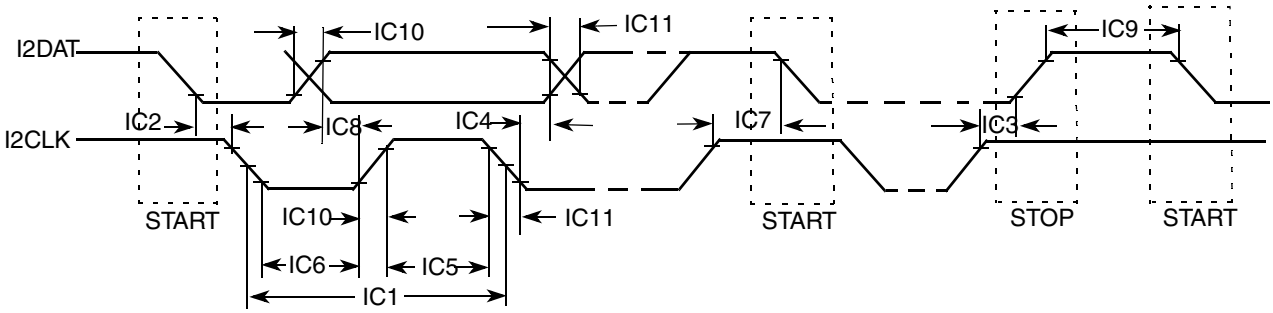


Figure 41. I²C Bus Timing

Table 56. I²C Module Timing Parameters

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs

Table 56. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.9.6 One-Wire (OWIRE) Timing Parameters

Figure 42 depicts the RPP timing, and Table 57 lists the RPP timing parameters.

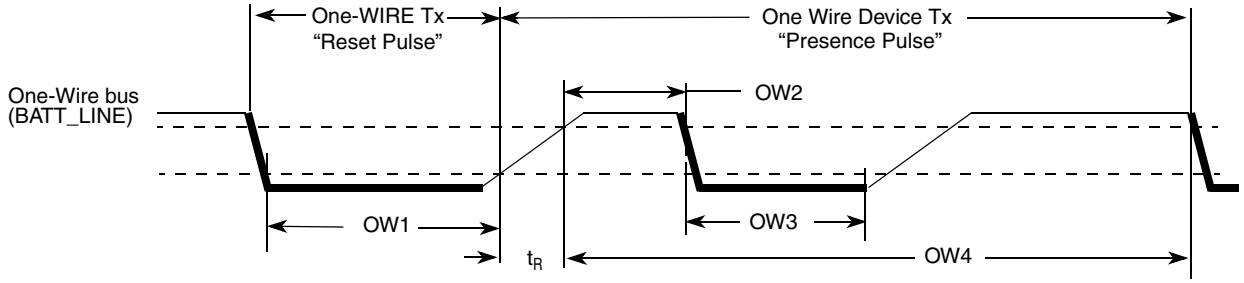


Figure 42. Reset and Presence Pulses (RPP) Timing Diagram

Table 57. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Unit
OW1	Reset Time Low	t_{RSTL}	480	511	—[1]	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High (includes recovery time)	t_{RSTH}	480	512	—	µs

[1] In order not to mask signaling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960 µs.

Figure 43 depicts Write 0 Sequence timing, and Table 58 lists the timing parameters.

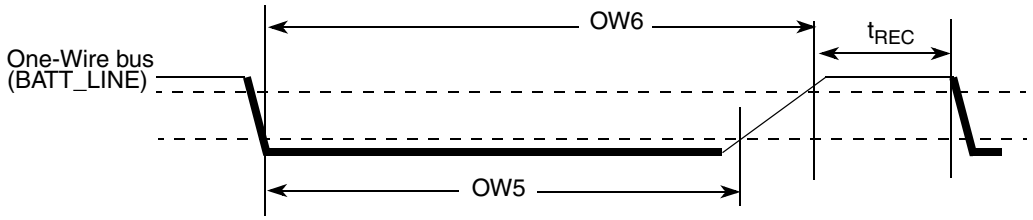


Figure 43. Write 0 Sequence Timing Diagram

Table 58. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW5	Write 0 Low Time	t_{LOW0}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs
—	Recovery time	t_{REC}	1	—	—	µs

Figure 44 depicts Write 1 Sequence timing, Figure 45 depicts the Read Sequence timing, and Table 59 lists the timing parameters.

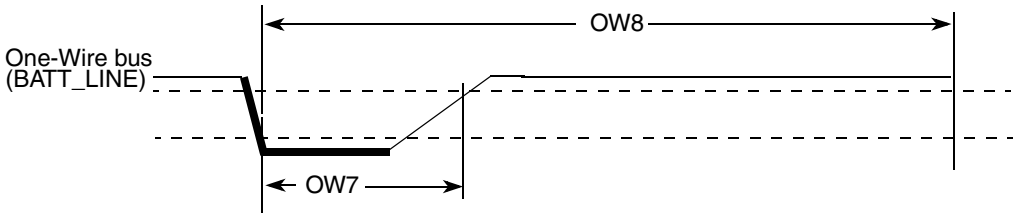


Figure 44. Write 1 Sequence Timing Diagram

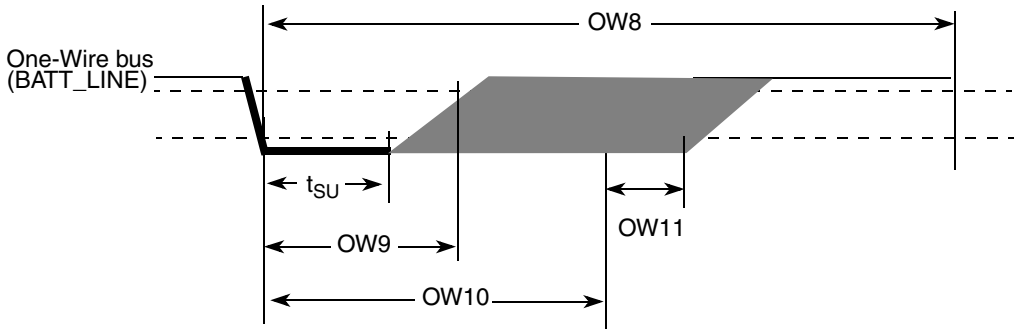


Figure 45. Read Sequence Timing Diagram

Table 59. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW7	Write 1 Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
—	Read Data Setup	t_{SU}	—	—	1	µs
OW9	Read Low Time	t_{LOWR}	1	5	15	µs
OW10	Read Data Valid	t_{RDV}	—	15	—	µs
OW11	Release Time	$t_{RELEASE}$	0	—	45	µs

4.9.7 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 46 depicts the timing of the PWM, and Table 60 lists the PWM timing parameters.

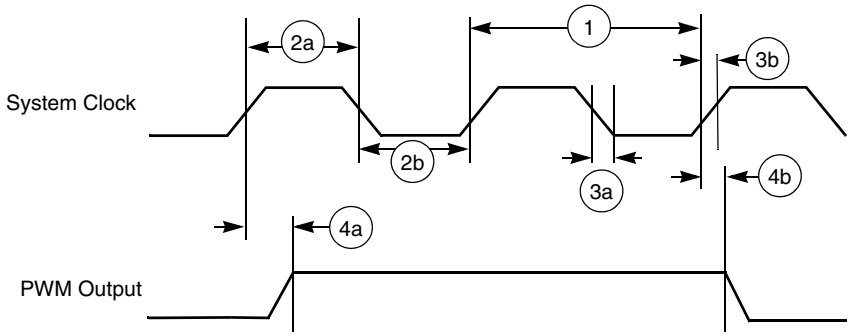


Figure 46. PWM Timing

Table 60. PWM Output Timing Parameter

Ref. No.	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

[1] CL of PWMO = 30 pF

4.9.8 Secure JTAG Controller (SJC) Timing Parameters

Figure 47 depicts the SJC test clock input timing. Figure 48 depicts the SJC boundary scan timing. Figure 49 depicts the SJC test access port. Figure 50 depicts the TRST timing. The signal parameters are listed in Table 61.

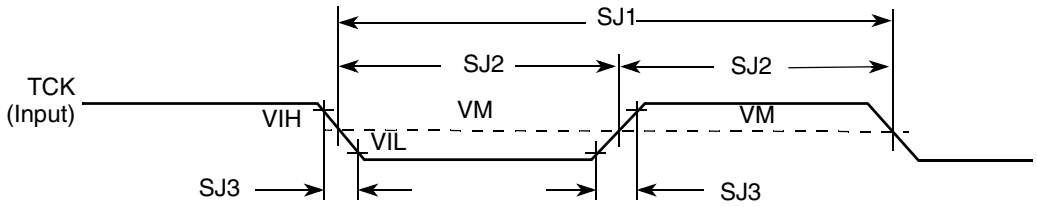


Figure 47. Test Clock Input Timing Diagram

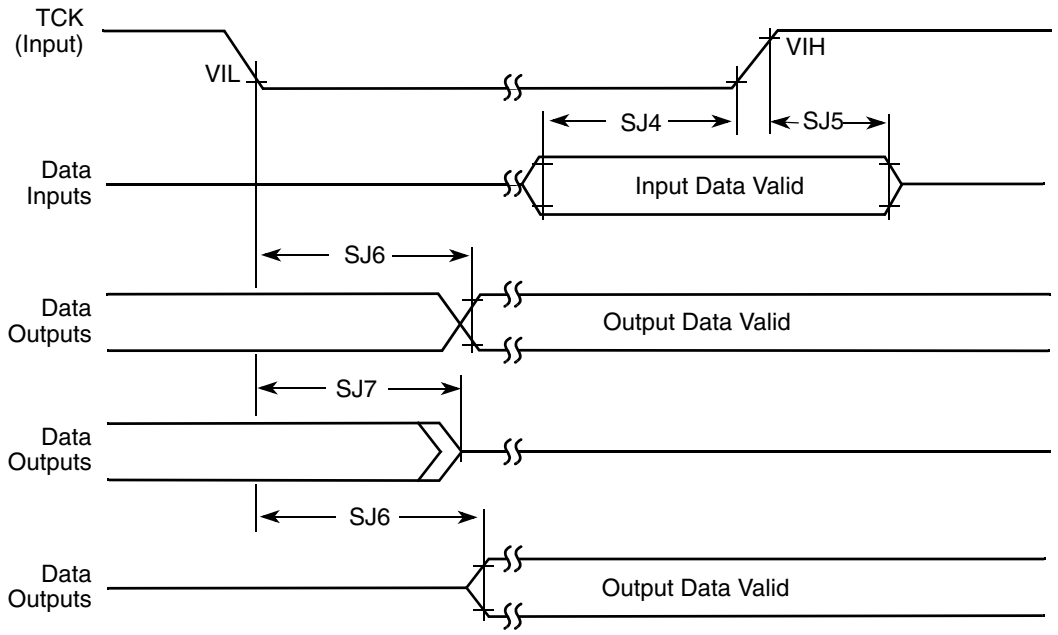


Figure 48. Boundary Scan (JTAG) Timing Diagram

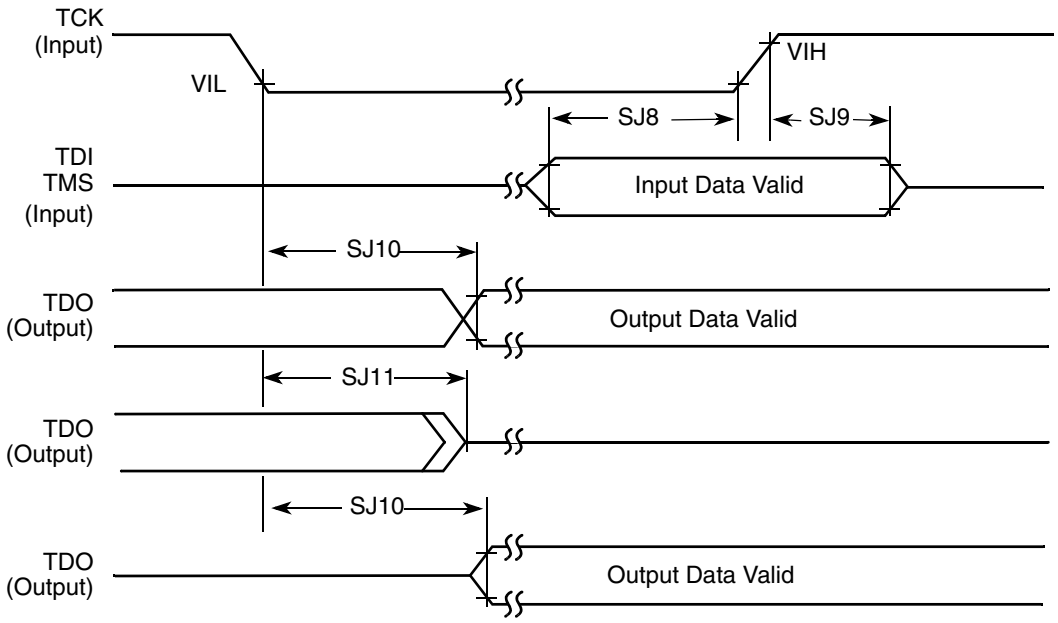


Figure 49. Test Access Port Timing Diagram

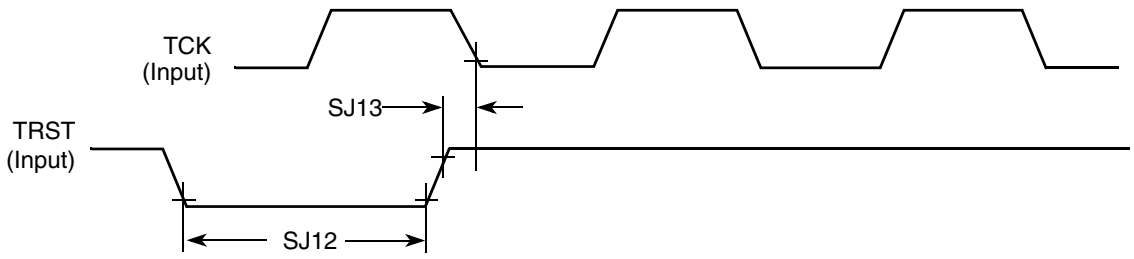


Figure 50. $\overline{\text{TRST}}$ Timing Diagram

Table 61. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.9.9 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 62.

Table 62. AUDMUX Port Allocation

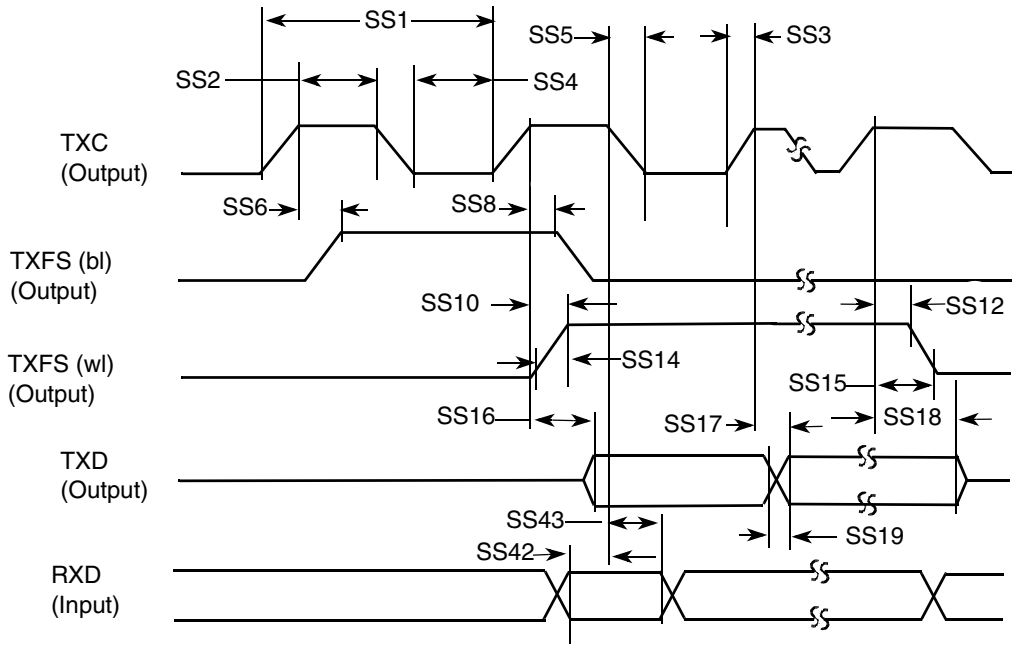
Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External— AUD3 I/O
AUDMUX port 4	AUD4	External—EIM or CSPI1 I/O through IOMUX
AUDMUX port 5	AUD5	External—EIM or SD1 I/O through IOMUX
AUDMUX port 6	AUD6	External—EIM or DISP2 through IOMUX

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

4.9.9.1 SSI Transmitter Timing with Internal Clock

Figure 51 depicts the SSI transmitter internal clock timing and Table 63 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only

Figure 51. SSI Transmitter Internal Clock Timing Diagram

Table 63. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns

Table 63. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6.0	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns
SS52	Loading	—	25.0	pF

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- Tx and Rx refer to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.9.9.2 SSI Receiver Timing with Internal Clock

Figure 52 depicts the SSI receiver internal clock timing and Table 64 lists the timing parameters for the receiver timing with internal clock.

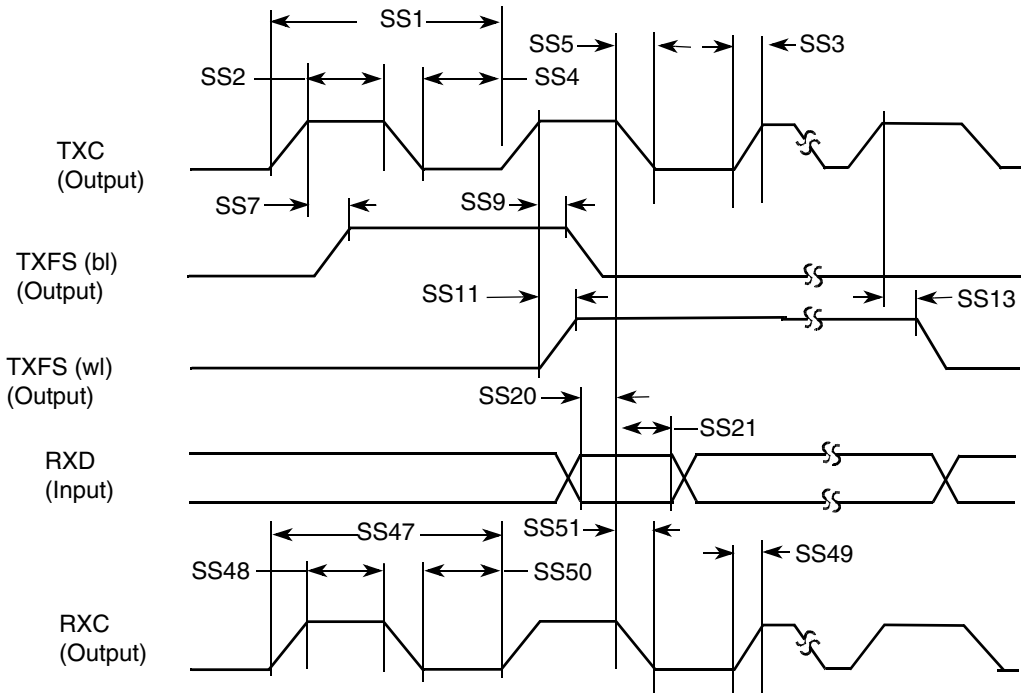


Figure 52. SSI Receiver Internal Clock Timing Diagram

Table 64. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns

Table 64. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS as shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- **Tx** and **Rx** refer to the transmit and receive sections of the SSI.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- For internal frame sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.9.9.3 SSI Transmitter Timing with External Clock

Figure 53 depicts the SSI transmitter external clock timing and Table 65 lists the timing parameters for the transmitter timing with external clock.

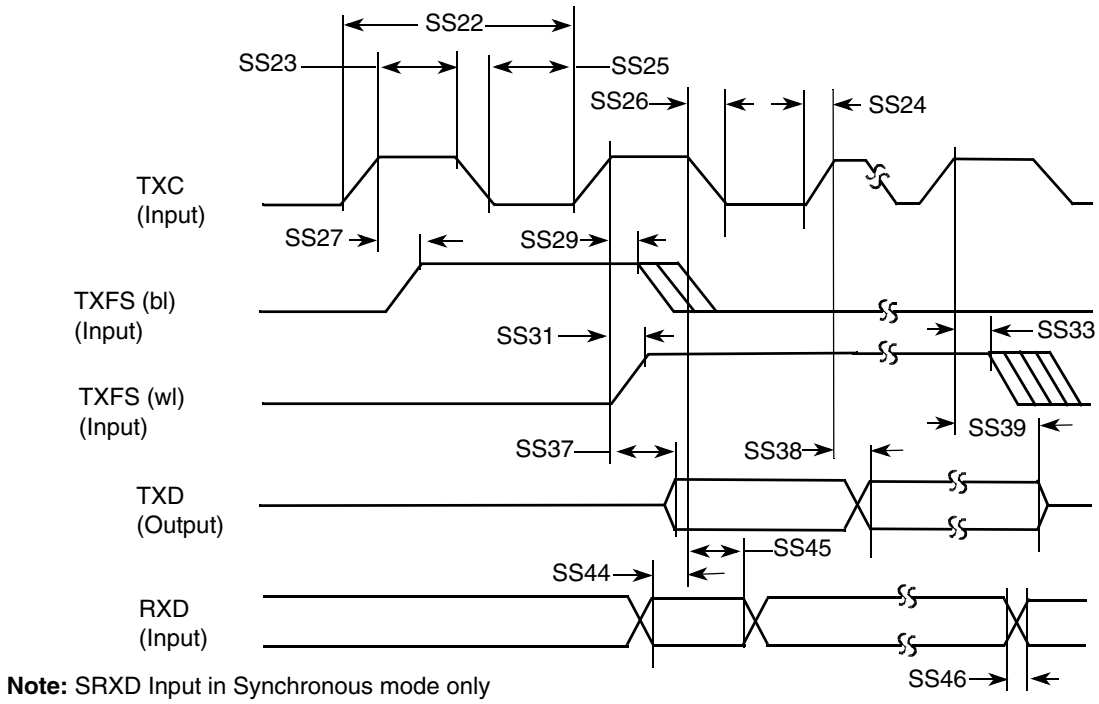


Figure 53. SSI Transmitter External Clock Timing Diagram

Table 65. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

Table 65. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- Tx and Rx refer to the transmit and receive sections of the SSI.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- For internal frame sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.9.9.4 SSI Receiver Timing with External Clock

Figure 54 depicts the SSI receiver external clock timing and Table 66 lists the timing parameters for the receiver timing with external clock.

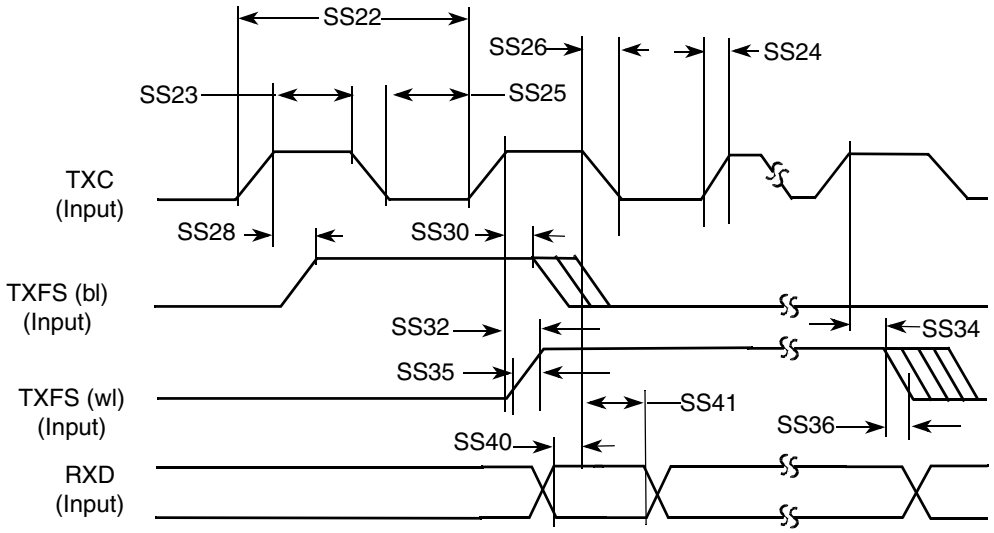


Figure 54. SSI Receiver External Clock Timing Diagram

Table 66. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	–10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- Tx and Rx refer to the transmit and receive sections of the SSI.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.9.10 UART I/O Configuration and Timing Parameters

The following sections describe the UART I/O configuration and timing parameters.

4.9.10.1 UART RS-232 I/O Configuration in Different Modes

Table 67 shows the UART I/O configuration based on which mode is enabled.

Table 67. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.9.10.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.9.10.2.1 UART Transmitter

Figure 55 depicts the transmit timing of UART in the RS-232 serial mode with 8 data bit/1 stop bit format. Table 68 lists the UART RS-232 serial mode transmit timing characteristics.

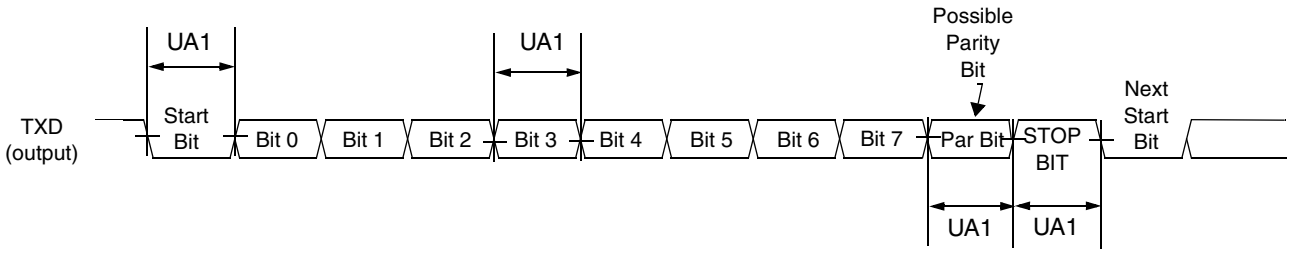


Figure 55. UART RS-232 Serial Mode Transmit Timing Diagram

Table 68. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.10.2.2 UART Receiver

Figure 56 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 69 lists serial mode receive timing characteristics.

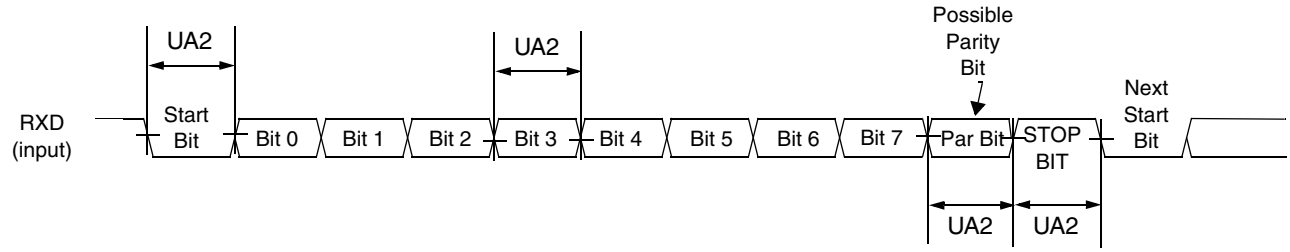


Figure 56. UART RS-232 Serial Mode Receive Timing Diagram

Table 69. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] – $1/(16*F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16*F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16*F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.9.10.3 UART IrDA Mode Timing

The following sections give the UART transmit and receive timings in IrDA mode.

4.9.10.3.1 UART IrDA Mode Transmitter

Figure 57 depicts the UART IrDA mode transmit timing with 8 data bit/1 stop bit format. Table 70 lists the transmit timing characteristics.

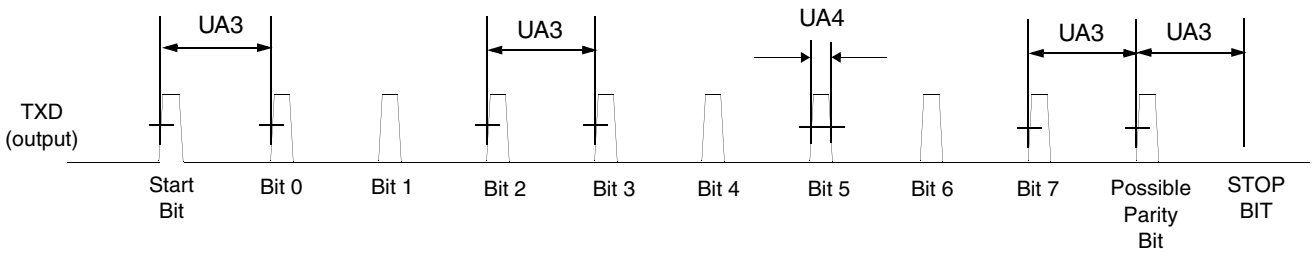


Figure 57. UART IrDA Mode Transmit Timing Diagram

Table 70. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)*(1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16)*(1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.10.3.2 UART IrDA Mode Receiver

Figure 58 depicts the UART IrDA mode receive timing with 8 data bit/1 stop bit format. Table 71 lists the receive timing characteristics.

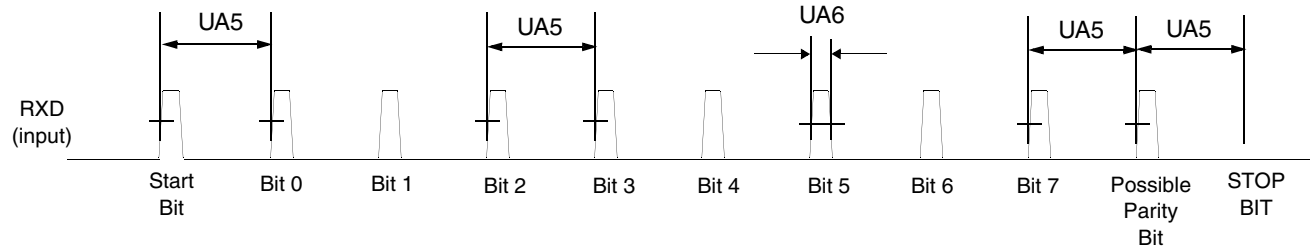


Figure 58. UART IrDA Mode Receive Timing Diagram

Table 71. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$ [2] – $1/(16*F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16*F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16)*(1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16*F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.9.11 USB PHY Parameters

This section describes the USB OTG PHY and the USB host port PHY parameters.

4.9.11.1 USB PHY AC Parameters

Table 72 lists the AC timing parameters for USB PHY.

Table 72. USB PHY AC Timing Parameters

Parameter	Conditions	Min	Typ	Max	Unit
trise	1.5Mbps 12Mbps 480Mbps	75 4 0.5	—	300 20	ns
tfall	1.5Mbps 12Mbps 480Mbps	75 4 0.5	—	300 20	ns
Jitter	1.5Mbps 12Mbps 480Mbps	—	—	10 1 0.2	ns

4.9.11.2 USB PHY Additional Electrical Parameters

Table 73 lists the parameters for additional electrical characteristics for USB PHY.

Table 73. Additional Electrical Characteristics for USB PHY

Parameter	Conditions	Min	Typ	Max	Unit
Vcm DC (dc level measured at receiver connector)	HS Mode LS/FS Mode	–0.05 0.8	—	0.5 2.5	V
Crossover Voltage	LS Mode FS Mode	1.3 1.3	—	2 2	V
Power supply ripple noise (analog 3.3 V)	< 160 MHz	–50	0	50	mV
Power supply ripple noise (analog 2.5 V)	< 1.2 MHz > 1.2 MHz	–10 –50	0 0	10 50	mV
Power supply ripple noise (Digital 1.2 V)	All conditions	–50	0	50	mV

4.9.11.3 USB PHY System Clocking (SYSCLK)

Table 74 lists the USB PHY system clocking parameters

Table 74. USB PHY System Clocking Parameters

Parameter	Conditions	Min	Typ	Max	Unit
Clock deviation	Reference Clock frequency 24 MHz	–150	—	150	ppm
Rise/fall time	—	—	—	200	ps

Table 74. USB PHY System Clocking Parameters (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Jitter (peak-peak)	<1.2 MHz	0	—	50	ps
Jitter (peak-peak)	>1.2 MHz	0	—	100	ps
Duty-cycle	Reference Clock frequency 24 MHz	40	—	60	%

4.9.11.4 USB VBUS Parameters

Table 75 lists the USB VBUS input parameters.

Table 75. VBUS Comparators Thresholds

Parameter	Conditions	Min	Typ	Max	Unit
A-Device Session Valid Comparator Threshold	—	0.8	1.4	2.0	V
B-Device Session Valid Comparator Threshold	—	0.8	1.4	4.0	V
B-Device Session End Comparator Threshold	—	0.2	0.45	0.8	V
VBUS Valid Comparator Threshold[1]	—	4.4	4.6	4.75	V
VBUS for CHRG_DET_B Operation	—	3.0	—	—	V
VBUS Input Current	VBUS = 5.25 V	—	—	500	μA

[1] For VBUS maximum rating, see Table 7.

5 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

5.1 416 MAPBGA 13 × 13 mm Package Information

This section contains the outline drawing, signal assignment map, ground, power, reference ID (by ball grid location) for the 13 × 13 mm, 0.5 mm pitch 416 Pin MAPBGA package.

5.1.1 Case 416 MAPBGA, 13 × 13 mm, 0.5 mm Pitch Package Views

Figure 59 shows the top view of the 13 × 13 mm package, Figure 60 shows the bottom view (416 soldier balls) of the 13 × 13 mm package, and Figure 61 shows the side view of the 13 × 13 mm package.

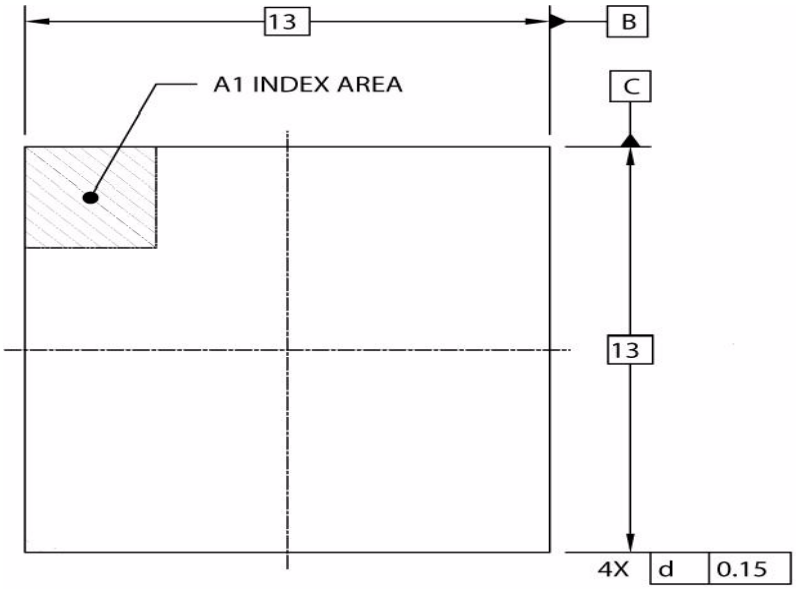


Figure 59. 416 Pin MAPBGA 13 × 13 mm Package Top View

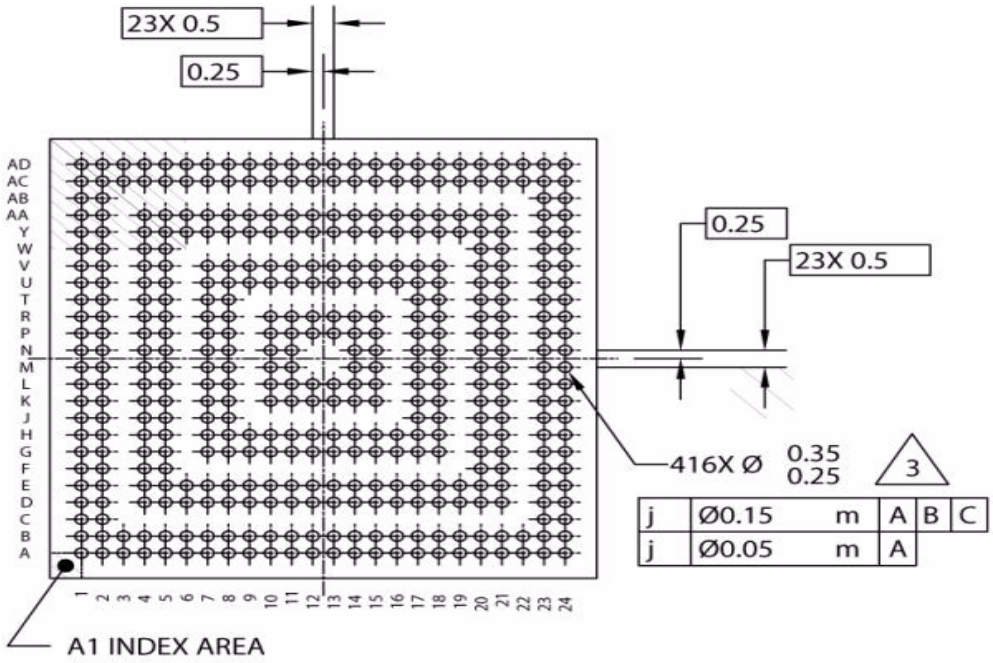


Figure 60. 416 Pin MAPBGA 13 × 13 mm Package Bottom View

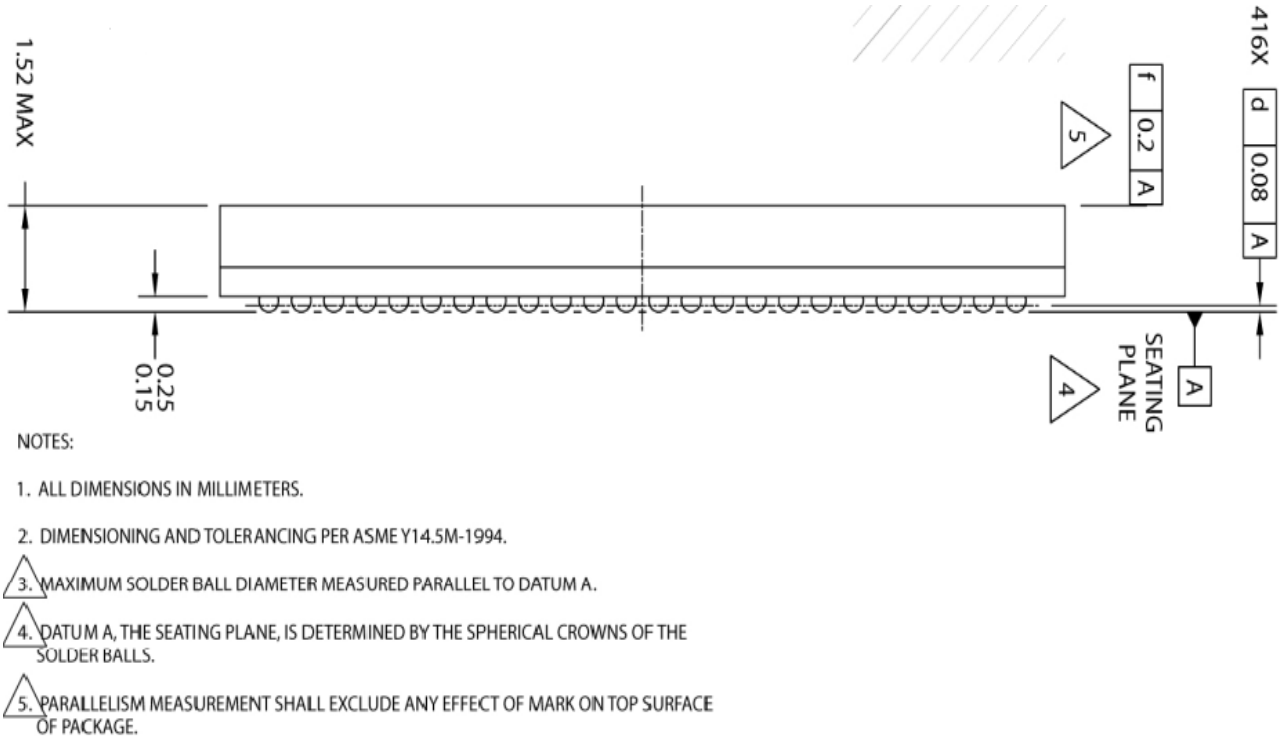


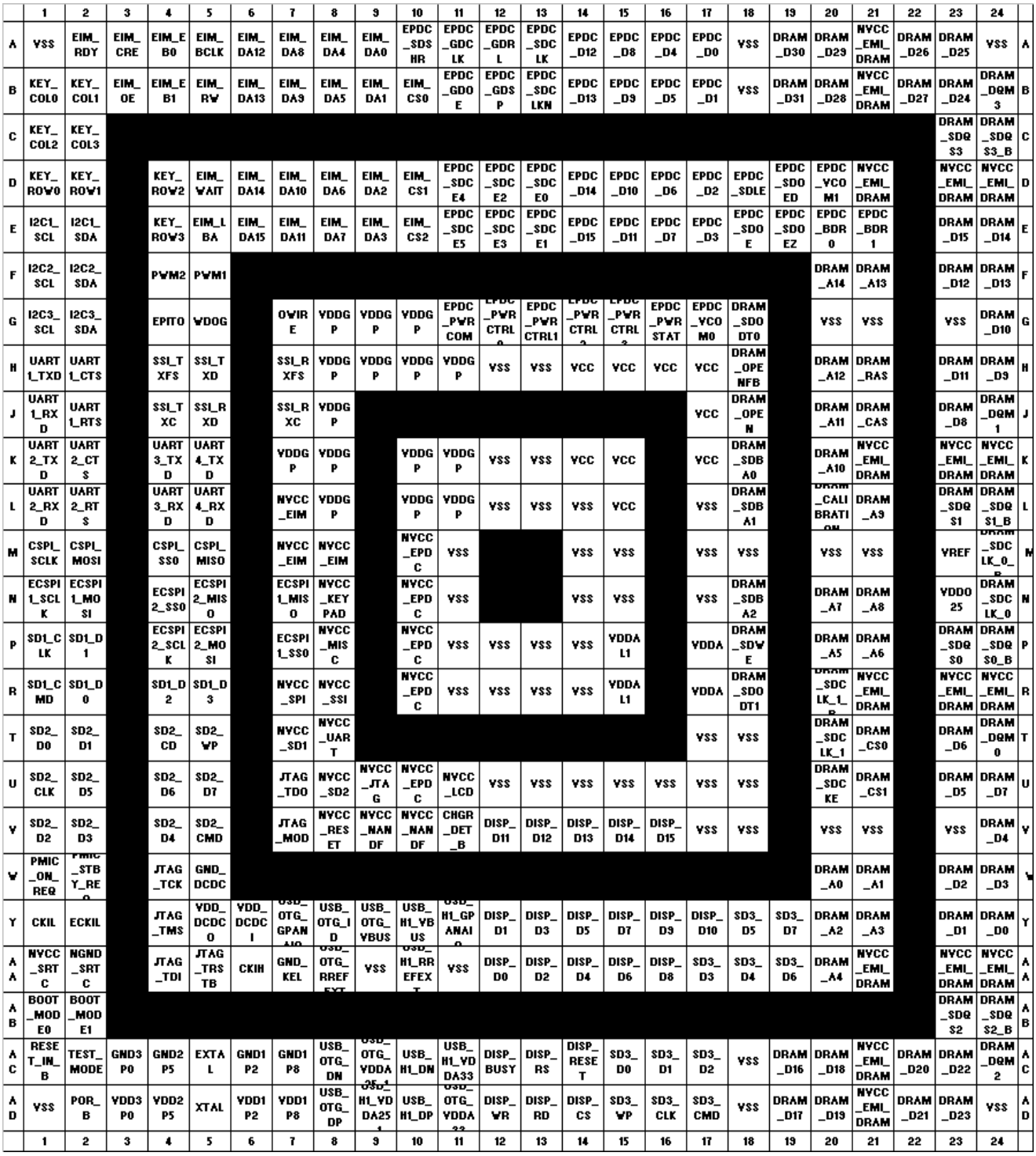
Figure 61. 416 Pin MAPBGA 13 × 13 mm Package Side View

The following notes apply to Figure 59, Figure 60, and Figure 61:

- Unless otherwise specified dimensions are in millimeters.
- All dimensions and tolerances conform to ASME Y14.5M-1994.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

5.1.2 416 MAPBGA 13 × 13 mm, 0.5 Pitch Ball Map

Figure 62 shows the 416 MAPBGA 13 × 13 mm, 0.5 pitch ball map.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
A	VSS	EIM_RDY	EIM_CRE	EIM_EB0	EIM_BCLK	EIM_DA12	EIM_DA8	EIM_DA4	EIM_DA0	EPDC_SDSHR	EPDC_GDCLK	EPDC_GDRL	EPDC_SDCLK	EPDC_D12	EPDC_D8	EPDC_D4	EPDC_D0	VSS	DRAM_D30	DRAM_D29	NVCC_EMI_DRAM	DRAM_D26	DRAM_D25	VSS	A
B	KEY_COL0	KEY_COL1	EIM_OE	EIM_EB1	EIM_RW	EIM_DA13	EIM_DA9	EIM_DA5	EIM_DA1	EIM_CS0	EPDC_GDOE	EPDC_GDSP	EPDC_SDCLKN	EPDC_D13	EPDC_D9	EPDC_D5	EPDC_D1	VSS	DRAM_D31	DRAM_D28	NVCC_EMI_DRAM	DRAM_D27	DRAM_D24	DRAM_DQM3	B
C	KEY_COL2	KEY_COL3																					DRAM_SDQS3	DRAM_SDQS3_B	C
D	KEY_ROW0	KEY_ROW1		KEY_ROW2	EIM_WAIT	EIM_DA14	EIM_DA10	EIM_DA6	EIM_DA2	EIM_CS1	EPDC_SDCE4	EPDC_SDCE2	EPDC_SDCE0	EPDC_D14	EPDC_D10	EPDC_D6	EPDC_D2	EPDC_SDLE	EPDC_SDOED	EPDC_VCOM1	NVCC_EMI_DRAM		NVCC_EMI_DRAM	NVCC_EMI_DRAM	D
E	I2C1_SCL	I2C1_SDA		KEY_ROW3	EIM_LBA	EIM_DA15	EIM_DA11	EIM_DA7	EIM_DA3	EIM_CS2	EPDC_SDCE5	EPDC_SDCE3	EPDC_SDCE1	EPDC_D15	EPDC_D11	EPDC_D7	EPDC_D3	EPDC_SDOE	EPDC_SDOEZ	EPDC_BDR0	EPDC_BDR1		DRAM_D15	DRAM_D14	E
F	I2C2_SCL	I2C2_SDA		PWM2	PWM1															DRAM_A14	DRAM_A13		DRAM_D12	DRAM_D13	F
G	I2C3_SCL	I2C3_SDA		EPITO	WDOG		OWIRE	VDDGP	VDDGP	VDDGP	EPDC_PWRCOM	EPDC_PWRCTRL0	EPDC_PWRCTRL1	EPDC_PWRCTRL2	EPDC_PWRCTRL3	EPDC_PWRSTAT	EPDC_VCOM0	DRAM_SDODT0		VSS	VSS		VSS	DRAM_D10	G
H	UART1_TXD	UART1_CTS		SSI_TXFS	SSI_TXD		SSI_RXFS	VDDGP	VDDGP	VDDGP	VDDGP	VSS	VSS	VCC	VCC	VCC	VCC	DRAM_OPENFB		DRAM_A12	DRAM_RAS		DRAM_D11	DRAM_D9	H
J	UART1_RXD	UART1_RTS		SSI_TXC	SSI_RXD		SSI_RXC	VDDGP									VCC	DRAM_OPEN		DRAM_A11	DRAM_CAS		DRAM_D8	DRAM_DQM1	J
K	UART2_TXD	UART2_CTS		UART3_TXD	UART4_TXD		VDDGP	VDDGP		VDDGP	VDDGP	VSS	VSS	VCC	VCC		VCC	DRAM_SDBA0		DRAM_A10	NVCC_EMI_DRAM		NVCC_EMI_DRAM	NVCC_EMI_DRAM	K
L	UART2_RXD	UART2_RTS		UART3_RXD	UART4_RXD		NVCC_EIM	VDDGP		VDDGP	VDDGP	VSS	VSS	VSS	VCC		VSS	DRAM_SDBA1		DRAM_CALIBRATION	DRAM_A9		DRAM_SDQS1	DRAM_SDQS1_B	L
M	CSPI_SCLK	CSPI_MOSI		CSPI_SS0	CSPI_MISO		NVCC_EIM	NVCC_EIM		NVCC_EPDC	VSS			VSS	VSS		VSS	VSS		VSS	VSS		VREF	DRAM_SDCLK_0_B	M
N	ECSPI1_SCLK	ECSPI1_MOSI		ECSPI2_SS0	ECSPI2_MISO		ECSPI1_MISO	NVCC_KEYPAD		NVCC_EPDC	VSS			VSS	VSS		VSS	DRAM_SDBA2		DRAM_A7	DRAM_A8		VDDO25	DRAM_SDCLK_0	N
P	SD1_CLK	SD1_D1		ECSPI2_SCLK	ECSPI2_MOSI		ECSPI1_SS0	NVCC_MISC		NVCC_EPDC	VSS	VSS	VSS	VSS	VDDAL1		VDDA	DRAM_SDWE		DRAM_A5	DRAM_A6		DRAM_SDQS0	DRAM_SDQS0_B	P
R	SD1_CMD	SD1_D0		SD1_D2	SD1_D3		NVCC_SPI	NVCC_SSI		NVCC_EPDC	VSS	VSS	VSS	VSS	VDDAL1		VDDA	DRAM_SDODT1		DRAM_SDCLK_1_B	NVCC_EMI_DRAM		NVCC_EMI_DRAM	NVCC_EMI_DRAM	R
T	SD2_D0	SD2_D1		SD2_CD	SD2_WP		NVCC_SD1	NVCC_UART									VSS	VSS		DRAM_SDCLK_1	DRAM_CS0		DRAM_D6	DRAM_DQM0	T
U	SD2_CLK	SD2_D5		SD2_D6	SD2_D7		JTAG_TDO	NVCC_SD2	NVCC_JTAG	NVCC_EPDC	NVCC_LCD	VSS	VSS	VSS	VSS	VSS	VSS	VSS		DRAM_SDCKE	DRAM_CS1		DRAM_D5	DRAM_D7	U
V	SD2_D2	SD2_D3		SD2_D4	SD2_CMD		JTAG_MOD	NVCC_RESET	NVCC_NANDF	NVCC_NANDF	CHGR_DET_B	DISP_D11	DISP_D12	DISP_D13	DISP_D14	DISP_D15	VSS	VSS		VSS	VSS		VSS	DRAM_D4	V
W	PMIC_ON_REQ	PMIC_STBY_REQ		JTAG_TCK	GND_DCDC															DRAM_A0	DRAM_A1		DRAM_D2	DRAM_D3	W
Y	CKIL	ECKIL		JTAG_TMS	VDD_DCDCO	VDD_DCDCI	USB_OTG_GPANAIO	USB_OTG_ID	USB_OTG_VBUS	USB_H1_VBUS	USB_H1_GPANAIO	DISP_D1	DISP_D3	DISP_D5	DISP_D7	DISP_D9	DISP_D10	SD3_D5	SD3_D7	DRAM_A2	DRAM_A3		DRAM_D1	DRAM_D0	Y
AA	NVCC_SRC	NGND_SRC		JTAG_TDI	JTAG_TRSTB	CKIH	GND_KEL	USB_OTG_RREFEXT	VSS	USB_H1_RREFEXT	VSS	DISP_D0	DISP_D2	DISP_D4	DISP_D6	DISP_D8	SD3_D3	SD3_D4	SD3_D6	DRAM_A4	NVCC_EMI_DRAM		NVCC_EMI_DRAM	NVCC_EMI_DRAM	AA
AB	BOOT_MODE0	BOOT_MODE1																					DRAM_SDQS2	DRAM_SDQS2_B	AB
AC	RESET_IN_B	TEST_MODE	GND3P0	GND2P5	EXTAL	GND1P2	GND1P8	USB_OTG_DN	USB_OTG_VDDA25_1	USB_H1_DN	USB_H1_VDDA33	DISP_BUSY	DISP_RS	DISP_RESET	SD3_D0	SD3_D1	SD3_D2	VSS	DRAM_D16	DRAM_D18	NVCC_EMI_DRAM	DRAM_D20	DRAM_D22	DRAM_DQM2	AC
AD	VSS	POR_B	VDD3P0	VDD2P5	XTAL	VDD1P2	VDD1P8	USB_OTG_DP	USB_H1_VDDA25_1	USB_H1_DP	USB_OTG_VDDA33	DISP_WR	DISP_RD	DISP_CS	SD3_WP	SD3_CLK	SD3_CMD	VSS	DRAM_D17	DRAM_D19	NVCC_EMI_DRAM	DRAM_D21	DRAM_D23	VSS	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	

Figure 62. 13 x 13 mm, 0.5 Pitch Ball Map

5.1.3 416 MAPBGA 13 x 13 Power Rails

Table 76. 416 MAPBGA 13 x 13 Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number	Comments
NVCC_EIM	L7 M7 M8	—
NVCC_EMI_DRAM	A21 AA21 AA23 AA24 D23 R24 AC21 AD21 B21 D21 D24 K21 K23 K24 R21 R23	—
NVCC_EPDC	M10 N10 P10 R10 U10	—
NVCC_JTAG	U9	—
NVCC_KEYPAD	N8	—
NVCC_LCD	U11	—
NVCC_MISC	P8	—
NVCC_NANDF	V10 V9	—
NVCC_RESET	V8	—
NVCC_SD1	T7	—
NVCC_SD2	U8	—
NVCC_SPI	R7	—
NVCC_SRTC	AA1	—
NVCC_SSI	R8	—
NVCC_UART	T8	—
USB_H1_VDDA25	AD9	Note that on the 416 MAPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the substrate.
USB_H1_VDDA33	AC11	Note that on the 416 MAPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the substrate.
USB_OTG_VDDA25	AC9	Note that on the 416 MAPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the substrate.
USB_OTG_VDDA33	AD11	Note that on the 416 MAPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the substrate.
VCC	H14 H15 H16 H17 J17 K14 K15 K17 L15	—
VDD1P2	AD6	—
VDD1P8	AD7	—
VDD2P5	AD4	—
VDD3P0	AD3	—
VDDA	P17 R17	—
VDDAL1	P15 R15	—

Table 76. 416 MAPBGA 13 x 13 Ground, Power, Sense, and Reference Contact Signals

VDDGP	L11 G10 G8 G9 H10 L10 L8 H11 H8 H9 J8 K10 K11 K7 K8	—
VDDO25	N23	—
VSS	A1 L13 H12 H13 L17 R13 V21 AA2 A18 AC3 AC4 AC6 AC7 A24 AA11 AA9 AC18 AD1 AD18 AD24 B18 G21 G20 G23 K12 K13 L12 P12 M11 L14 M14 P13 M15 M17 M18 M20 M21 N11 N14 N15 R12 N17 P11 P14 R11 R14 T17 T18 U12 U13 U14 U15 U16 U17 U18 V17 V18 V20 V23	—
VDD_DCDCI	Y6	—
VDD_DCDCO	Y5	—
GND_DCDC	W5	—

5.2 400 MAPBGA 17x 17 mm 0.8 mm Pitch Package Information

This section contains the outline drawing, signal assignment map, ground, power, reference ID (by ball grid location) for the 17 x 17 mm 400 Pin MAPBGA package.

5.2.1 400 MAPBGA 17 x 17 mm Package Views

Figure 63 shows the top view of the 17 x 17 mm package, Figure 64 shows the bottom view of the package, and Figure 65 shows the side view of the package.

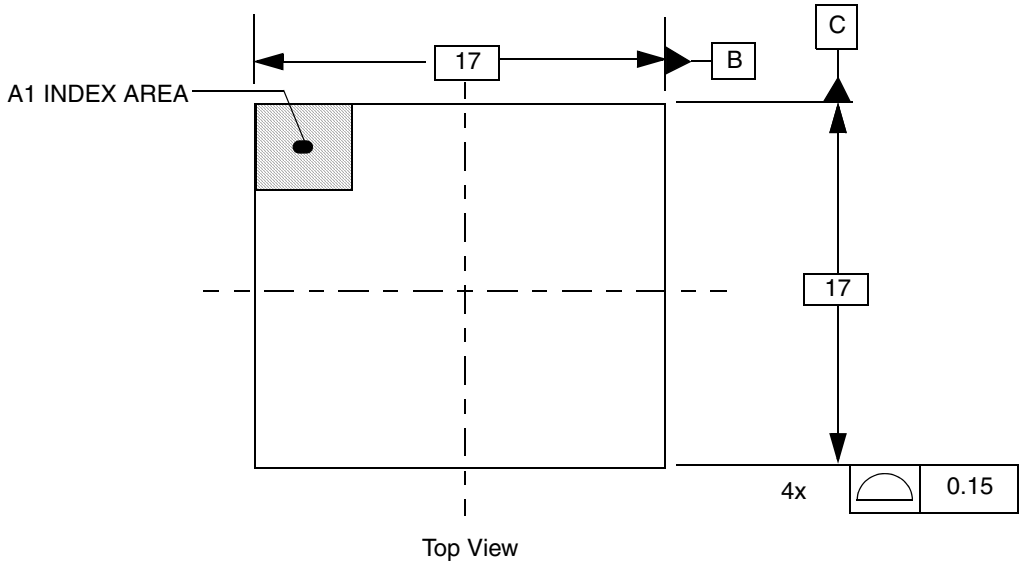


Figure 63. 400 MAPBGA 17x17 mm, Package Top view

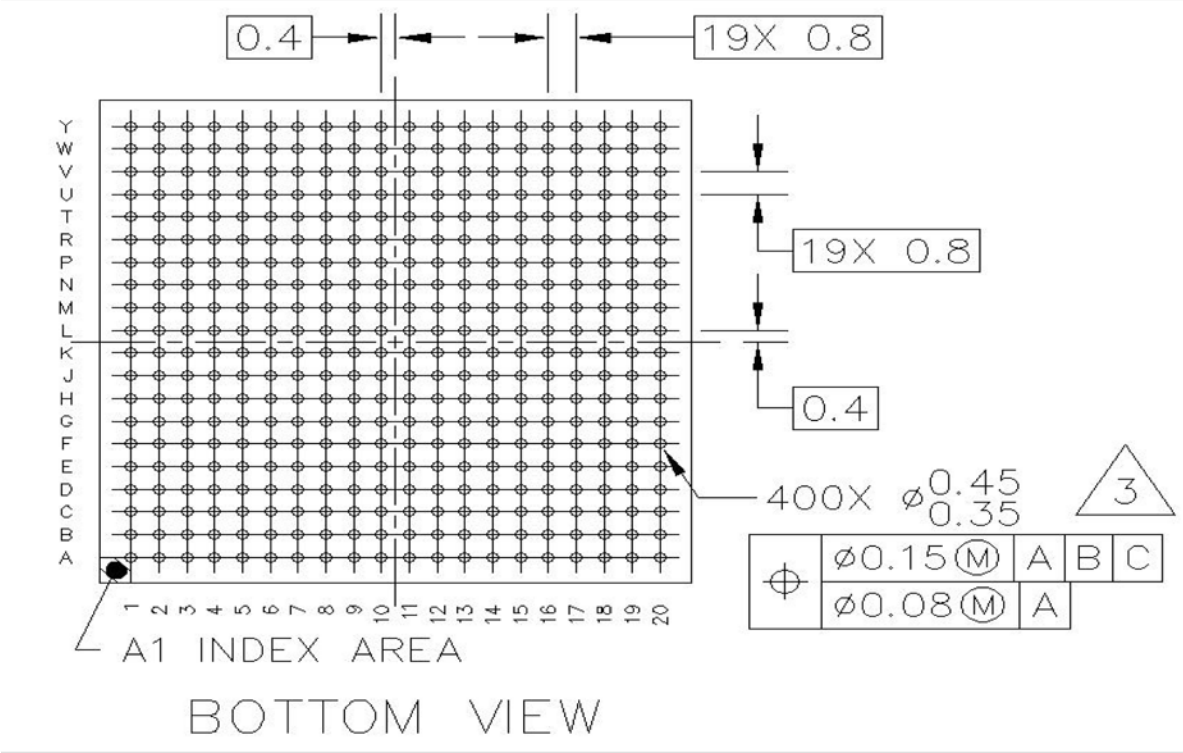


Figure 64. 400 MAPBGA 17x17 mm, Package Bottom View

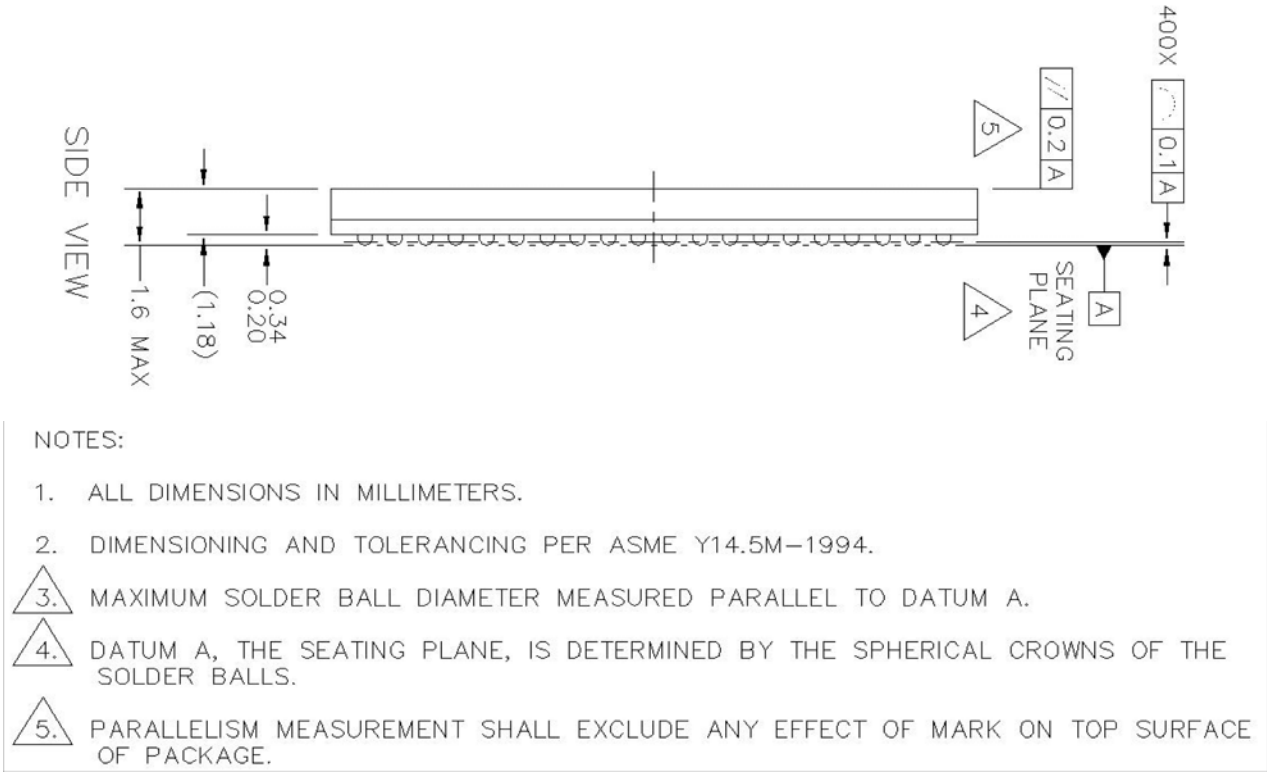


Figure 65. 400 MAPBGA 17x17mm, Package Side View

The following notes apply to Figure 63, Figure 64, and Figure 65:

- Unless otherwise specified dimensions are in millimeters.
- All dimensions and tolerances conform to ASME Y14.5M-1994.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

5.2.2 400 MAPBGA 17 x 17 mm Ball Map

Figure 66 shows the 400 MAPBGA 17 x 17 mm ball map.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	EIM_RDY	EIM_CRE	EIM_EB0	EIM_BCLK	EIM_DA12	EIM_DA8	EPDC_SDSHR	EIM_DA4	EPDC_GDRL	EPDC_GDCLK	EPDC_SDCE1	EPDC_D5	EPDC_D1	EPDC_BDR0	DRAM_D26	DRAM_D28	DRAM_D29	DRAM_D30	NC
B	KEY_COL0	KEY_COL1	EIM_OE	EIM_EB1	EIM_RW	EIM_DA13	EIM_DA9	EIM_DA5	EIM_DA1	EIM_DA0	EIM_CS0	EPDC_SDCE0	EPDC_SDCLK	EPDC_VCOM0	EPDC_D0	EPDC_D2	DRAM_D27	DRAM_D25	DRAM_D24	DRAM_D31
C	KEY_COL2	KEY_COL3	KEY_ROW2	EIM_WAIT	EIM_DA14	EIM_DA10	EIM_DA6	EIM_DA2	EIM_CS1	EPDC_GDOE	EPDC_SDCE2	EPDC_PWRSTAT	EPDC_SDOE	EPDC_D6	EPDC_SDLE	EPDC_D3	DRAM_D15	DRAM_D14	DRAM_SDQS3	DRAM_SDQS3_B
D	KEY_ROW0	KEY_ROW1	KEY_ROW3	EIM_LBA	EIM_DA15	EIM_DA11	EIM_DA7	EIM_DA3	EIM_CS2	EPDC_SDCE4	EPDC_GDSP	EPDC_SDCLKN	EPDC_D10	EPDC_D7	EPDC_D4	EPDC_BDR1	DRAM_D8	DRAM_D12	DRAM_D11	DRAM_DQM3
E	I2C1_SCL	I2C1_SDA	PWM2	PWM1	OWIRE	EPDC_SDCE5	EPDC_PWRCOM	EPDC_SDCE3	EPDC_PWRCTRL1	EPDC_PWRCTRL0	EPDC_D14	EPDC_PWRCTRL2	EPDC_D15	EPDC_D13	EPDC_D8	EPDC_D9	DRAM_D10	DRAM_D13	DRAM_A12	DRAM_RAS
F	I2C2_SCL	I2C2_SDA	SSI_RXD	WDOG	EPITO	NVCC_EIM	NVCC_EIM	NVCC_EIM	NVCC_EPDC	NVCC_EPDC	NVCC_EPDC	NVCC_EPDC	EPDC_D12	EPDC_D11	EPDC_PWRCTRL3	EPDC_SDOEZ	DRAM_DQM1	DRAM_D9	DRAM_A13	DRAM_CALIBRATION
G	I2C3_SCL	I2C3_SDA	SSI_TXC	SSI_TXD	SSI_RXFS	VDDGP	VDDGP	VDDGP	VDDGP	VDDGP	VSS	VSS	VSS	VSS	EPDC_VCOM1	EPDC_SDOED	DRAM_SDQS1_B	DRAM_SDQS1_B	DRAM_A9	DRAM_CAS
H	UART1_TXD	UART4_TXD	SSI_TXFS	SSI_RXC	NVCC_KEYPAD	VDDGP	VDDGP	VDDGP	VDDGP	VDDGP	VSS	VSS	VSS	VSS	VSS	NVCC_EMI_DRAM	DRAM_OPENFB	DRAM_OPEN	DRAM_A11	DRAM_SDBA1
J	UART1_CTS	UART3_TXD	UART4_RXD	CSPI_SS0	NVCC_MISC	VDDGP	VDDGP	VSS	VDDAL1	VDDAL1	VDDA	VCC	VSS	VSS	NVCC_EMI_DRAM	NVCC_EMI_DRAM	DRAM_SDCLK_0_B	DRAM_SDCLK_0_B	DRAM_A10	DRAM_SDBA0
K	UART1_RXD	UART1_RTS	UART3_RXD	CSPI_MISO	NVCC_SSI	VDDGP	VDDGP	VSS	VDDA	VCC	VCC	VCC	VSS	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	VREF	DRAM_SDODT0	DRAM_A5	DRAM_A7
L	UART2_TXD	UART2_RXD	CSPI_MOSI	ECSPI2_MISO	NVCC_UART	VDDGP	VSS	VSS	VSS	VCC	VCC	VCC	VSS	VSS	NVCC_EMI_DRAM	NVCC_EMI_DRAM	VDDO25	DRAM_SDWE	DRAM_A6	DRAM_A8
M	CSPI_SCLK	ECSPI2_SS0	ECSPI1_MISO	ECSPI1_MOSI	NVCC_SPI	VSS	VSS	VSS	VSS	VCC	VCC	VSS	VSS	VSS	VSS	NVCC_EMI_DRAM	DRAM_SDQS0	DRAM_SDQS0_B	DRAM_SDBA2	DRAM_D6
N	ECSPI2_MOSI	ECSPI1_SCLK	ECSPI1_SS0	ECSPI2_SCLK	NVCC_SD1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	DRAM_DQM0	DRAM_D5	DRAM_D7	DRAM_D4
P	SD1_D1	SD1_D3	SD1_D2	SD1_CMD	NVCC_SD2	NVCC_RESET	VSS	VSS	NVCC_JTAG	NVCC_LCD	NVCC_NANDF	NVCC_NANDF	VSS	VSS	NVCC_EMI_DRAM	NVCC_EMI_DRAM	DRAM_CS0	DRAM_CS1	DRAM_D3	DRAM_D2
R	SD1_CLK	SD1_D0	SD2_D0	SD2_D6	NVCC_SRTC	GND_DCDC	VDD_DCDCI	JTAG_TCK	JTAG_TMS	VSS	VSS	VSS	VSS	VSS	VSS	NVCC_EMI_DRAM	DRAM_A4	DRAM_SDCKE	DRAM_D1	DRAM_D0
T	SD2_CD	SD2_WP	SD2_CLK	SD2_D3	VSS	VDD_DCDCO	GND_KEL	JTAG_MOD	JTAG_TDO	CHGR_DET_B	DISP_D1	DISP_CS	DISP_D13	DISP_RESET	SD3_D7	SD3_D2	DRAM_A0	DRAM_A1	DRAM_SDQS2	DRAM_SDQS2_B
U	SD2_D1	SD2_D5	BOOT_MODE1	TEST_MODE	VDD3P0	VDD1P2	JTAG_TRSTB	JTAG_TDI	USB_H1_RREFEXT	USB_H1_GPANAIO	DISP_BUSY	DISP_D6	DISP_D5	DISP_D14	SD3_D3	SD3_CMD	SD3_D5	DRAM_A2	DRAM_D23	DRAM_DQM2
V	SD2_CMD	SD2_D4	BOOT_MODE0	CKIH	VDD2P5	VDD1P8	USB_OTG_GPANAIO	USB_OTG_VBUS	USB_H1_VBUS	DISP_WR	DISP_D0	DISP_RD	DISP_D7	DISP_D12	DISP_D9	SD3_D1	SD3_D6	DRAM_A3	DRAM_D18	DRAM_D22
W	SD2_D7	SD2_D2	RESET_IN_B	ECKIL	VSS	EXTAL	USB_OTG_RREFEXT	USB_OTG_DN	USB_OTG_VDDA25	USB_H1_DN	USB_H1_VDDA33	DISP_D2	DISP_D3	DISP_D11	DISP_D8	SD3_WP	SD3_D4	DRAM_D21	DRAM_D19	DRAM_D20
Y	NC	PMIC_STBY_REQ	PMIC_ON_REQ	CKIL	POR_B	XTAL	USB_OTG_ID	USB_OTG_DP	USB_H1_VDDA25	USB_H1_DP	USB_OTG_VDDA33	DISP_RS	DISP_D4	SD3_CLK	DISP_D15	DISP_D10	SD3_D0	DRAM_D17	DRAM_D16	NC

Figure 66. 400 MAPBGA 17 x 17 Ball Map

5.2.3 400 MAPBGA 17 x 17 Power Rails

Table 77. 400 MAPBGA 17 x 17 Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number
NC	A1 Y1 A20 Y20
NVCC_EIM	F6 F7 F8
NVCC_EMI_DRAM	K14 N14 J15 K15 L15 N15 P15 H16 J16 K16 L16 M16 N16 P16 R16
NVCC_EPDC	F9 F10 F11 F12
NVCC_JTAG	P9
NVCC_KEYPAD	H5
NVCC_LCD	P10
NVCC_MISC	J5
NVCC_NANDF	P11 P12
NVCC_RESET	P6
NVCC_SD1	N5
NVCC_SD2	P5
NVCC_SPI	M5
NVCC_SRTC	R5
NVCC_SSI	K5
NVCC_UART	L5
USB_H1_VDDA25	Y9
USB_H1_VDDA33	W11
USB_OTG_VDDA25	W9
USB_OTG_VDDA33	Y11
VCC	K10 L10 M10 K11 L11 M11 J12 K12 L12
VDD1P2	U6
VDD1P8	V6
VDD2P5	V5
VDD3P0	U5
VDDA	K9 J11
VDDAL1	J9 J10
VDDGP	G6 H6 J6 K6 L6 G7 H7 J7 K7 G8 H8 G9 H9 G10 H10
VDDO25	L17
VSS	T5 W5 M6 N6 L7 M7 N7 P7 J8 K8 L8 M8 N8 P8 L9 M9 N9 N10 R10 G11 H11 N11 R11 G12 H12 M12 N12 R12 G13 H13 J13 K13 L13 M13 N13 P13 R13 G14 H14 J14 L14 M14 P14 R14 H15 M15 R15

Table 77. 400 MAPBGA 17 x 17 Ground, Power, Sense, and Reference Contact Signals (continued)

VDD_DCDCI	R7
VDD_DCDCO	T6
GND_DCDC	R6

5.3 Signal Assignments

Table 78. Alphabetical List of Signal Assignments

Pin Name	416 MAPBGA Ball	400 MAPBGA Ball	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
BOOT_MODE0	AB1	V3	NVCC_RESET	LVIO	ALT0	IN	100K PU
BOOT_MODE1	AB2	U3	NVCC_RESET	LVIO	ALT0	IN	100K PU
CHGR_DET_B	V11	T10	USB_H1_VDDA	ANALOG25	—	OUT-OD	—
CKIH	AA6	V4	NVCC_JTAG	ANALOG	—	—	—
CKIL	Y1	Y4	NVCC_SRTC	ANALOG	—	—	—
CSPI_MISO	M5	K4	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_MOSI	M2	L3	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SCLK	M1	M1	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SS0	M4	J4	NVCC_SPI	HVIO	ALT1	IN	Keeper
DISP_BUSY	AC12	U11	NVCC_LCD	HVIO	ALT1	IN	Keeper
DISP_CS	AD14	T12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D0	AA12	V11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D1	Y12	T11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D10	Y17	Y16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D11	V12	W14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D12	V13	V14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D13	V14	T13	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D14	V15	U14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D15	V16	Y15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D2	AA13	W12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D3	Y13	W13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D4	AA14	Y13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D5	Y14	U13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D6	AA15	U12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D7	Y15	V13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D8	AA16	W15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D9	Y16	V15	NVCC_NANDF	HVIO	ALT1	IN	Keeper

Table 78. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball	400 MAPBGA Ball	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
DISP_RD	AD13	V12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_RESET	AC14	T14	NVCC_LCD	HVIO	ALT1	IN	Keeper
DISP_RS	AC13	Y12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_WR	AD12	V10	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DRAM_A0	W20	T17	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A1	W21	T18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A10	K20	J19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A11	J20	H19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A12	H20	E19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A13	F21	F19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A14	F20	—	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A2	Y20	U18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A3	Y21	V18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A4	AA20	R17	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A5	P20	K19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A6	P21	L19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A7	N20	K20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A8	N21	L20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A9	L21	G19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_CALIBRATION	L20	F20	NVCC_EMI_DRAM	DRAM	—	—	—
DRAM_CAS	J21	G20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_CS0	T21	P17	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_CS1	U21	P18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_D0	Y24	R20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D1	Y23	R19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D10	G24	E17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D11	H23	D19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D12	F23	D18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D13	F24	E18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper

Table 78. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball	400 MAPBGA Ball	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
DRAM_D14	E24	C18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D15	E23	C17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D16	AC19	Y19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D17	AD19	Y18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D18	AC20	V19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D19	AD20	W19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D2	W23	P20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D20	AC22	W20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D21	AD22	W18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D22	AC23	V20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D23	AD23	U19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D24	B23	B19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D25	A23	B18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D26	A22	A16	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D27	B22	B17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D28	B20	A17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D29	A20	A18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D3	W24	P19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D30	A19	A19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D31	B19	B20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D4	V24	N20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D5	U23	N18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D6	T23	M20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D7	U24	N19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D8	J23	D17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D9	H24	F18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM0	T24	N17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM1	J24	F17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM2	AC24	U20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM3	B24	D20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper

Table 78. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball	400 MAPBGA Ball	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
DRAM_OPEN	J18	H18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_OPENFB	H18	H17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_RAS	H21	E20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_SDBA0	K18	J20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDBA1	L18	H20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDBA2	N18	M19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCKE	U20	R18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCLK_0	M24	J17	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCLK_0_B	N24	J18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	—
DRAM_SDCLK_1	R20	—	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCLK_1_B	T20	—	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	—
DRAM_SDODT0	G18	K18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDODT1	R18	—	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDQS0	P24	M17	NVCC_EMI_DRAM	DRAM	ALT0	IN	—
DRAM_SDQS0_B	P23	M18	NVCC_EMI_DRAM	DRAM	ALT0	IN	—
DRAM_SDQS1	L23	G17	NVCC_EMI_DRAM	DRAM	ALT0	IN	—
DRAM_SDQS1_B	L24	G18	NVCC_EMI_DRAM	DRAM	ALT0	IN	—
DRAM_SDQS2	AB23	T19	NVCC_EMI_DRAM	DRAM	ALT0	IN	—
DRAM_SDQS2_B	AB24	T20	NVCC_EMI_DRAM	DRAM	ALT0	IN	—
DRAM_SDQS3	C23	C19	NVCC_EMI_DRAM	DRAM	ALT0	IN	—
DRAM_SDQS3_B	C24	C20	NVCC_EMI_DRAM	DRAM	ALT0	IN	—
DRAM_SDWE	P18	L18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
ECKIL	Y2	W4	NVCC_SRTC	ANALOG	—	—	—
ECSPI1_MISO	N7	M3	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI1_MOSI	N2	M4	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI1_SCLK	N1	N2	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI1_SS0	P7	N3	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI2_MISO	N5	L4	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI2_MOSI	P5	N1	NVCC_SPI	HVIO	ALT1	IN	Keeper

Table 78. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball	400 MAPBGA Ball	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
ECSPI2_SCLK	P4	N4	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI2_SS0	N4	M2	NVCC_SPI	HVIO	ALT1	IN	Keeper
EIM_BCLK	A5	A5	NVCC_EIM	HVIO	ALT0	OUT-LO	100K PU
EIM_CRE	A3	A3	NVCC_EIM	HVIO	ALT0	OUT-LO	100K PU
EIM_CS0	B10	B11	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_CS1	D10	C9	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_CS2	E10	D9	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_DA0	A9	B10	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA1	B9	B9	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA10	D7	C6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA11	E7	D6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA12	A6	A6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA13	B6	B6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA14	D6	C5	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA15	E6	D5	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA2	D9	C8	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA3	E9	D8	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA4	A8	A9	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA5	B8	B8	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA6	D8	C7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA7	E8	D7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA8	A7	A7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA9	B7	B7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_EB0	A4	A4	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_EB1	B4	B4	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_LBA	E5	D4	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_OE	B3	B3	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_RDY	A2	A2	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_RW	B5	B5	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_WAIT	D5	C4	NVCC_EIM	HVIO	ALT0	IN	100K PU

Table 78. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball	400 MAPBGA Ball	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
EPDC_BDR0	E20	A15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_BDR1	E21	D16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D0	A17	B15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D1	B17	A14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D10	D15	D13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D11	E15	F14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D12	A14	F13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D13	B14	E14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D14	D14	E11	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D15	E14	E13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D2	D17	B16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D3	E17	C16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D4	A16	D15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D5	B16	A13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D6	D16	C14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D7	E16	D14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D8	A15	E15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D9	B15	E16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_GDCLK	A11	A11	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_GDOE	B11	C10	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_GDRL	A12	A10	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_GDSP	B12	D11	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRCOM	G11	E7	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRCTRL0	G12	E10	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRCTRL1	G13	E9	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRCTRL2	G14	E12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRCTRL3	G15	F15	NVCC_EPDC	HVIO	ALT1	IN	Keeper

Table 78. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball	400 MAPBGA Ball	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
EPDC_PWRSTAT	G16	C12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE0	D13	B12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE1	E13	A12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE2	D12	C11	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE3	E12	E8	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE4	D11	D10	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE5	E11	E6	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCLK	A13	B13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCLKN	B13	D12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDLE	D18	C15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOE	E18	C13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOED	D19	G16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOEZ	E19	F16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDSHR	A10	A8	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_VCOM0	G17	B14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_VCOM1	D20	G15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPITO	G4	F5	NVCC_MISC	HVIO	ALT1	IN	Keeper
EXTAL	AC5	W6	VDD2P5	ANALOG	—	—	—
GND_KEL	AA7	T7	VDD2P5	ANALOG	—	—	—
I2C1_SCL	E1	E1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C1_SDA	E2	E2	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C2_SCL	F1	F1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C2_SDA	F2	F2	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C3_SCL	G1	G1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C3_SDA	G2	G2	NVCC_MISC	HVIO	ALT1	IN	Keeper
JTAG_MOD	V7	T8	NVCC_JTAG	GPIO	ALT0	IN	100K PU
JTAG_TCK	W4	R8	NVCC_JTAG	GPIO	ALT0	IN	100K PD
JTAG_TDI	AA4	U8	NVCC_JTAG	GPIO	ALT0	IN	47K PU
JTAG_TDO	U7	T9	NVCC_JTAG	GPIO	ALT0	OUT-LO	Keeper
JTAG_TMS	Y4	R9	NVCC_JTAG	GPIO	ALT0	IN	47K PU

Table 78. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball	400 MAPBGA Ball	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
JTAG_TRSTB	AA5	U7	NVCC_JTAG	GPIO	ALT0	IN	47K PU
KEY_COL0	B1	B1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL1	B2	B2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL2	C1	C1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL3	C2	C2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW0	D1	D1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW1	D2	D2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW2	D4	C3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW3	E4	D3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
OWIRE	G7	E5	NVCC_MISC	HVIO	ALT1	IN	Keeper
PMIC_ON_REQ	W1	Y3	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
PMIC_STBY_REQ	W2	Y2	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
POR_B	AD2	Y5	NVCC_RESET	LVIO	ALT0	IN	100K PU
PWM1	F5	E4	NVCC_MISC	HVIO	ALT1	IN	Keeper
PWM2	F4	E3	NVCC_MISC	HVIO	ALT1	IN	Keeper
RESET_IN_B	AC1	W3	NVCC_RESET	LVIO	ALT0	IN	100K PU
SD1_CLK	P1	R1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_CMD	R1	P4	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D0	R2	R2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D1	P2	P1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D2	R4	P3	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D3	R5	P2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD2_CD	T4	T1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CLK	U1	T3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CMD	V5	V1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D0	T1	R3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D1	T2	U1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D2	V1	W2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D3	V2	T4	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D4	V4	V2	NVCC_SD2	HVIO	ALT1	IN	Keeper

Table 78. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball	400 MAPBGA Ball	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
SD2_D5	U2	U2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D6	U4	R4	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D7	U5	W1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_WP	T5	T2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD3_CLK	AD16	Y14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_CMD	AD17	U16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D0	AC15	Y17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D1	AC16	V16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D2	AC17	T16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D3	AA17	U15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D4	AA18	W17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D5	Y18	U17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D6	AA19	V17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D7	Y19	T15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_WP	AD15	W16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SSI_RXC	J7	H4	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_RXD	J5	F3	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_RXFS	H7	G5	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXC	J4	G3	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXD	H5	G4	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXFS	H4	H3	NVCC_SSI	HVIO	ALT1	IN	Keeper
TEST_MODE	AC2	U4	NVCC_RESET	LVIO	ALT0	IN	100K PD
UART1_CTS	H2	J1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_RTS	J2	K2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_RXD	J1	K1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_TXD	H1	H1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_CTS	K2		NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_RTS	L2		NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_RXD	L1	L2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_TXD	K1	L1	NVCC_UART	HVIO	ALT1	IN	Keeper

Table 78. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball	400 MAPBGA Ball	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
UART3_RXD	L4	K3	NVCC_UART	HVIO	ALT1	IN	Keeper
UART3_TXD	K4	J2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART4_RXD	L5	J3	NVCC_UART	HVIO	ALT1	IN	Keeper
UART4_TXD	K5	H2	NVCC_UART	HVIO	ALT1	IN	Keeper
USB_H1_DN	AC10	W10	USB_H1_VDDA	ANALOG50	—	—	—
USB_H1_DP	AD10	Y10	USB_H1_VDDA	ANALOG50	—	—	—
USB_H1_GPANAIO	Y11	U10	USB_H1_VDDA	ANALOG25	—	—	—
USB_H1_RREFEXT	AA10	U9	USB_H1_VDDA	ANALOG25	—	—	—
USB_H1_VBUS	Y10	V9	USB_H1_VDDA	ANALOG50	—	—	—
USB_OTG_DN	AC8	W8	USB_OTG_VDDA	ANALOG50	—	—	—
USB_OTG_DP	AD8	Y8	USB_OTG_VDDA	ANALOG50	—	—	—
USB_OTG_GPANAIO	Y7	V7	USB_OTG_VDDA	ANALOG25	—	—	—
USB_OTG_ID	Y8	Y7	USB_OTG_VDDA	ANALOG25	—	—	—
USB_OTG_RREFEXT	AA8	W7	USB_OTG_VDDA	ANALOG25	—	—	—
USB_OTG_VBUS	Y9	V8	USB_OTG_VDDA	ANALOG50	—	—	—
VREF	M23	K17	VDDO25	ANALOG	—	—	—
WDOG	G5	F4	NVCC_MISC	HVIO	ALT1	IN	—
XTAL	AD5	Y6	VDD2P5	ANALOG	—	—	—

6 Revision History

Table 79 provides a revision history for this data sheet.

Table 79. i.MX50 Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev 0	07/2011	Initial release.

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Document Number: IMX50CEC
Rev. 0
7/2011