

SCOPE: QUAD, CMOS, 8-BIT D/A CONVERTER

<u>Device Type</u>	<u>Generic Number</u>	<u>Circuit Function</u>
01	MX7226T(x)/883B	DAC with 2 LSB
02	MX7226U(x)/883B	DAC with 1 LSB

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
Q	GDIP1-T20 or CDIP2-T20	20 LEAD CERDIP	J20
E	CQCC1-N20	20 LCC	L20

Absolute Maximum Ratings:

V_{DD} to AGND	-0.3V, +17V
V_{DD} to DGND	-0.3V, +17V
V_{SS} to AGND	-7V, V_{DD}
V_{SS} to DGND	-7V, V_{DD}
V_{DD} to V_{SS}	-0.3V, +24V
Digital Input Voltage to DGND	-0.3V, V_{DD}
V_{REF} to AGND	-0.3V, V_{DD}
V_{OUT} to AGND	V_{SS} , V_{DD}
Lead Temperature (soldering, 10 seconds)	+300°C
Storage Temperature	-65°C to +150°C
Continuous Power Dissipation	$T_A=+70^\circ\text{C}$
20 pin CERDIP(derate 11.1mW/°C above +70°C)	889mW
20 pin LCC(derate 9.1mW/°C above +70°C)	727mW
Junction Temperature T_J	+150°C
Thermal Resistance, Junction to Case, Θ_{JC}	
20 pin CERDIP.....	40°C/W
20 pin LCC	20°C/W
Thermal Resistance, Junction to Ambient, Θ_{JA} :	
20 pin CERDIP.....	90°C/W
20 pin LCC	110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A)	-55°C to +125°C
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Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS		Limits Min	Limits Max	Units	
		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ $\frac{1}{\text{U}}$	Group A Subgroup				Device type
STATIC PERFORMANCE							
Resolution	RES	Guaranteed, but not tested	1,2,3	All	8.0	Bits	
Total Unadjusted Error	ET	$V_{DD}=+14\text{V}$, $V_{SS}=-5\text{V}$, $V_{REF}=+10\text{V}$	1,2,3	01 02	-2.0 -1.0	2.0 1.0	LSB
Relative Accuracy	RA	$V_{DD}=+14\text{V}$, $V_{SS}=-5\text{V}$, $V_{REF}=+10\text{V}$	1,2,3	01 02	-1.0 -0.5	1.0 0.5	LSB
Differential Nonlinearity	DNL	$V_{DD}=+14\text{V}$, $V_{SS}=-5\text{V}$, $V_{REF}=+10\text{V}$	1,2,3	All	-1.0	1.0	LSB
Full-Scale Error	AE	$V_{DD}=+14\text{V}$, $V_{SS}=-5\text{V}$, $V_{REF}=+10\text{V}$	1,2,3	01 02	-1.0 -0.5	1.0 0.5	LSB
Zero-Code Error		$V_{DD}=+11.4\text{V}$, 14V , 16.5V , $V_{SS}=-5\text{V}$, $V_{REF}=V_{DD}-4\text{V}$	1,2,3	01	-30	30	mV
Zero-Code Error		$V_{DD}=+11.4\text{V}$, 14V , 16.5V , $V_{SS}=-5\text{V}$, $V_{REF}=V_{DD}-4\text{V}$	1 2,3	02	-15 20	15 20	mV
DYNAMIC PERFORMANCE							
Voltage Output Settling Time NOTES 2, 4	T_{SL}	Positive (Full Scale) Negative (Full Scale)	4	All		5 7	μs
Voltage Output Slew Rate NOTE 2	T_{SR}		4	All	2.5		$\text{V}/\mu\text{s}$
Minimum Load Resistance	$R_{L\text{MIN}}$	$V_{OUT}=+10\text{V}$, $V_{DD}=14\text{V}$	4	All	2		$\text{k}\Omega$
REFERENCE INPUT							
Reference Input Voltage Range				All	2	$V_{DD}-4$	V
Reference Input Resistance	R_{IN}	$V_{DD}=14\text{V}$	1,2,3	All	2		$\text{k}\Omega$
Reference Input Capacitance	C_{IN}	DAC loaded with all 1s DAC loaded with all 0s	4	All		300 30	pF
DIGITAL INPUTS							
Digital Input High Voltage	V_{IH}	$V_{DD}=11.4\text{V}$	1,2,3	All	2.4		V
Digital Input Low Voltage	V_{IL}	$V_{DD}=11.4\text{V}$	1,2,3	All		0.8	V
Digital Input Leakage Current	I_{IN}	$V_{IN}=0\text{V}$ or V_{DD} , $V_{DD}=16.5\text{V}$, $V_{SS}=5.5\text{V}$	1,2,3	All	-1.0	1.0	μA
Digital Input Capacitance	C_{IN}		4	All		8.0	pF
SWITCHING CHARACTERISTICS							
Write Pulse Width, t_1	t_{WR}	NOTE 5	9	All	200		ns
Address to Write-Setup Time, t_2	t_{AS}	NOTE 5	9	All	0		ns
Address to Write-Hold Time, t_3	t_{AH}	NOTE 5	9	All	10		ns
Data Valid to Write Set-up Time, t_4	t_{DS}	NOTE 5	9	All	100		ns

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C <=T _A <= +125°C <u>1/</u> Unless otherwise specified					
Data Valid to Write Hold Time, t ₅	t _{DH}	NOTE 5	9	All	10		ns
POWER SUPPLIES							
Positive Supply Current	I _{DD}	V _{IN} =V _{IL} or V _{IH} , V _{DD} =16.5V, V _{SS} =-5.5V, VREF=12.5V	1,2,3	All		13	mA
Negative Supply Current	I _{SS}	V _{IN} =V _{IL} or V _{IH} , V _{DD} =16.5V, V _{SS} =-5.5V, VREF=12.5V	1,2,3	All		11	mA

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C <=T _A <= +125°C <u>6/</u> Unless otherwise specified					
STATIC PERFORMANCE							
Resolution	RES	NOTE 2		All	8.0		Bits
Total Unadjusted Error	E _T	V _{DD} =14V, VREF=10V	1,2,3	01 02	-2.0 -1.0	2.0 1.0	LSB
Differential Nonlinearity	DNL	NOTE 3	1,2,3	All	-1.0	1.0	LSB
REFERENCE INPUT							
Minimum Load Resistance	R _{L-MIN}	V _{OUT} =10V, V _{DD} =15V NOTE 5	4	All	2		kΩ
Reference Input Resistance	R _{IN}	V _{DD} =14V	1,2,3	All	2		kΩ
Reference Input Capacitance	C _{IN}	DAC loaded with all 1s DAC loaded with all 0s	4	All		300 30	pF
DYNAMIC PERFORMANCE							
Voltage Output Settling Time NOTES 2,4, 5	T _{SL}	Positive (Full Scale) Negative (Full Scale)	4	All		5 20	μs
Voltage Output Slew Rate NOTES 2, 5	T _{SR}		4	All	2.5		V/μs
DIGITAL INPUTS							
Digital Input High Voltage	V _{IH}	V _{DD} =14.25V	1,2,3	All	2.4		V
Digital Input Low Voltage	V _{IL}	V _{DD} =14.25V	1,2,3	All		0.8	V
Digital Input Leakage Current	I _{IN}	V _{IN} =0V or V _{DD} , V _{DD} =15.75V	1,2,3	All	-1	1	μA
Digital Input Capacitance	C _{IN}		4	All		8	pF
SWITCHING CHARACTERISTICS							
Same as Dual Supply Operation							
POWER SUPPLIES							
Power-Supply Current	I _{DD}	V _{IN} =V _{IL} or V _{IH} , V _{DD} =15.75V, VREF=10V	1,2,3	All		13	mA

NOTE 1: Dual-Supply operation, $V_{DD}=+11.4V$ to $+16.5$, $V_{SS}=-5V$, $AGND=DGND=0V$, $VREF=+2V$ to $(V_{DD}-4V)$, unless otherwise specified.

NOTE 2: Characteristics supplied for use as a typical design limit but not production tested.

NOTE 3: Guaranteed monotonic to 8 bits.

NOTE 4: Settling time to $\pm 0.5LSB$.

NOTE 5: Timing shown in Figure 6 of Commercial Datasheet.

NOTE 6: Single-supply operation, $V_{DD}=+14.25V$ to $+15.75V$, $V_{SS}=AGND=DGND=0V$, $VREF=+10V$ unless otherwise specified.

MODE SELECTION:

\overline{WR}	A1	A0	SELECTED INPUT REGISTER
H	X	X	No operation. Device not selected
L	L	L	DAC A transparent
\uparrow	L	L	DAC A latched
L	L	H	DAC B transparent
\uparrow	L	H	DAC B latched
L	H	L	DAC C transparent
\uparrow	H	L	DAC C latched
L	H	H	DAC D transparent
\uparrow	H	H	DAC D latched

TERMINAL CONNECTIONS:

Pin	J20/L20	Pin	J20/L20
1	V_{OUTB}	11	D3
2	V_{OUTA}	12	D2
3	V_{SS}	13	D1
4	VREF	14	D0(LSB)
5	AGND	15	\overline{WR}
6	DGND	16	A1
7	D7(MSB)	17	A0
8	D6	18	V_{DD}
9	D5	19	V_{OUTD}
10	D4	20	V_{OUTC}

	Package	ORDERING INFORMATION:
01	20 pin CERDIP	MX7226TQ/883B
02	20 pin CERDIP	MX7226UQ/883B
01	20 pin LCC	MX7226TE/883B
02	20 pin LCC	MX7226UE/883B

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 4**, 9
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4, capacitance tests shall be tested at initial qualification and upon redesign.
Sample size will be 116 units.