
64M-BIT [4M x 16/8M x 8] CMOS EQUAL SECTOR FLASH MEMORY

FEATURES

GENERAL FEATURES

- 8M Bytes/4M Words switchable
- 128 Equal Sectors with 64K Bytes (32K words) each
 - Any combination of sectors can be erased with erase suspend/resume function
- Single Power Supply Operation
 - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1.0V to 1.5 x V_{cc}
- Low V_{cc} write inhibit is equal to or less than VLKO
- Compatible with JEDEC standard
 - Pinout and software compatible to single power supply Flash

PERFORMANCE

- High Performance
 - Access time: 90ns
 - Program time: 11 us/word
 - Erase time: 0.7s/sector, 45s/chip (typical)
- Low Power Consumption
 - Low active read current: 9mA (typical) at 5MHz
 - Low standby current: 5uA (typical)
- 100,000 erase/program cycles (typical)
- 10 years data retention

SOFTWARE FEATURES

- Support Common Flash Interface (CFI)
 - Flash device parameters stored on the device and provide the host system to access
- Erase Suspend/ Erase Resume
 - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
 - Data# polling & Toggle bits provide detection of program and erase operation completion or not

HARDWARE FEATURES

- Ready/Busy (RY/BY#) Output
 - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
 - Provides a hardware method to reset the internal state machine to read mode
- ACC input pin
 - Provides accelerated program capability
- WP#/ACC input
 - Write protect (WP#) function allows protection highest or lowest sector, regardless of sector protection settings

SECURITY

- Sector Protection/Chip Unprotect
 - Provides sector protect function to prevent program or erase operation in the protected sector
 - Provides chip unprotect function to allow code changes
 - Provides temporary sector unprotect function for code changes in previously protected sector
- Sector Permanent Lock
 - A unique lock bit feature allows the content to be permanently locked

(Please contact Macronix sales for specific information regarding this permanent lock feature)

- Secured Silicon Sector
 - Provides a 128-word area for code or data that can be permanently protected
 - Once this sector is protected, it is prohibited to program or erase within the sector again

PACKAGE

- 64-ball BGA
- **All Pb-free devices are RoHS Compliant**

GENERAL DESCRIPTION

MX29LA641D H/L is a 64Mbit flash memory that can be organized as 8Mbytes of 8 bits each or as 4Mbytes of 16 bits each. These devices operate over a voltage range of 2.7V to 3.6V typically using a 3V power supply input. The memory array is divided into 128 equal 64 Kilo byte blocks.

The MX29LA641D H/L is offered in a 64-ball BGA(LFBGA) JEDEC standard package. The package is offered in leaded, as well as lead-free version that is compliant to the RoHS specifications. The software algorithm used for this device also adheres to the JEDEC standard for single power supply devices. These flash parts can be programmed in system or on commercially available EPROM/Flash programmers.

Separate OE# and CEx (Output Enable and Chip Enable) signals are provided to simplify system design. When used with high speed processors, the 90ns read access time of this flash memory permits operation with minimal time lost due to system timing delays.

The automatic write algorithm provided on Macronix flash memories perform an automatic erase prior to write. The user only needs to provide a write command to the command register. The on-chip state machine automatically controls the program and erase functions including all necessary internal timings. Since erase and write operations take much longer time than read operations, erase/write can be interrupted to perform read operations in other sectors of the device. For this, Erase Suspend operation along with Erase Resume operation are provided. Data# polling or Toggle bits are used to indicate the end of the erase/write operation.

The device is manufactured at the Macronix fabrication facility using the time tested and proven MXIC advanced technology. This proprietary non-epi process provides a very high degree of latch-up protection for stresses up to 100 milliamperes on address and data pins from -1V to 1.5xVCC.

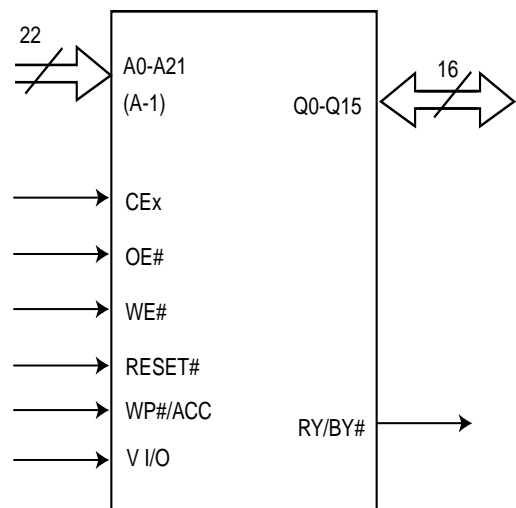
With low power consumption and enhanced hardware and software features, this flash memory retains data reliably for at least ten years. Erase and programming functions have been tested to meet a typical specification of 100,000 cycles of operation.

PIN CONFIGURATION

Please contact Macronix sales for specific information regarding 64-ball BGA (10x13mm) package pin configuration.

PIN DESCRIPTION

| SYMBOL | PIN NAME |
|------------|--|
| A0~A21/A-1 | Address Input/LSB addr (Byte Mode) |
| Q0~Q15 | 16 Data Inputs/Outputs |
| CE0~CE2 | Chip Enable Input (CE _x) |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| RESET# | Hardware Reset Pin, Active Low |
| WP#/ACC | Hardware Write Protect Input/ Hardware Acceleration Pin |
| RY/BY# | Read/Busy Output |
| BYTE# | Select 8 bit or 16 bit mode |
| VCC | +3.0V single power supply |
| V I/O | Output Power Supply (2.7V~3.6V), which is tied to VCC |
| GND | Device Ground |
| NC | Pin Not Connected Internally |

LOGIC SYMBOL

Chip Enable Truth Table

| DEVICE | CE0 | CE1 | CE2 |
|---------------|------------|------------|------------|
| Enabled | VIL | VIL | VIL |
| Disabled | VIL | VIH | VIL |
| Enabled | VIL | VIL | VIH |
| Enabled | VIL | VIH | VIH |
| Disabled | VIH | VIL | VIL |
| Disabled | VIH | VIH | VIL |
| Enabled | VIH | VIL | VIH |
| Disabled | VIH | VIH | VIH |

Note: For Single-chip applications, CE2 and CE1 can be strapped to GND.

BLOCK DIAGRAM

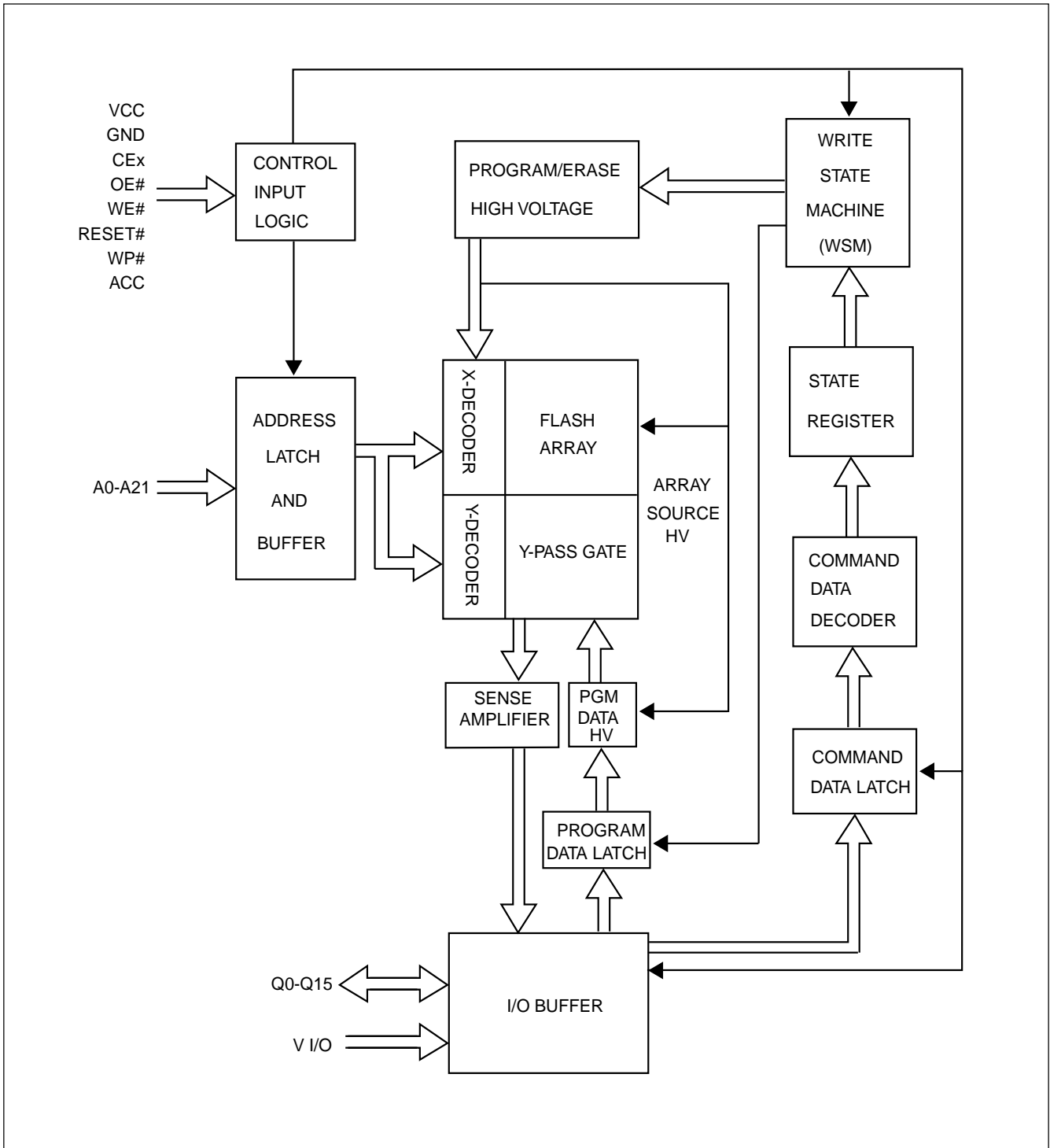


Table 1. BLOCK STRUCTURE

MX29LA641D SECTOR ARCHITECTURE

| Sector Size | | Sector | Sector Address A21-A15 | (x8) | (x16) |
|-------------|--------|--------|---------------------------|-----------------|-----------------|
| Kbytes | Kwords | | | Address Range | Address Range |
| 64 | 32 | SA0 | 0000000 | 000000h-00FFFFh | 000000h-007FFFh |
| 64 | 32 | SA1 | 0000001 | 010000h-01FFFFh | 008000h-00FFFFh |
| 64 | 32 | SA2 | 0000010 | 020000h-02FFFFh | 010000h-017FFFh |
| 64 | 32 | SA3 | 0000011 | 030000h-03FFFFh | 018000h-01FFFFh |
| 64 | 32 | SA4 | 0000100 | 040000h-04FFFFh | 020000h-027FFFh |
| 64 | 32 | SA5 | 0000101 | 050000h-05FFFFh | 028000h-02FFFFh |
| 64 | 32 | SA6 | 0000110 | 060000h-06FFFFh | 030000h-037FFFh |
| 64 | 32 | SA7 | 0000111 | 070000h-07FFFFh | 038000h-03FFFFh |
| 64 | 32 | SA8 | 0001000 | 080000h-08FFFFh | 040000h-047FFFh |
| 64 | 32 | SA9 | 0001001 | 090000h-09FFFFh | 048000h-04FFFFh |
| 64 | 32 | SA10 | 0001010 | 0A0000h-0AFFFFh | 050000h-057FFFh |
| 64 | 32 | SA11 | 0001011 | 0B0000h-0BFFFFh | 058000h-05FFFFh |
| 64 | 32 | SA12 | 0001100 | 0C0000h-0CFFFFh | 060000h-067FFFh |
| 64 | 32 | SA13 | 0001101 | 0D0000h-0DFFFFh | 068000h-06FFFFh |
| 64 | 32 | SA14 | 0001110 | 0E0000h-0EFFFFh | 070000h-077FFFh |
| 64 | 32 | SA15 | 0001111 | 0F0000h-0FFFFFh | 078000h-07FFFFh |
| 64 | 32 | SA16 | 0010000 | 100000h-10FFFFh | 080000h-087FFFh |
| 64 | 32 | SA17 | 0010001 | 110000h-11FFFFh | 088000h-08FFFFh |
| 64 | 32 | SA18 | 0010010 | 120000h-12FFFFh | 090000h-097FFFh |
| 64 | 32 | SA19 | 0010011 | 130000h-13FFFFh | 098000h-09FFFFh |
| 64 | 32 | SA20 | 0010100 | 140000h-14FFFFh | 0A0000h-0A7FFFh |
| 64 | 32 | SA21 | 0010101 | 150000h-15FFFFh | 0A8000h-0AFFFFh |
| 64 | 32 | SA22 | 0010110 | 160000h-16FFFFh | 0B0000h-0B7FFFh |
| 64 | 32 | SA23 | 0010111 | 170000h-17FFFFh | 0B8000h-0BFFFFh |
| 64 | 32 | SA24 | 0011000 | 180000h-18FFFFh | 0C0000h-0C7FFFh |
| 64 | 32 | SA25 | 0011001 | 190000h-19FFFFh | 0C8000h-0CFFFFh |
| 64 | 32 | SA26 | 0011010 | 1A0000h-1AFFFFh | 0D0000h-0D7FFFh |
| 64 | 32 | SA27 | 0011011 | 1B0000h-1BFFFFh | 0D8000h-0DFFFFh |
| 64 | 32 | SA28 | 0011100 | 1C0000h-1CFFFFh | 0E0000h-0E7FFFh |
| 64 | 32 | SA29 | 0011101 | 1D0000h-1DFFFFh | 0E8000h-0EFFFFh |
| 64 | 32 | SA30 | 0011110 | 1E0000h-1EFFFFh | 0F0000h-0F7FFFh |
| 64 | 32 | SA31 | 0011111 | 1F0000h-1FFFFFh | 0F8000h-0FFFFFh |
| 64 | 32 | SA32 | 0100000 | 200000h-20FFFFh | 100000h-107FFFh |
| 64 | 32 | SA33 | 0100001 | 210000h-21FFFFh | 108000h-10FFFFh |
| 64 | 32 | SA34 | 0100010 | 220000h-22FFFFh | 110000h-117FFFh |
| 64 | 32 | SA35 | 0100011 | 230000h-23FFFFh | 118000h-11FFFFh |
| 64 | 32 | SA36 | 0100100 | 240000h-24FFFFh | 120000h-127FFFh |
| 64 | 32 | SA37 | 0100101 | 250000h-25FFFFh | 128000h-12FFFFh |



| Sector Size | | Sector | Sector Address A21-A15 | (x8) | (x16) |
|-------------|--------|--------|---------------------------|-----------------|-----------------|
| Kbytes | Kwords | | | Address Range | Address Range |
| 64 | 32 | SA38 | 0100110 | 260000h-26FFFFh | 130000h-137FFFh |
| 64 | 32 | SA39 | 0100111 | 270000h-27FFFFh | 138000h-13FFFFh |
| 64 | 32 | SA40 | 0101000 | 280000h-28FFFFh | 140000h-147FFFh |
| 64 | 32 | SA41 | 0101001 | 290000h-29FFFFh | 148000h-14FFFFh |
| 64 | 32 | SA42 | 0101010 | 2A0000h-2AFFFFh | 150000h-157FFFh |
| 64 | 32 | SA43 | 0101011 | 2B0000h-2BFFFFh | 158000h-15FFFFh |
| 64 | 32 | SA44 | 0101100 | 2C0000h-2CFFFFh | 160000h-167FFFh |
| 64 | 32 | SA45 | 0101101 | 2D0000h-2DFFFFh | 168000h-16FFFFh |
| 64 | 32 | SA46 | 0101110 | 2E0000h-2EFFFFh | 170000h-177FFFh |
| 64 | 32 | SA47 | 0101111 | 2F0000h-2FFFFFh | 178000h-17FFFFh |
| 64 | 32 | SA48 | 0110000 | 300000h-30FFFFh | 180000h-187FFFh |
| 64 | 32 | SA49 | 0110001 | 310000h-31FFFFh | 188000h-18FFFFh |
| 64 | 32 | SA50 | 0110010 | 320000h-32FFFFh | 190000h-197FFFh |
| 64 | 32 | SA51 | 0110011 | 330000h-33FFFFh | 198000h-19FFFFh |
| 64 | 32 | SA52 | 0110100 | 340000h-34FFFFh | 1A0000h-1A7FFFh |
| 64 | 32 | SA53 | 0110101 | 350000h-35FFFFh | 1A8000h-1AFFFFh |
| 64 | 32 | SA54 | 0110110 | 360000h-36FFFFh | 1B0000h-1B7FFFh |
| 64 | 32 | SA55 | 0110111 | 370000h-37FFFFh | 1B8000h-1BFFFFh |
| 64 | 32 | SA56 | 0111000 | 380000h-38FFFFh | 1C0000h-1C7FFFh |
| 64 | 32 | SA57 | 0111001 | 390000h-39FFFFh | 1C8000h-1CFFFFh |
| 64 | 32 | SA58 | 0111010 | 3A0000h-3AFFFFh | 1D0000h-1D7FFFh |
| 64 | 32 | SA59 | 0111011 | 3B0000h-3BFFFFh | 1D8000h-1DFFFFh |
| 64 | 32 | SA60 | 0111100 | 3C0000h-3CFFFFh | 1E0000h-1E7FFFh |
| 64 | 32 | SA61 | 0111101 | 3D0000h-3DFFFFh | 1E8000h-1EFFFFh |
| 64 | 32 | SA62 | 0111110 | 3E0000h-3EFFFFh | 1F0000h-1F7FFFh |
| 64 | 32 | SA63 | 0111111 | 3F0000h-3FFFFFh | 1F8000h-1FFFFFh |
| 64 | 32 | SA64 | 1000000 | 400000h-40FFFFh | 200000h-207FFFh |
| 64 | 32 | SA65 | 1000001 | 410000h-41FFFFh | 208000h-20FFFFh |
| 64 | 32 | SA66 | 1000010 | 420000h-42FFFFh | 210000h-217FFFh |
| 64 | 32 | SA67 | 1000011 | 430000h-43FFFFh | 218000h-21FFFFh |
| 64 | 32 | SA68 | 1000100 | 440000h-44FFFFh | 220000h-227FFFh |
| 64 | 32 | SA69 | 1000101 | 450000h-45FFFFh | 228000h-22FFFFh |
| 64 | 32 | SA70 | 1000110 | 460000h-46FFFFh | 230000h-237FFFh |
| 64 | 32 | SA71 | 1000111 | 470000h-47FFFFh | 238000h-23FFFFh |
| 64 | 32 | SA72 | 1001000 | 480000h-48FFFFh | 240000h-247FFFh |
| 64 | 32 | SA73 | 1001001 | 490000h-49FFFFh | 248000h-24FFFFh |
| 64 | 32 | SA74 | 1001010 | 4A0000h-4AFFFFh | 250000h-257FFFh |
| 64 | 32 | SA75 | 1001011 | 4B0000h-4BFFFFh | 258000h-25FFFFh |
| 64 | 32 | SA76 | 1001100 | 4C0000h-4CFFFFh | 260000h-267FFFh |
| 64 | 32 | SA77 | 1001101 | 4D0000h-4DFFFFh | 268000h-26FFFFh |



| Sector Size | | Sector | Sector Address A21-A15 | (x8) | (x16) |
|-------------|--------|--------|---------------------------|------------------|------------------|
| Kbytes | Kwords | | | Address Range | Address Range |
| 64 | 32 | SA78 | 1001110 | 4E0000h-4EFFFFh | 270000h-277FFFh |
| 64 | 32 | SA79 | 1001111 | 4F0000h-4FFFFFFh | 278000h-27FFFFh |
| 64 | 32 | SA80 | 1010000 | 500000h-50FFFFh | 280000h-287FFFh |
| 64 | 32 | SA81 | 1010001 | 510000h-51FFFFh | 288000h-28FFFFh |
| 64 | 32 | SA82 | 1010010 | 520000h-52FFFFh | 290000h-297FFFh |
| 64 | 32 | SA83 | 1010011 | 530000h-53FFFFh | 298000h-29FFFFh |
| 64 | 32 | SA84 | 1010100 | 540000h-54FFFFh | 2A0000h-2A7FFFh |
| 64 | 32 | SA85 | 1010101 | 550000h-55FFFFh | 2A8000h-2AFFFFh |
| 64 | 32 | SA86 | 1010110 | 560000h-56FFFFh | 2B0000h-2B7FFFh |
| 64 | 32 | SA87 | 1010111 | 570000h-57FFFFh | 2B8000h-2BFFFFh |
| 64 | 32 | SA88 | 1011000 | 580000h-58FFFFh | 2C0000h-2C7FFFh |
| 64 | 32 | SA89 | 1011001 | 590000h-59FFFFh | 2C8000h-2CFFFFh |
| 64 | 32 | SA90 | 1011010 | 5A0000h-5AFFFFh | 2D0000h-2D7FFFh |
| 64 | 32 | SA91 | 1011011 | 5B0000h-5BFFFFh | 2D8000h-2DFFFFh |
| 64 | 32 | SA92 | 1011100 | 5C0000h-5CFFFFh | 2E0000h-2E7FFFh |
| 64 | 32 | SA93 | 1011101 | 5D0000h-5DFFFFh | 2E8000h-2EFFFFh |
| 64 | 32 | SA94 | 1011110 | 5E0000h-5EFFFFh | 2F0000h-2F7FFFh |
| 64 | 32 | SA95 | 1011111 | 5F0000h-5FFFFFFh | 2F8000h-2FFFFFFh |
| 64 | 32 | SA96 | 1100000 | 600000h-60FFFFh | 300000h-307FFFh |
| 64 | 32 | SA97 | 1100001 | 610000h-61FFFFh | 308000h-30FFFFh |
| 64 | 32 | SA98 | 1100010 | 620000h-62FFFFh | 310000h-317FFFh |
| 64 | 32 | SA99 | 1100011 | 630000h-63FFFFh | 318000h-31FFFFh |
| 64 | 32 | SA100 | 1100100 | 640000h-64FFFFh | 320000h-327FFFh |
| 64 | 32 | SA101 | 1100101 | 650000h-65FFFFh | 328000h-32FFFFh |
| 64 | 32 | SA102 | 1100110 | 660000h-66FFFFh | 330000h-337FFFh |
| 64 | 32 | SA103 | 1100111 | 670000h-67FFFFh | 338000h-33FFFFh |
| 64 | 32 | SA104 | 1101000 | 680000h-68FFFFh | 340000h-347FFFh |
| 64 | 32 | SA105 | 1101001 | 690000h-69FFFFh | 348000h-34FFFFh |
| 64 | 32 | SA106 | 1101010 | 6A0000h-6AFFFFh | 350000h-357FFFh |
| 64 | 32 | SA107 | 1101011 | 6B0000h-6BFFFFh | 358000h-35FFFFh |
| 64 | 32 | SA108 | 1101100 | 6C0000h-6CFFFFh | 360000h-367FFFh |
| 64 | 32 | SA109 | 1101101 | 6D0000h-6DFFFFh | 368000h-36FFFFh |
| 64 | 32 | SA110 | 1101110 | 6E0000h-6EFFFFh | 370000h-377FFFh |
| 64 | 32 | SA111 | 1101111 | 6F0000h-6FFFFFFh | 378000h-37FFFFh |
| 64 | 32 | SA112 | 1110000 | 700000h-70FFFFh | 380000h-387FFFh |
| 64 | 32 | SA113 | 1110001 | 710000h-71FFFFh | 388000h-38FFFFh |
| 64 | 32 | SA114 | 1110010 | 720000h-72FFFFh | 390000h-397FFFh |
| 64 | 32 | SA115 | 1110011 | 730000h-73FFFFh | 398000h-39FFFFh |
| 64 | 32 | SA116 | 1110100 | 740000h-74FFFFh | 3A0000h-3A7FFFh |
| 64 | 32 | SA117 | 1110101 | 750000h-75FFFFh | 3A8000h-3AFFFFh |



| Sector Size | | Sector | Sector Address A21-A15 | (x8) | (x16) |
|-------------|--------|--------|---------------------------|------------------|------------------|
| Kbytes | Kwords | | | Address Range | Address Range |
| 64 | 32 | SA118 | 1110110 | 760000h-76FFFFh | 3B0000h-3B7FFFh |
| 64 | 32 | SA119 | 1110111 | 770000h-77FFFFh | 3B8000h-3BFFFFh |
| 64 | 32 | SA120 | 1111000 | 780000h-78FFFFh | 3C0000h-3C7FFFh |
| 64 | 32 | SA121 | 1111001 | 790000h-79FFFFh | 3C8000h-3CFFFFh |
| 64 | 32 | SA122 | 1111010 | 7A0000h-7AFFFFh | 3D0000h-3D7FFFh |
| 64 | 32 | SA123 | 1111011 | 7B0000h-7BFFFFh | 3D8000h-3DFFFFh |
| 64 | 32 | SA124 | 1111100 | 7C0000h-7CFFFFh | 3E0000h-3E7FFFh |
| 64 | 32 | SA125 | 1111101 | 7D0000h-7DFFFFh | 3E8000h-3EFFFFh |
| 64 | 32 | SA126 | 1111110 | 7E0000h-7EFFFFh | 3F0000h-3F7FFFh |
| 64 | 32 | SA127 | 1111111 | 7F0000h-7FFFFFFh | 3F8000h-3FFFFFFh |

BUS OPERATION

Table 2-1. BUS OPERATION

| Mode Select | RESET# | CE _x | WE# | OE# | Address | Q8~Q15 | | Data (I/O) | WP#/ |
|----------------------------|-----------------------|-----------------|-----|-----|--|--------|------------------|------------|-----------------|
| | | | | | | Word | Byte | Q0~Q7 | ACC |
| Device Reset | L | X | X | X | X | HighZ | HighZ | HighZ | L/H |
| Standby Mode | V _{cc} ±0.3V | disable | X | X | X | HighZ | HighZ | HighZ | H |
| Output Disable | H | enable | H | H | X | HighZ | HighZ | HighZ | L/H |
| Read Mode | H | enable | H | L | AIN | DOUT | Q8~Q15 =HighZ | DOUT | L/H |
| Write (Program/Erase) | H | enable | L | H | AIN | Note 3 | Q8~Q15 =HighZ | Note 3 | Note 2 |
| Accelerate Program | H | enable | L | H | AIN | Note 3 | Q8~Q15 =HighZ | Note 3 | V _{hv} |
| Temporary Sector Unprotect | V _{hv} | X | X | X | AIN | Note 3 | HighZ | Note 3 | Note 2 |
| Sector Protect (Note 2) | V _{hv} | enable | L | H | Sector Address, A6=L, A1=H, A0=L | X | X | Note 3 | H |
| Chip Unprotect (Note 2) | V _{hv} | enable | L | H | Sector Address, A6=H, A1=H, A0=L | X | X | Note 3 | H |

Legend:

L=Logic LOW=V_{il}, H=Logic High=V_{ih}, V_{hv}=10.0±0.5V, X=Don't Care, AIN=Address IN, DIN=Data IN, DOUT=Data OUT

Notes:

1. Through programming equipment, the sector protect and chip unprotect functions can also be implemented.
2. If WP#=L, all sectors are protected. If WP# remove to H, all sectors recover previous protected or unprotected status, determined by "sector protect" or "chip unprotect" function.
3. By following the requests of command sequence, sector protection, or data polling algorithm, Q0~Q15 would be Data Input or Data Output.
4. In Word mode, A21~A0 are address pins. In Byte mode A21~A-1 are address pins. In both modes, A21~A15 are sector address.

Table 2-2. BUS OPERATION

| Description | Control Input | | | A21 to A15 | A14 to A10 | A9 | A8 to A7 | A6 | A5 to A4 | A3 to A2 | A1 | A0 | Q8 to Q15 | Q7 to Q0 | |
|---|---------------|-----|-----|------------------|------------------|-----|----------------|----|----------------|----------------|----|----|-----------------|----------------|-----|
| | CEx | OE# | WE# | | | | | | | | | | | | |
| Sector Lock Status Verification | enable | L | H | SA | X | Vhv | X | L | X | L | H | L | X | Note 1 | |
| Read Indicator Bit(Q7) For Security Sector | enable | L | H | X | X | Vhv | X | L | X | L | H | H | X | Note 2 | |
| Read Manufacturer ID | enable | L | H | X | X | Vhv | X | L | X | L | L | L | 00 | C2h | |
| Read Device ID--- | | | | | | | | | | | | | | | |
| 1st cycle | enable | L | H | X | X | Vhv | X | L | X | L | L | H | 22 | 7Eh | |
| 2nd cycle | | | | | | | | | | H | H | L | 22 | 13h | |
| 3rd cycle | | | | | | | | | | 641DH | H | H | H | 22 | 01h |
| | | | | | | | | | | 641DL | H | H | H | 22 | 00h |

Legend: L=Logic Low=VIL, H=Logic High=VIH, SA=Sector Address, X=Don't care.

Notes:

- Sector unprotected code: 00h, sector protected code:01h.
- Factory locked code: For 29LA641DL: 88h.
For 29LA641DH: 98h.
Factory unlocked code: For 29LA641DL: 08h.
For 29LA641DH: 18h.

WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CEx to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of CEx and WE#, and all data are latched at the earlier rising edge of CE# and WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in the array, it has to drive CEx (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CEx or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped temporarily after a period of time no more than Tready and the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased.

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.
2. The device is in auto select mode or CFI mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

ACCELERATED PROGRAM OPERATION

The accelerated program can improve programming performance compared with word/byte program. By applying Vhv on WP#/ACC pin, the device will enter accelerated program and draw current no more than IACC from WP#/ACC pin. Removing the Vhv from WP#/ACC pin will put the device back to normal operation (not accelerated).

RESET# OPERATION

Driving RESET# pin low for a period more than T_{rp} will reset the device back to read mode. If the device is in program or erase operation, the reset operation will take at most a period of T_{ready} for the device to return to read array mode. Before the device returns to read array mode, the RY/BY# pin remains low (busy status).

When RESET# pin is held at $GND \pm 0.3V$, the device consumes standby current (I_{sb}). However, device draws larger current if RESET# pin is held at V_{il} but not within $GND \pm 0.3V$.

It is recommended that the system to tie its reset signal to RESET# pin of flash memory, so that the flash memory will be reset during system reset and allows system to read the boot-up firmware from flash memory.

SECTOR PROTECT OPERATION

When a sector is protected, program or erase operation will be disabled on these sectors. MX29LA641D H/L provides two methods for sector protection.

Once the sector is protected, the sector remains protected until next chip unprotect, or is temporarily unprotected by asserting RESET# pin at V_{hv} . Refer to temporary sector unprotect operation for further details.

The first method is by applying V_{hv} on RESET# pin. Refer to Figure 14 for timing diagram and Figure 15 for the algorithm for this method.

The other method is asserting V_{hv} on A9 and OE# pins, with A6 and CEx at V_{il} . The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

CHIP UNPROTECT OPERATION

MX29LA641D H/L provides two methods for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sectors groups are unprotected when shipped from the factory.

The first method is by applying V_{hv} on RESET# pin. Refer to Figure 14 for timing diagram and Figure 15 for algorithm of the operation.

The other method is asserting V_{hv} on A9 and OE# pins, with A6 at V_{ih} and CE# at V_{il} (see Table 2). The unprotect operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

TEMPORARY SECTOR UNPROTECT OPERATION

System can apply RESET# pin at V_{hv} to place the device in temporary unprotect mode. In this mode, previously protected sectors can be programmed or erased just as it is unprotected. The device returns to normal operation once V_{hv} is removed from RESET# pin and previously protected sectors are again protected.

WRITE PROTECT (WP#)

This Write Protect function provides a hardware protection method to protect all sectors without using Vhv.

By driving the WP#/ACC pin Low, the device disable program and erase function in all sectors. If the WP#/ACC is held high (Vih to Vcc), these sectors revert to their previous protected/unprotected status.

AUTOMATIC SELECT OPERATION

When the device is in Read array mode, erase-suspended read array mode or CFI mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

MX29LA641D H/L provides hardware method to access the silicon ID read operation. Which method requires Vhv on A9 pin, Vil on CEx, OE# and A6 pins. Which apply A1=Vil, A0=Vil, the device will output MXIC's manufacture code of C2h. Which apply A1=Vil, A0=Vih, the device will output device code of 227Eh. Table 2 shows the sequence for reading MX29LA641D H/L device codes.

VERIFY SECTOR PROTECT STATUS OPERATION

MX29LA641D H/L provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires Vhv on A9 pin, Vih on WE# and A1 pins, Vil on CEx, OE#, A6 and A0 pins, and sector address on A15 to A21 pins. If the read out data is 01H, the designated sector is protected. Oppositely, if the read out data is 00H, the designated sector is not protected.

SECURITY SECTOR FLASH MEMORY REGION

The Security Sector region is an extra OTP memory space of 128 words in length. The security sectors can be locked upon shipping from factory, or it can be locked by customer after shipping. Customer can issue Security Sector Factory Protect Verify and/or Security Sector Protect Verify to query the lock status of the device.

In factory-locked device, security sector region is protected when shipped from factory and the security silicon sector indicator bit is set to "1". In customer lockable device, security sector region is unprotected when shipped from factory and the security silicon indicator bit is set to "0".

Factory Locked: Security Sector Programmed and Protected at the Factory

In a factory locked device, the security silicon region is permanently locked after shipping from factory. The device will have a 16-byte (8-word) ESN in the security region at address : 000000h - 000007h.

The secured silicon sector address space in this device is allocated as follows.

| Secured Silicon Sector Address Range | Standard Factory Locked | Express Flash Factory Locked | Customer Lockable |
|--------------------------------------|-------------------------|-------------------------------|------------------------|
| 000000h-000007h | ESN | ESN or Determined by Customer | Determined by Customer |
| 000008h-00007Fh | Unavailable | Determined by Customer | |

Customer Lockable: Security Sector NOT Programmed or Protected at the Factory

When the security feature is not required, the security region can act as an extra memory space.

Security silicon sector can also be protected by two methods. Note that once the security silicon sector is protected, there is no way to unprotect the security silicon sector and the content of it can no longer be altered.

The first method is to write a three-cycle command of Enter Security Region, and then follow the sector protect algorithm as illustrated in Figure 15, except that RESET# pin may at either Vih or Vhv.

The other method is to write a three-cycle command of Enter Security Region, and then follow the alternate method of sector protect with A9, OE# at Vhv.

After the security silicon is locked and verified, system must write Exit Security Sector Region, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.

DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than VLKO. This prevents data from spuriously altered. The device automatically resets itself when Vcc is lower than VLKO and write cycles are ignored until Vcc is greater than VLKO. System must provide proper signals on control pins after Vcc is larger than VLKO to avoid unintentional program or erase operation

WRITE PULSE "GLITCH" PROTECTION

CEx, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CEx and WE# at Vil with OE# at Vih. Write cycle is ignored when either CEx at Vih, WE# a Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, MX29LA641D H/L is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.



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POWER-UP WRITE INHIBIT

When WE#, CEx is held at V_{il} and OE# is held at V_{ih} during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the V_{cc} and GND to reduce the noise effect.

SOFTWARE COMMAND DEFINITIONS

Table 3 indicates all valid command sequences. Please note that if you give wrong address and data, or write them by wrong command sequence, the device will be reset into read mode.

While WE# or CEx goes low, the falling edge of which happens later will latch all address. While WE# or CEx goes high, and the rising edge of which happens first will latch all data.

TABLE 3. MX29LA641D H/L COMMAND DEFINITIONS

| Command | | Read Mode | Reset Mode | Automatic Select | | | | | | | | | | | |
|-------------|------|-----------|------------|------------------|------|---------------------|------|--|-----------|-----------------------|-------|-----|-----|----------|----------|
| | | | | Manufacturer ID | | Device ID (* Notes) | | Security Sector Factory Protect Verify | | Sector Protect Verify | | | | | |
| | | | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | | | | |
| 1st Bus Cyc | Hex | | | | | | | | | | | | | | |
| | Addr | Addr | XXX | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | | |
| | Data | Data | F0 | AA | AA | AA | AA | AA | AA | AA | AA | AA | AA | AA | AA |
| 2nd Bus Cyc | Addr | | | 2AA | 555 | 2AA | 555 | 2AA | 555 | 2AA | 555 | 2AA | 555 | | |
| | Data | | | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 |
| 3rd Bus Cyc | Addr | | | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | | |
| | Data | | | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 |
| 4th Bus Cyc | Addr | | | X00 | X00 | X01 | X02 | X03 | X06 | | | | | (Sector) | (Sector) |
| | Data | | | C2H | C2H | ID1 | ID1 | 98/18 (H) | 98/18 (H) | 00/01 | 00/01 | | | | |
| | | | | | | | | 88/08 (L) | 88/08 (L) | | | | | | |
| 5th Bus Cyc | Addr | | | | | X0E | X1C | | | | | | | | |
| | Data | | | | | ID2 | ID2 | | | | | | | | |
| 6th Bus Cyc | Addr | | | | | X0F | X1E | | | | | | | | |
| | Data | | | | | ID3 | ID3 | | | | | | | | |

| Command | | Enter Security Sector Region Enable | | Exit Security Sector | | Program | | Chip Erase | | Sector Erase | | CFI Read | | Erase Suspend | Erase Resume |
|-------------|------|-------------------------------------|------|----------------------|------|---------|------|------------|------|--------------|--------|----------|------|---------------|--------------|
| | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Byte/Word | Byte/Word |
| 1st Bus Cyc | Hex | | | | | | | | | | | | | | |
| | Addr | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | 55 | AA | XXX | XXX |
| | Data | AA | AA | AA | AA | AA | AA | AA | AA | AA | AA | 98 | 98 | B0 | 30 |
| 2nd Bus Cyc | Addr | 2AA | 555 | 2AA | 555 | 2AA | 555 | 2AA | 555 | 2AA | 555 | | | | |
| | Data | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | | | | |
| 3rd Bus Cyc | Addr | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | | | | |
| | Data | 88 | 88 | 90 | 90 | A0 | A0 | 80 | 80 | 80 | 80 | | | | |
| 4th Bus Cyc | Addr | | | XXX | XXX | Addr | Addr | 555 | AAA | 555 | AAA | | | | |
| | Data | | | 00 | 00 | Data | Data | AA | AA | AA | AA | | | | |
| 5th Bus Cyc | Addr | | | | | | | 2AA | 555 | 2AA | 555 | | | | |
| | Data | | | | | | | 55 | 55 | 55 | 55 | | | | |
| 6th Bus Cyc | Addr | | | | | | | 555 | AAA | Sector | Sector | | | | |
| | Data | | | | | | | 10 | 10 | 30 | 30 | | | | |



Notes:

| Device ID | ID1 | | ID2 | | ID3 | |
|-------------|------|------|------|------|------|------|
| | Word | Byte | Word | Byte | Word | Byte |
| MX29LA641DH | 227E | 7E | 2213 | 13 | 2201 | 01 |
| MX29LA641DL | 227E | 7E | 2213 | 13 | 2200 | 00 |

RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not secured silicon is locked and whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

| Identifier Code | Word/Byte Mode | Address | Data (Hex) | Representation |
|-----------------------|----------------|-----------------------|------------------------|-------------------------|
| Manufacturer ID | Word | X00 | C2 | |
| | Byte | X00 | C2 | |
| Device ID, cycle 1 | Word | X01 | 227E | |
| | Byte | X02 | 7E | |
| Device ID, cycle 2 | Word | X0E | 2213 | |
| | Byte | X1C | 13 | |
| Device ID, cycle 3 | Word | X0F | 2201/2200 | 29LA641D H/L |
| | Byte | X1E | 01/00 | |
| Secured Silicon | Word | X03 | 98/18 (H) 88/08 (L) | Factory locked/unlocked |
| | Byte | X06 | 98/18 (H) 88/08 (L) | Factory locked/unlocked |
| Sector Protect Verify | Word | (Sector address) X 02 | 00/01 | Unprotected/protected |
| | Byte | (Sector address) X 04 | 00/01 | Unprotected/protected |

There is an alternative method to that shown in Table 2, which is intended for EPROM programmers and requires V_{hh} on address bit A9.

AUTOMATIC PROGRAMMING

The MX29LA641D H/L can provide the user program function by the form of Byte-Mode or Word-Mode. As long as the users enter the right cycle defined in the Table.3 (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming. With the internal write state controller, the device requires the user to write the program command and data only.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

The typical chip program time at room temperature of the MX29LA641D H/L is less than 45 seconds.

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

| Status | Q7 | Q6 | Q5 | RY/BY#*2 |
|-------------------|-----|---------------|----|----------|
| In progress*1 | Q7# | Toggling | 0 | 0 |
| Finished | Q7 | Stop toggling | 0 | 1 |
| Exceed time limit | Q7# | Toggling | 1 | 0 |

*1: The status "in progress" means both program mode and erase-suspended program mode.

*2: RY/BY# is an open drain output pin and should be weakly connected to VDD through a pull-up resistor.

*3: When an attempt is made to program a protected sector, Q7 will output its complement data or Q6 continues to toggle for about 1us or less and the device returns to read array state without programming the data in the protected sector.

CHIP ERASE

Chip Erase is to erase all the data with "1" and "0" as all "1". It needs 6 cycles to write the action in, and the first two cycles are "unlock" cycles, the third one is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle is the chip erase operation.

During chip erasing, all the commands will not be accepted except hardware reset or the working voltage is too low that chip erase will be interrupted. After Chip Erase, the chip will return to the state of Read Array.

When the embedded chip erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

| Status | Q7 | Q6 | Q5 | Q2 | RY/BY# |
|-------------------|----|---------------|----|----------|--------|
| In progress | 0 | Toggling | 0 | Toggling | 0 |
| Finished | 1 | Stop toggling | 0 | 1 | 1 |
| Exceed time limit | 0 | Toggling | 1 | Toggling | 0 |

SECTOR ERASE

Sector Erase is to erase all the data in a sector with "1" and "0" as all "1". It requires six command cycles to issue. The first two cycles are "unlock cycles", the third one is a configuration cycle, the fourth and fifth are also "unlock cycles" and the sixth cycle is the sector erase command. After the sector erase command sequence is issued, there is a time-out period of 50us counted internally. During the time-out period, additional sector address and sector erase command can be written multiply. Once user enters another sector erase command, the time-out period of 50us is recounted. If user enters any command other than sector erase or erase suspend during time-out period, the erase command would be aborted and the device is reset to read array condition. The number of sectors could be from one sector to all sectors. After time-out period passing by, additional erase command is not accepted and erase embedded operation begins.

During sector erasing, all commands will not be accepted except hardware reset and erase suspend and user can check the status as chip erase.

When the embedded erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

| Status | Q7 | Q6 | Q5 | Q3 | Q2 | RY/BY#*2 |
|-------------------|----|---------------|----|----|----------|----------|
| Time-out period | 0 | Toggling | 0 | 0 | Toggling | 0 |
| In progress | 0 | Toggling | 0 | 1 | Toggling | 0 |
| Finished | 1 | Stop toggling | 0 | 1 | 1 | 1 |
| Exceed time limit | 0 | Toggling | 1 | 1 | Toggling | 0 |

*1: The status Q3 is the time-out period indicator. When Q3=0, the device is in time-out period and is acceptable to another sector address to be erased. When Q3=1, the device is in erase operation and only erase suspend is valid.

*2: RY/BY# is open drain output pin and should be weakly connected to VDD through a pull-up resistor.

*3: When an attempt is made to erase a protected sector, Q7 will output its complement data or Q6 continues to toggle for 100us or less and the device returned to read array status without erasing the data in the protected sector.

SECTOR ERASE SUSPEND

During sector erasure, sector erase suspend is the only valid command. If user issue erase suspend command in the time-out period of sector erasure, device time-out period will be over immediately and the device will go back to erase-suspended read array mode. If user issue erase suspend command during the sector erase is being operated, device will suspend the ongoing erase operation, and after the Tready1 ($\leq 20\mu s$) suspend finishes and the device will enter erase-suspended read array mode. User can judge if the device has finished erase suspend through Q6, Q7, and RY/BY#.

After device has entered erase-suspended read array mode, user can read other sectors not at erase suspend by the speed of Taa; while reading the sector in erase-suspend mode, device will output its status. User can use Q6 and Q2 to judge the sector is erasing or the erase is suspended.

| Status | Q7 | Q6 | Q5 | Q3 | Q2 | RY/BY# |
|---|------|-----------|------|------|--------|--------|
| Erase suspend read in erase suspended sector | 1 | No toggle | 0 | N/A | Toggle | 1 |
| Erase suspend read in non-erase suspended sector | Data | Data | Data | Data | Data | 1 |
| Erase suspend program in non-erase suspended sector | Q7# | Toggle | 0 | N/A | N/A | 0 |

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

SECTOR ERASE RESUME

Sector erase resume command is valid only when the device is in erase suspend state. After erase resume, user can issue another erase suspend command, but there should be a 4ms interval between erase resume and the next erase suspend. If user issue infinite suspend-resume loop, or suspend-resume exceeds 1024 times, the time for erasing will increase.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LA641D H/L features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. The device enters the CFI Query mode when the system writes the CFI Query command "98H" to address "55H" any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4. A reset command is required to exit CFI mode and go back to ready array mode or erase suspend mode. The system can write the CFI Query command only when the device is in read mode, erase suspend, standby mode or automatic select mode.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

| Description | Address (h) | Address (h) | Data (h) |
|--|-------------|-------------|----------|
| | (Word Mode) | (Byte Mode) | |
| Query-unique ASCII string "QRY" | 10 | 20 | 0051 |
| | 11 | 22 | 0052 |
| | 12 | 24 | 0059 |
| Primary vendor command set and control interface ID code | 13 | 26 | 0002 |
| | 14 | 28 | 0000 |
| Address for primary algorithm extended query table | 15 | 2A | 0040 |
| | 16 | 2C | 0000 |
| Alternate vendor command set and control interface ID code | 17 | 2E | 0000 |
| | 18 | 30 | 0000 |
| Address for alternate algorithm extended query table | 19 | 32 | 0000 |
| | 1A | 34 | 0000 |

Table 4-2. CFI Mode: System Interface Data Values

| Description | Address (h) | Address (h) | Data (h) |
|--|-------------|-------------|----------|
| | (Word Mode) | (Byte Mode) | |
| Vcc supply minimum program/erase voltage | 1B | 36 | 0027 |
| Vcc supply maximum program/erase voltage | 1C | 38 | 0036 |
| VPP supply minimum program/erase voltage | 1D | 3A | 0000 |
| VPP supply maximum program/erase voltage | 1E | 3C | 0000 |
| Typical timeout per single word/byte write, 2 ⁿ us | 1F | 3E | 0004 |
| Typical timeout for maximum-size buffer write, 2 ⁿ us | 20 | 40 | 0000 |
| Typical timeout per individual block erase, 2 ⁿ ms | 21 | 42 | 000A |
| Typical timeout for full chip erase, 2 ⁿ ms | 22 | 44 | 0000 |
| Maximum timeout for word/byte write, 2 ⁿ times typical | 23 | 46 | 0005 |
| Maximum timeout for buffer write, 2 ⁿ times typical | 24 | 48 | 0000 |
| Maximum timeout per individual block erase, 2 ⁿ times typical | 25 | 4A | 0004 |
| Maximum timeout for chip erase, 2 ⁿ times typical | 26 | 4C | 0000 |

Table 4-3. CFI Mode: Device Geometry Data Values

| Description | Address (h) | Address (h) | Data (h) |
|--|-------------|-------------|----------|
| | (Word Mode) | (Byte Mode) | |
| Device size = 2 ⁿ in number of bytes | 27 | 4E | 0017 |
| Flash device interface description (02=asynchronous x8/x16) | 28 | 50 | 0002 |
| | 29 | 52 | 0000 |
| Maximum number of bytes in buffer write = 2 ⁿ (not support) | 2A | 54 | 0000 |
| | 2B | 56 | 0000 |
| Number of erase regions within device | 2C | 58 | 0001 |
| Index for Erase Bank Area 1 | 2D | 5A | 007F |
| [2E, 2D] = # of same-size sectors in region 1-1 | 2E | 5C | 0000 |
| [30, 2F] = sector size in multiples of 256-bytes | 2F | 5E | 0000 |
| | 30 | 60 | 0001 |
| Index for Erase Bank Area 2 | 31 | 62 | 0000 |
| | 32 | 64 | 0000 |
| | 33 | 66 | 0000 |
| | 34 | 68 | 0000 |
| Index for Erase Bank Area 3 | 35 | 6A | 0000 |
| | 36 | 6C | 0000 |
| | 37 | 6E | 0000 |
| | 38 | 70 | 0000 |
| Index for Erase Bank Area 4 | 39 | 72 | 0000 |
| | 3A | 74 | 0000 |
| | 3B | 76 | 0000 |
| | 3C | 78 | 0000 |

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

| Description | Address (h) | Address (h) | Data (h) |
|--|-------------|-------------|----------|
| | (Word Mode) | (Byte Mode) | |
| Query - Primary extended table, unique ASCII string, PRI | 40 | 80 | 0050 |
| | 41 | 82 | 0052 |
| | 42 | 84 | 0049 |
| Major version number, ASCII | 43 | 86 | 0031 |
| Minor version number, ASCII | 44 | 88 | 0033 |
| Unlock recognizes address (0= recognize, 1= don't recognize) | 45 | 8A | 0000 |
| Erase suspend (2= to both read and program) | 46 | 8C | 0002 |
| Sector protect (N= # of sectors/group) | 47 | 8E | 0004 |
| Temporary sector unprotect (1=supported) | 48 | 90 | 0001 |
| Sector protect/Chip unprotect scheme | 49 | 92 | 0004 |
| Simultaneous R/W operation (0=not supported) | 4A | 94 | 0000 |
| Burst mode (0=not supported) | 4B | 96 | 0000 |
| Page mode (0=not supported) | 4C | 98 | 0000 |
| Minimum acceleration supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV | 4D | 9A | 0095 |
| Maximum acceleration supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV | 4E | 9C | 00A5 |
| Low/High boot block indicator | 4F | 9E | 0004/ |
| 04h=Low boot device, | | | 0005 |
| 05h=High boot device | | | |

ABSOLUTE MAXIMUM STRESS RATINGS

| | |
|---|----------------------|
| Surrounding Temperature with Bias | -65°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage Range | |
| Vcc | -0.5 V to +4.0 V |
| RESET#, A9, ACC and OE# | -0.5 V to +10.5 V |
| The other pins. | -0.5 V to Vcc +0.5 V |
| Output Short Circuit Current (less than one second) | .200 mA |

Note:

1. Minimum voltage may undershoot to -2V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to Vcc+2V during transition and for less than 20ns during transitions.

OPERATING TEMPERATURE AND VOLTAGE

Commercial (C) Grade

Surrounding Temperature (T_A) 0° C to +70° C

Industrial (I) Grade

Surrounding Temperature (T_A) -40° C to +85° C

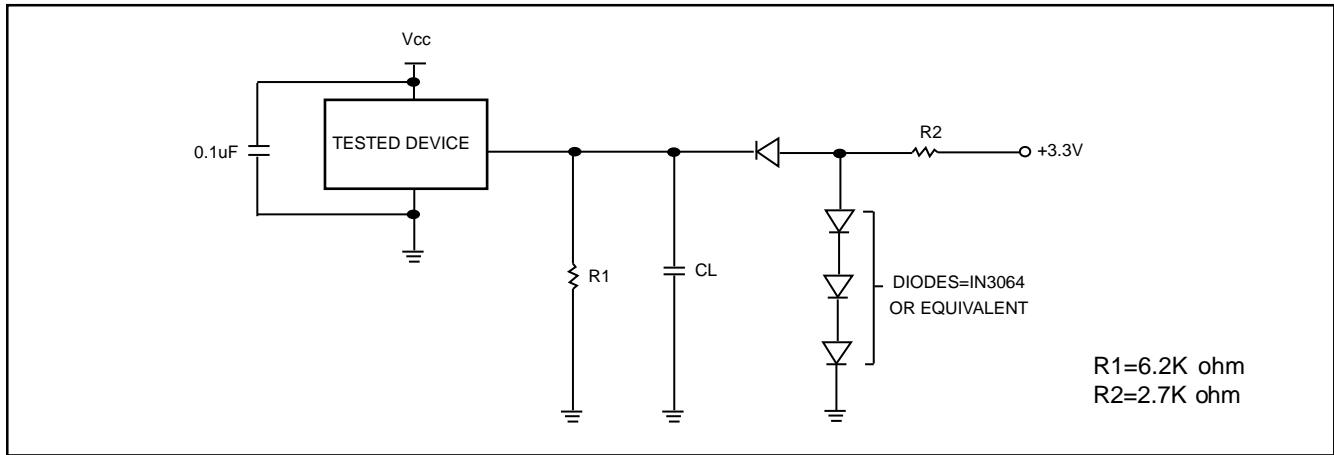
Vcc Supply Voltages

Vcc range +2.7 V to 3.6 V

DC CHARACTERISTICS

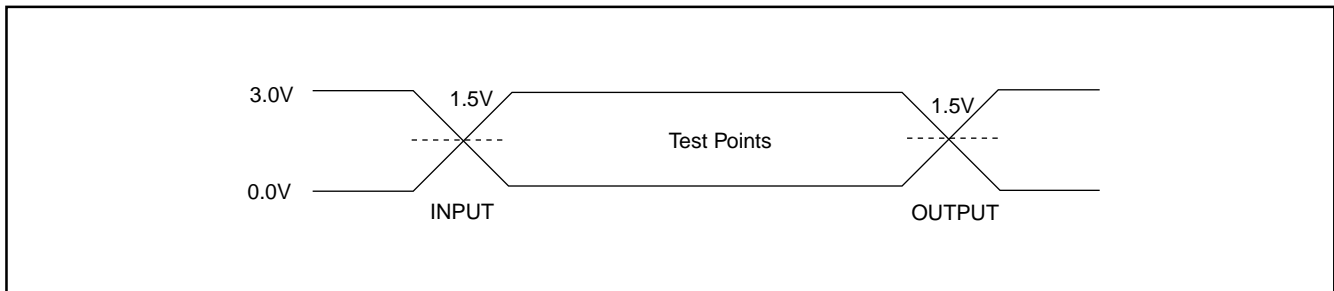
| Symbol | Description | Min | Typ | Max | Remark |
|-------------------|---|-----------------------|------|-----------------------|--|
| Iilk | Input Leak | | | ± 1.0uA | |
| Iilk9 | A9 Leak | | | 35uA | A9=10V |
| Iolk | Output Leak | | | ± 1.0uA | |
| Icr1 | Read Current(5MHz) | | 9mA | 16mA | CE#=Vil, OE#=Vih |
| Icr2 | Read Current(1MHz) | | 2mA | 4mA | CE#=Vil, OE#=Vih |
| Icw | Write Current | | 26mA | 30mA | CE#=Vil, OE#=Vih, WE#=Vil |
| I _{sb} | Standby Current | | 5uA | 15uA | V _{cc} =V _{cc max} , other pin disable |
| I _{sr} | Reset Current | | 5uA | 15uA | V _{cc} =V _{ccmax} , Reset# enable, other pin disable |
| I _{sb} s | Sleep Mode Current | | 5uA | 15uA | |
| Icp1 | Accelerated Pgm Current, WP#/Acc pin(Word/Byte) | | 5mA | 10mA | CE#=Vil, OE#=Vih, |
| Icp2 | Accelerated Pgm Current, Vcc pin,(Word/Byte) | | 15mA | 30mA | CE#=Vil, OE#=Vih, |
| Vil | Input Low Voltage | -0.5V | | 0.8V | |
| Vih | Input High Voltage | 0.7xV _{cc} | | V _{cc} +0.3V | |
| V _{hv} | Very High Voltage for hardware Protect/Unprotect/Auto Select/ Temporary Unprotect/ Accelerated Program | 9.5V | | 10.5V | |
| V _{ol} | Output Low Voltage | | | 0.45V | I _{ol} =4.0mA |
| V _{oh1} | Output High Voltage | 0.85xV _{cc} | | | I _{oh1} =-2mA |
| V _{oh2} | Output High Voltage | V _{cc} -0.4V | | | I _{oh2} =-100uA |
| Vlko | Low Vcc Lock-out Voltage | 2.3V | | 2.5V | |

SWITCHING TEST CIRCUITS



Test Condition
Output Load : 1 TTL gate
Output Load Capacitance, CL : 30pF
Rise/Fall Times : 5ns
In/Out reference levels : 1.5V
Input Pulse level : 0.0 ~ 3.0V

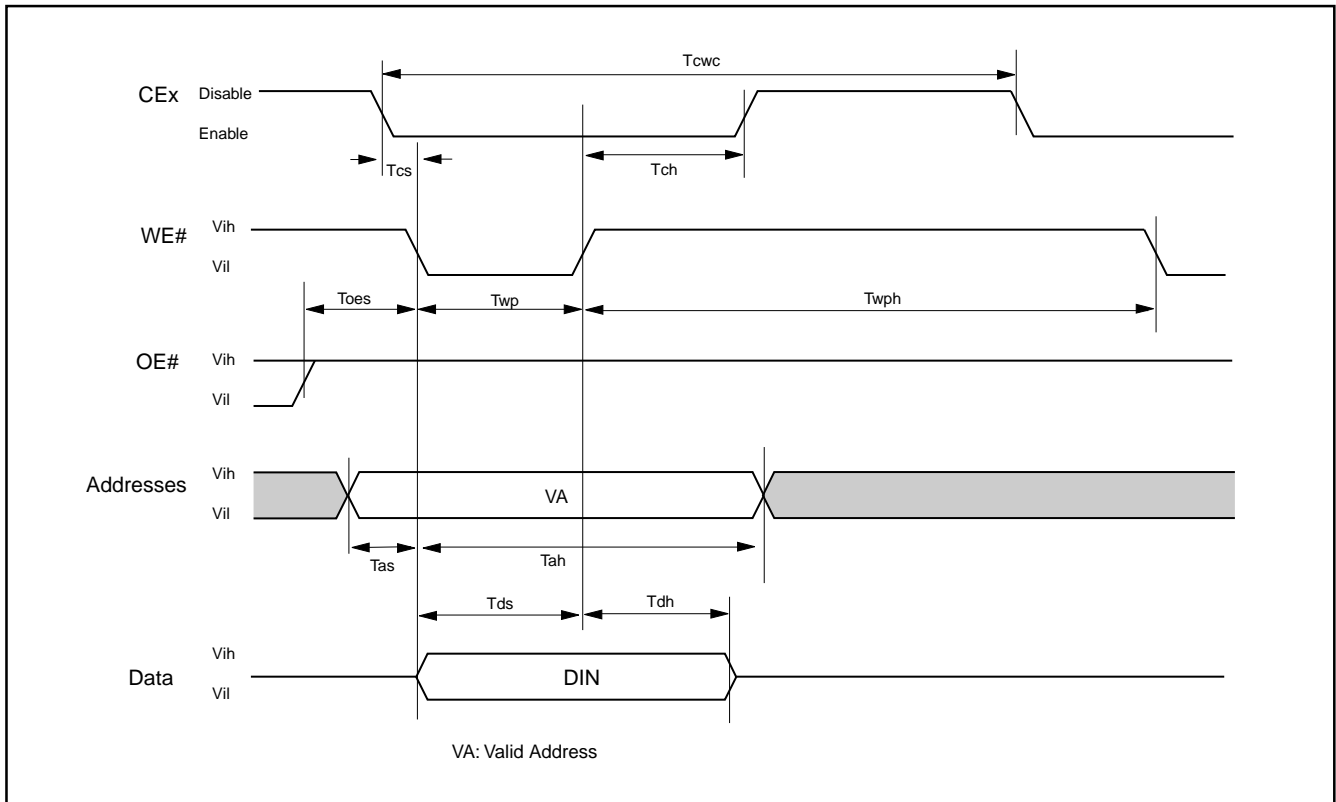
SWITCHING TEST WAVEFORMS



AC CHARACTERISTICS

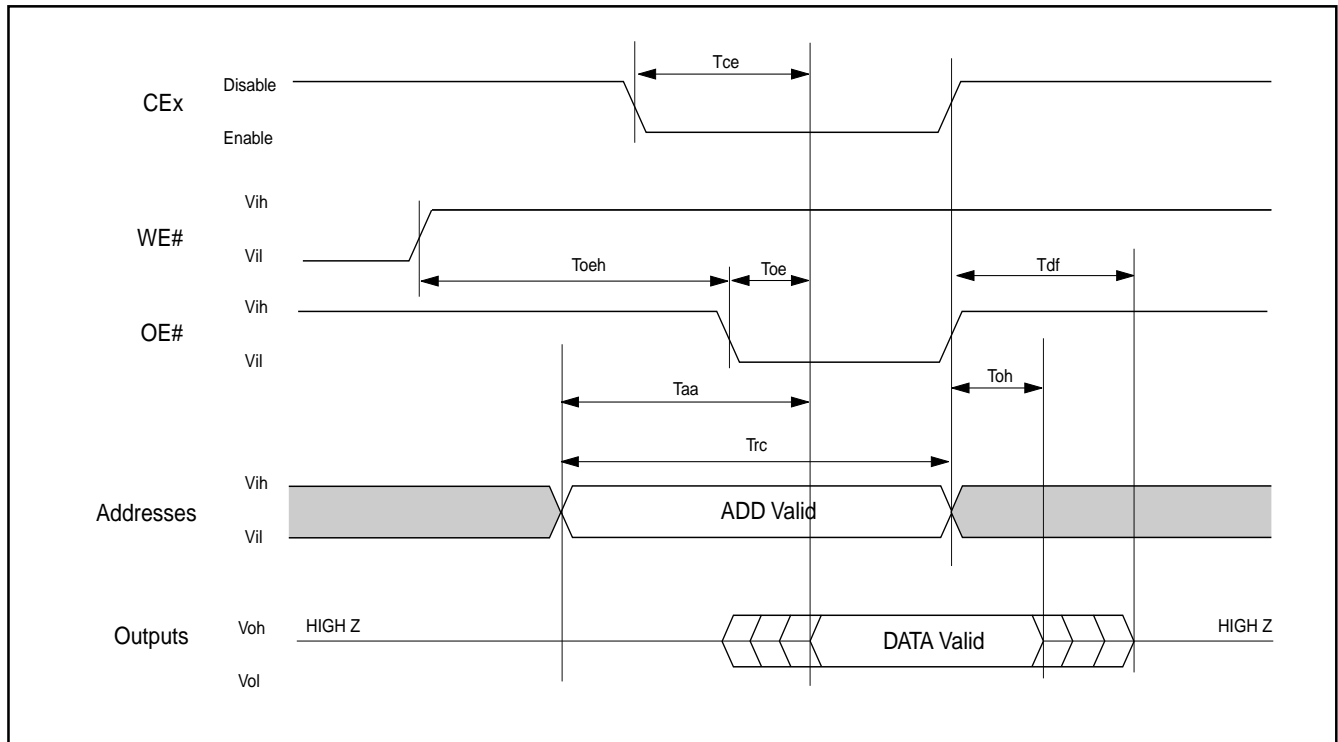
| Symbol | Description | Min | Typ | Max | Unit |
|--------|---|------------------------|-----|-----|------|
| Taa | Valid data output after address | | | 90 | ns |
| Tce | Valid data output after CEx low | | | 90 | ns |
| Toe | Valid data output after OE# low | | | 30 | ns |
| Tdf | Data output floating after OE# high | | | 30 | ns |
| Toh | Output hold time from the earliest rising edge of address, CEx, OE# | 0 | | | ns |
| Trc | Read period time | 90 | | | ns |
| Twc | Write period time | 90 | | | ns |
| Tcwc | Command write period time | 90 | | | ns |
| Tas | Address setup time | 0 | | | ns |
| Tah | Address hold time | 45 | | | ns |
| Tds | Data setup time | 45 | | | ns |
| Tdh | Data hold time | 0 | | | ns |
| Tvcs | Vcc setup time | 100 | | | us |
| Tcs | Chip enable Setup time | 0 | | | ns |
| Tch | Chip enable hold time | 0 | | | ns |
| Toes | Output enable setup time | 0 | | | ns |
| Toeh | Output enable hold time | Read | 0 | | ns |
| Toeh | | Toggle & Data# Polling | 10 | | ns |
| Tws | WE# setup time | 0 | | | ns |
| Twh | WE# hold time | 0 | | | ns |
| Tcep | CEx pulse width | 45 | | | ns |
| Tceph | CEx pulse width high | 30 | | | ns |
| Twp | WE# pulse width | 35 | | | ns |
| Twph | WE# pulse width high | 30 | | | ns |
| Tbusy | Program/Erase active time by RY/BY# | | | 90 | ns |
| Tghwl | Read recover time before write | 0 | | | ns |
| Tghel | Read recover time before write | 0 | | | ns |
| Twhwh1 | Program operation | | 11 | | us |
| Twhwh1 | Acc Program operation(Word/Byte) | | 7 | | us |
| Twhwh2 | Sector Erase Operation | | 0.7 | | sec |
| Tbal | Sector Add hold time | | | 50 | us |

Figure 1. COMMAND WRITE OPERATION



READ/RESET OPERATION

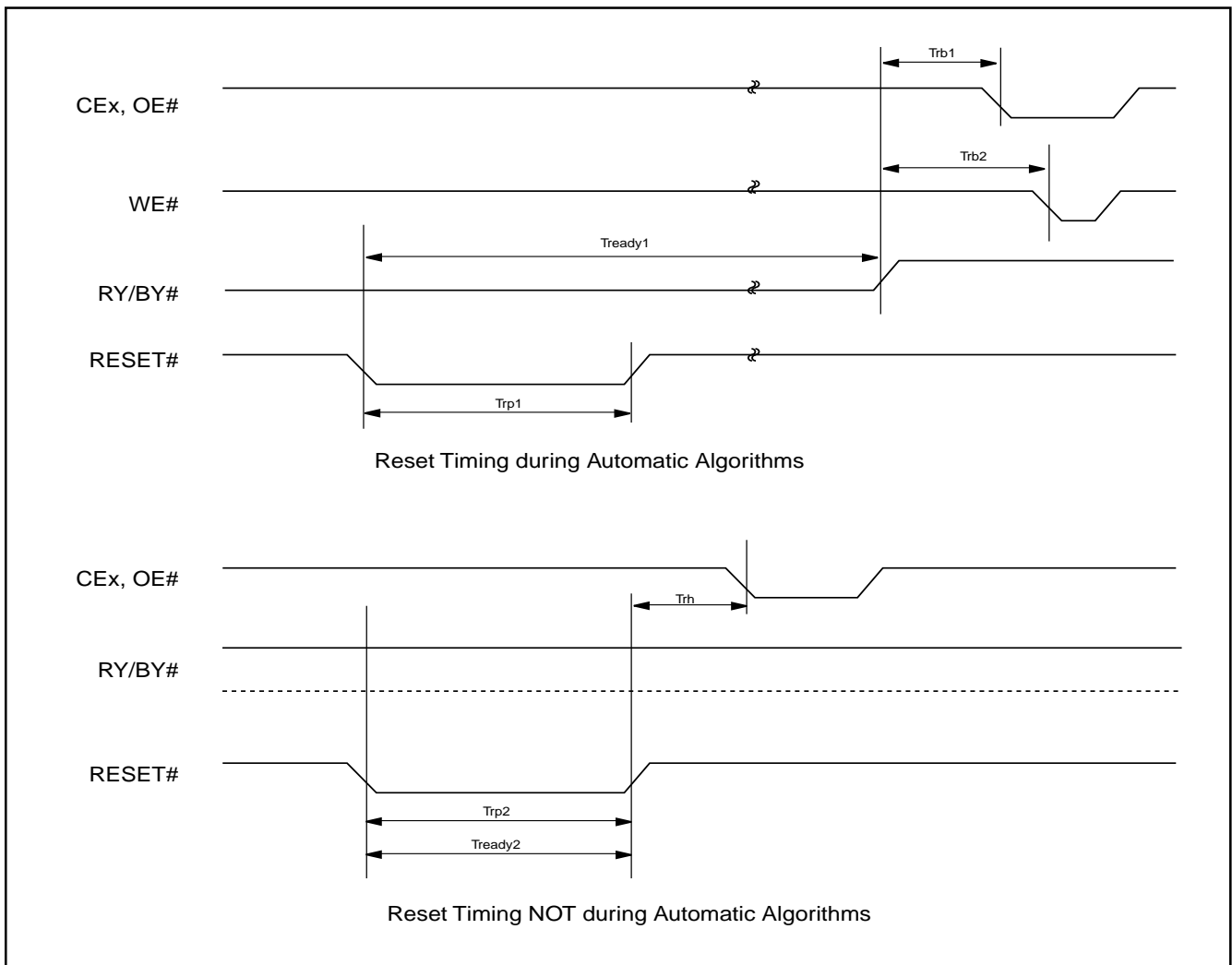
Figure 2. READ TIMING WAVEFORMS



AC CHARACTERISTICS

| Item | Description | Setup | Speed | Unit |
|---------|---|-------|-------|------|
| Trp1 | RESET# Pulse Width (During Automatic Algorithms) | MIN | 10 | us |
| Trp2 | RESET# Pulse Width (NOT During Automatic Algorithms) | MIN | 500 | ns |
| Trh | RESET# High Time Before Read | MIN | 50 | ns |
| Trb1 | RY/BY# Recovery Time (to CE#, OE# go low) | MIN | 0 | ns |
| Trb2 | RY/BY# Recovery Time (to WE# go low) | MIN | 50 | ns |
| Tready1 | RESET# PIN Low (During Automatic Algorithms) to Read or Write | MAX | 20 | us |
| Tready2 | RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write | MAX | 500 | ns |

Figure 3. RESET# TIMING WAVEFORM



ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

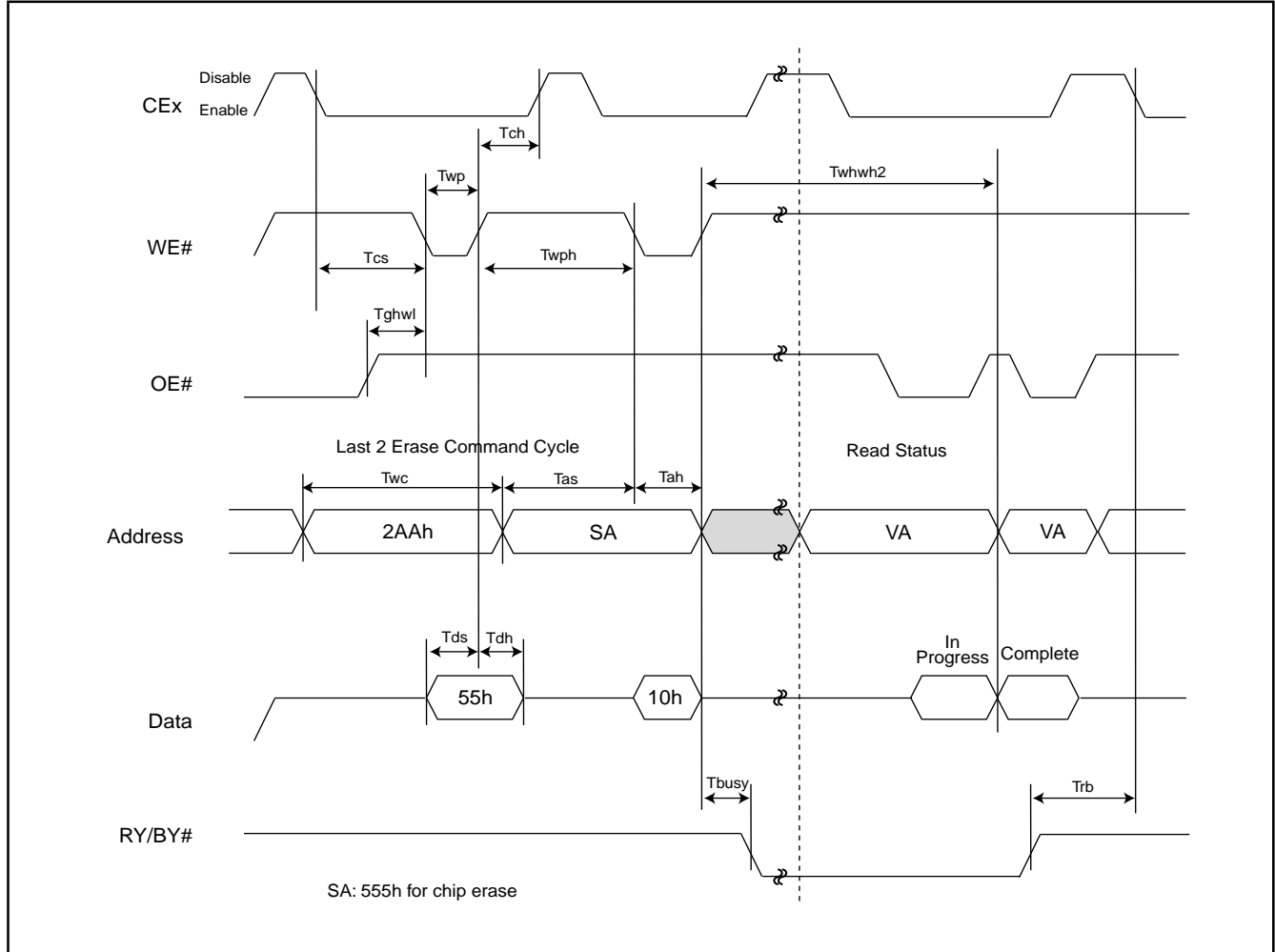


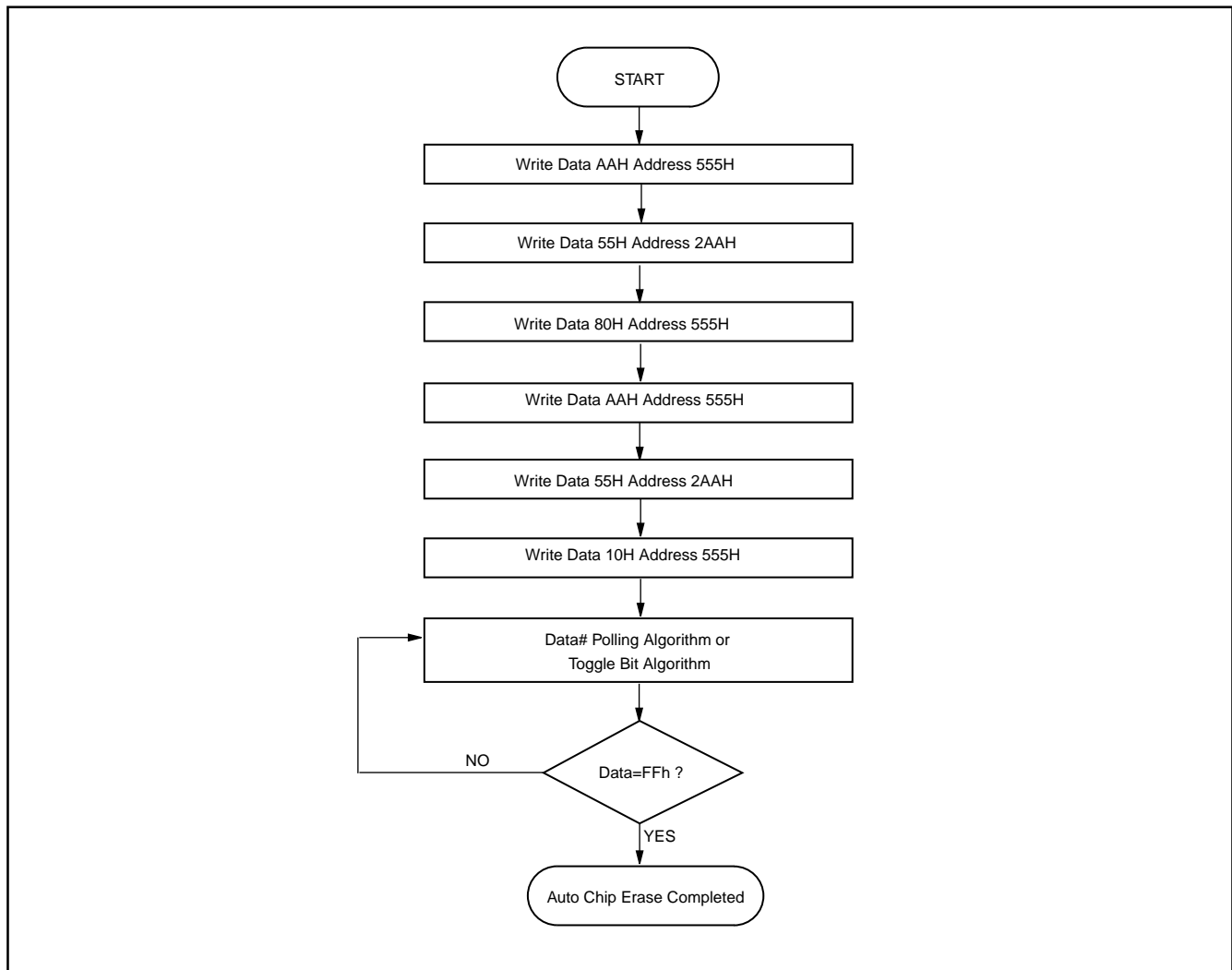
Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

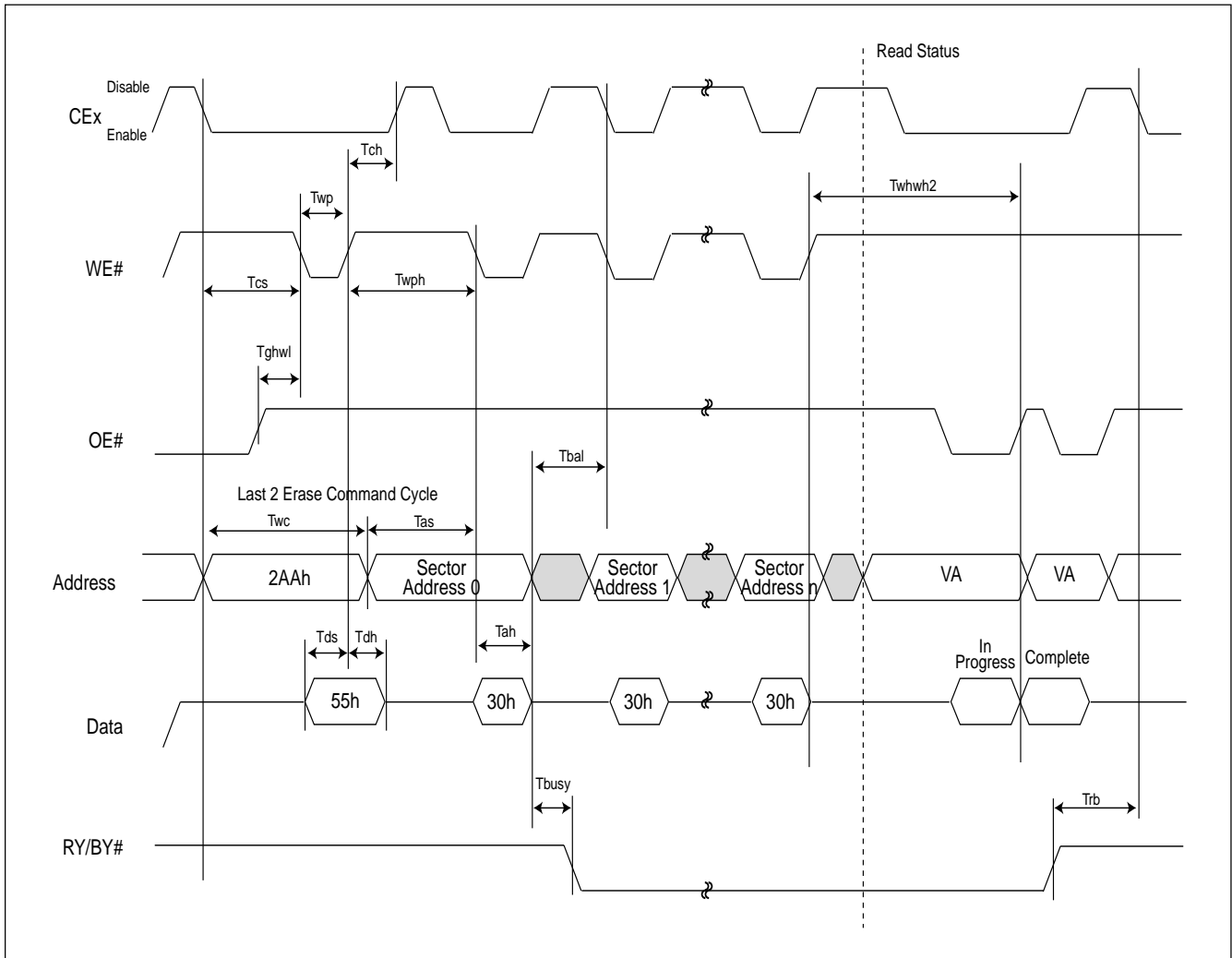


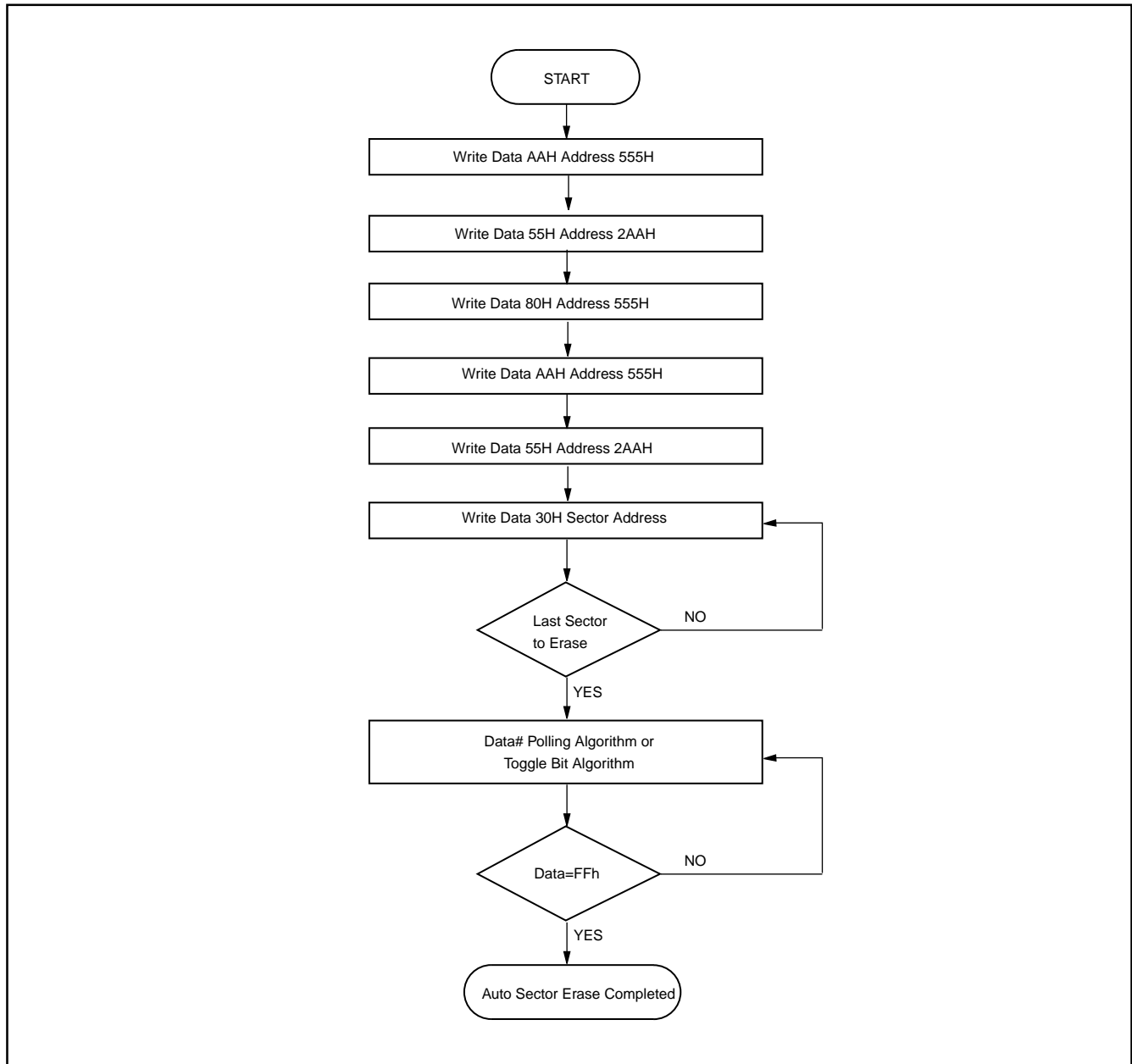
Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

Figure 8. ERASE SUSPEND/RESUME FLOWCHART

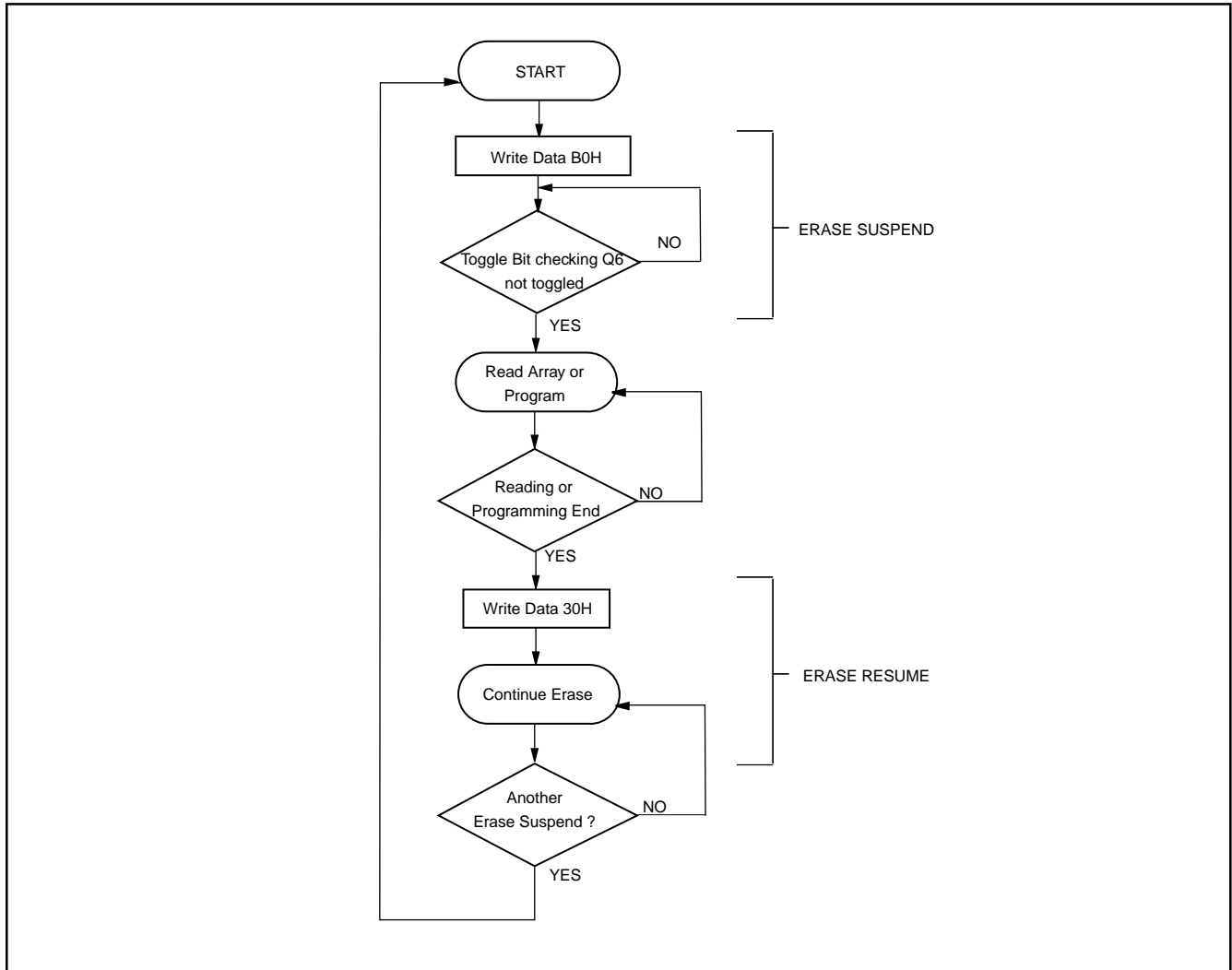


Figure 9. SECURED SILICON SECTOR PROTECTED ALGORITHMS FLOWCHART

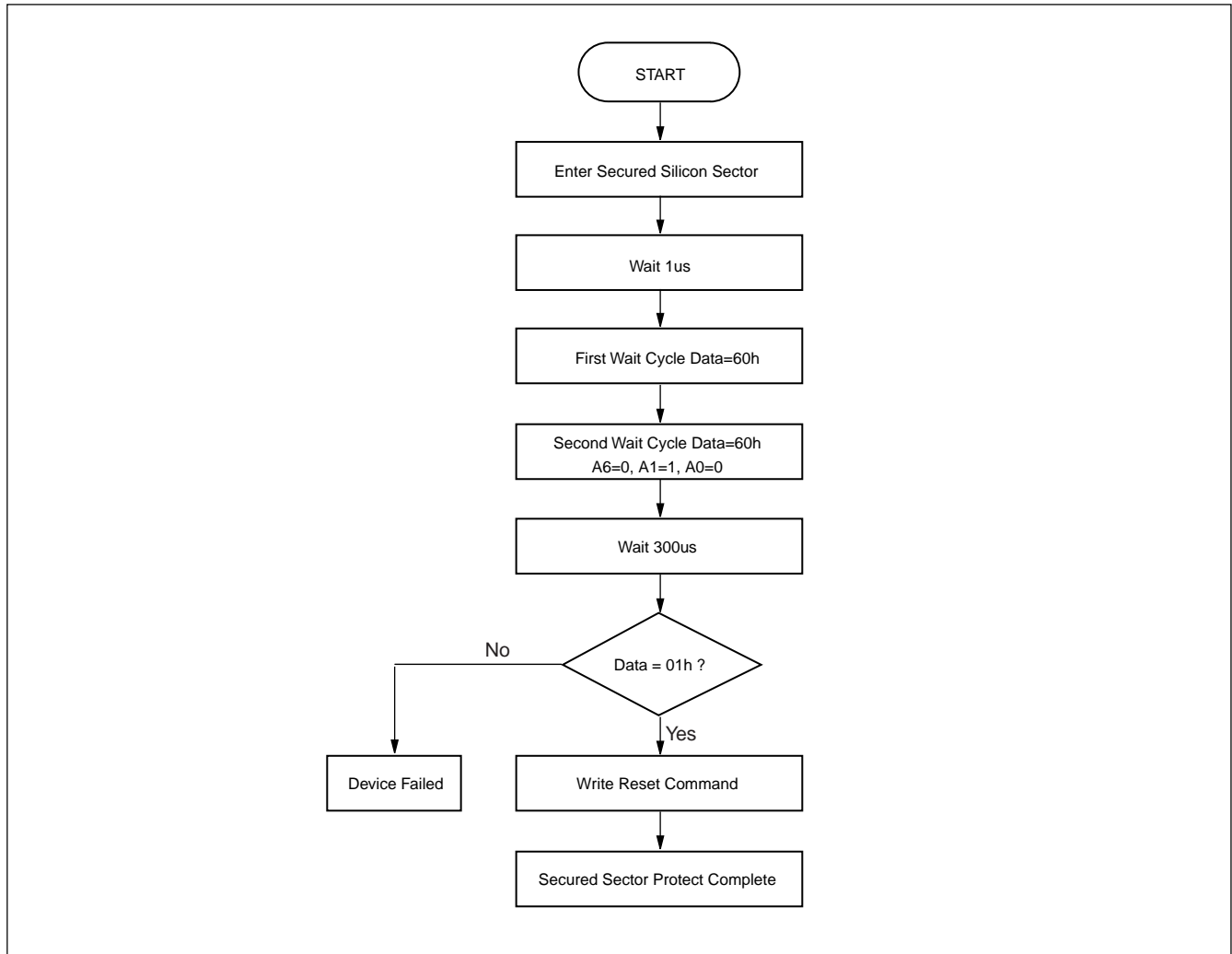


Figure 10. AUTOMATIC PROGRAM TIMING WAVEFORMS

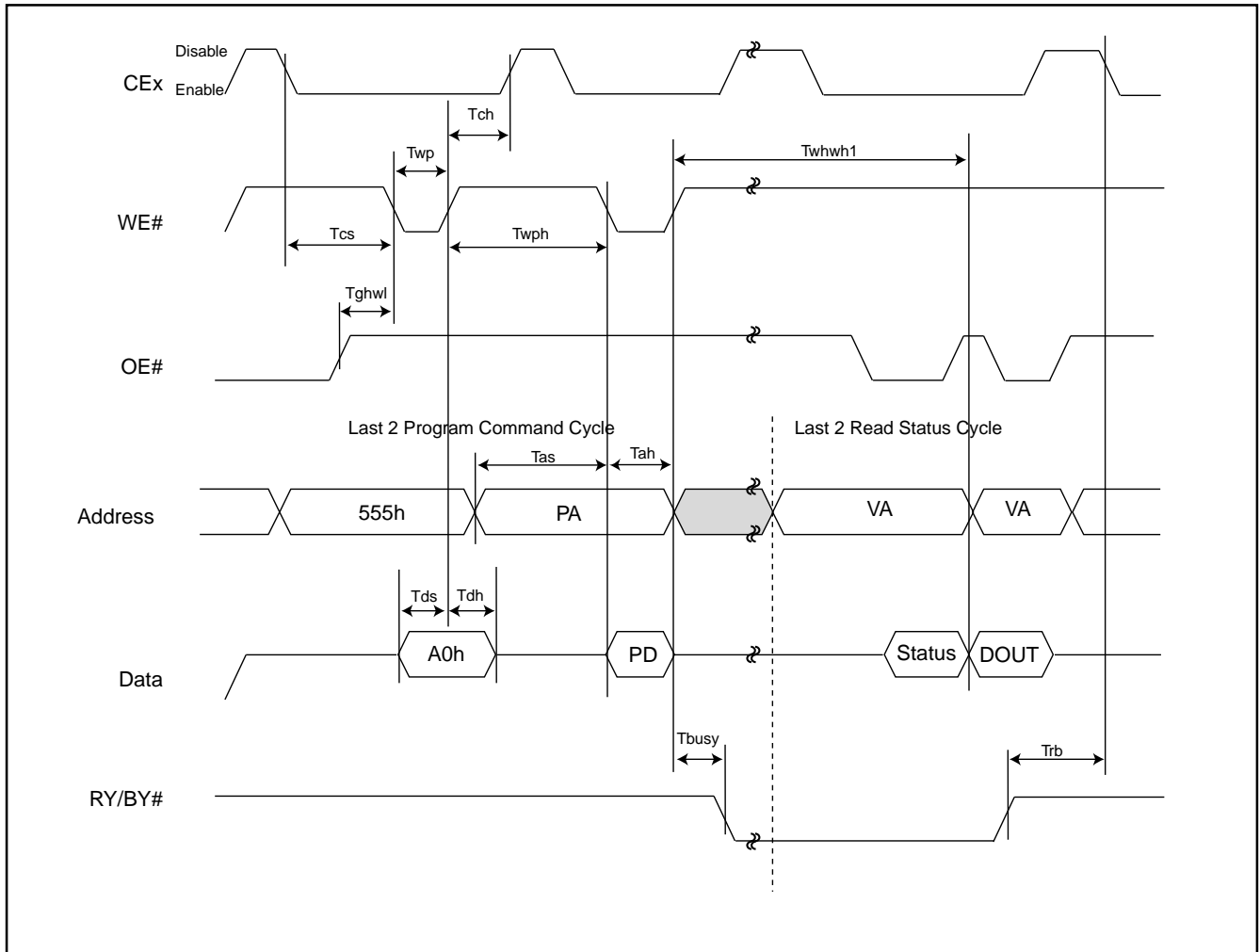


Figure 11. Accelerated Program Timing Diagram

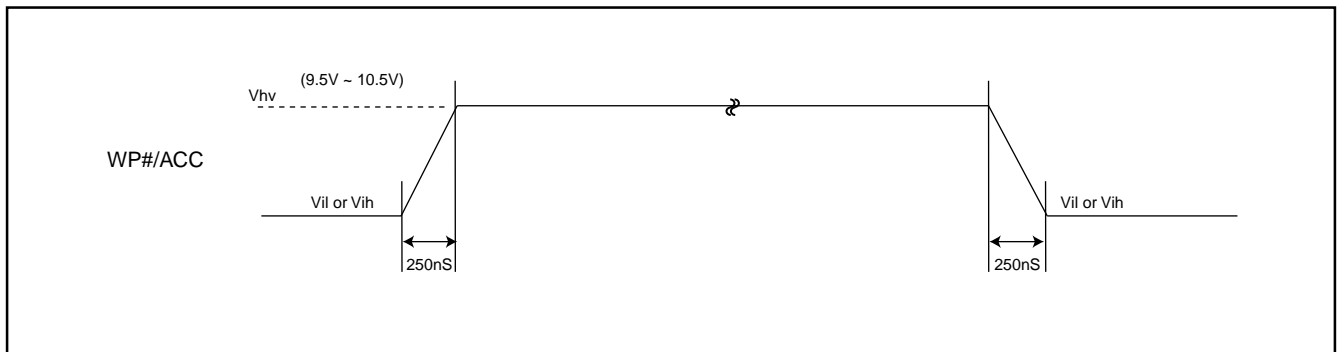


Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

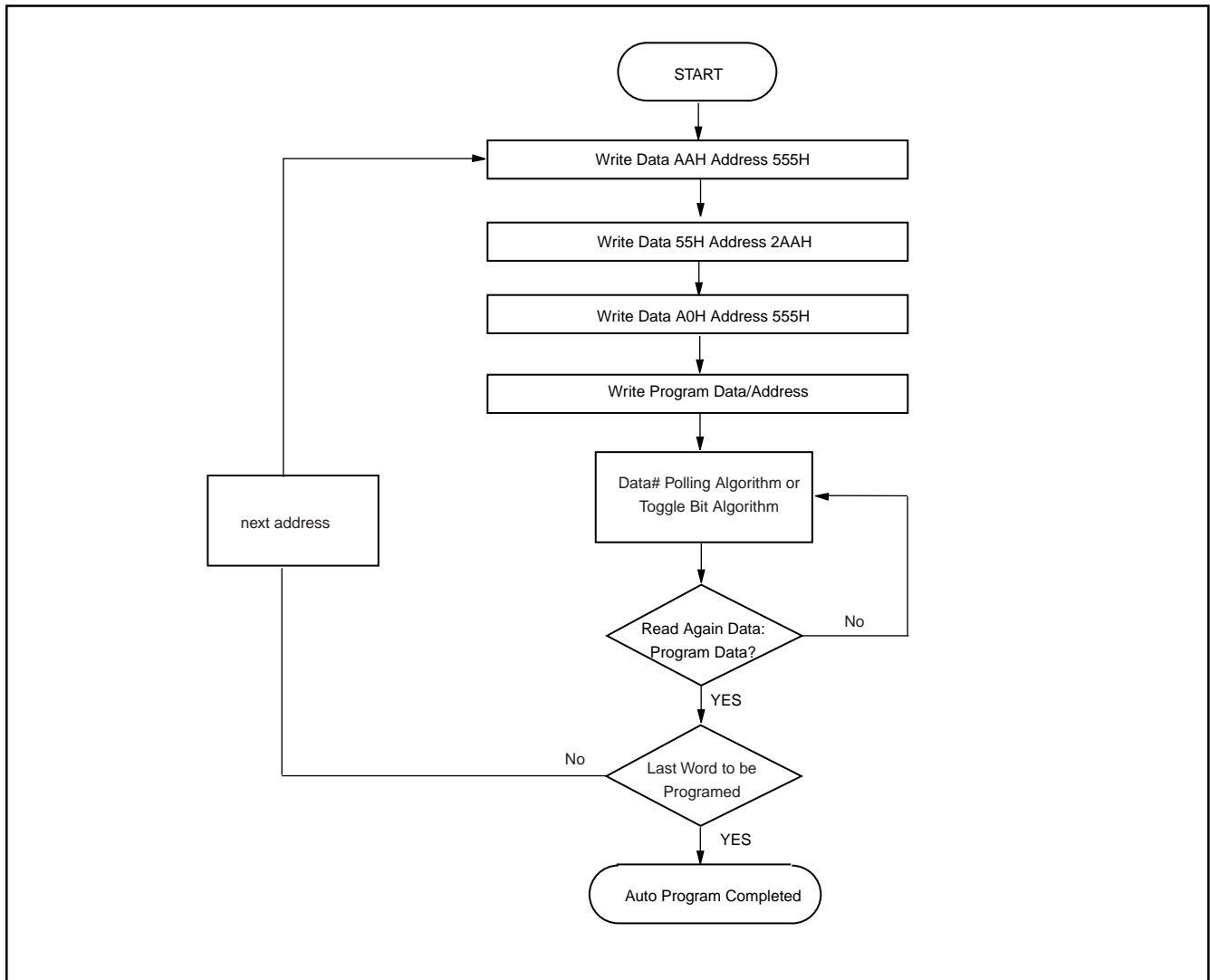
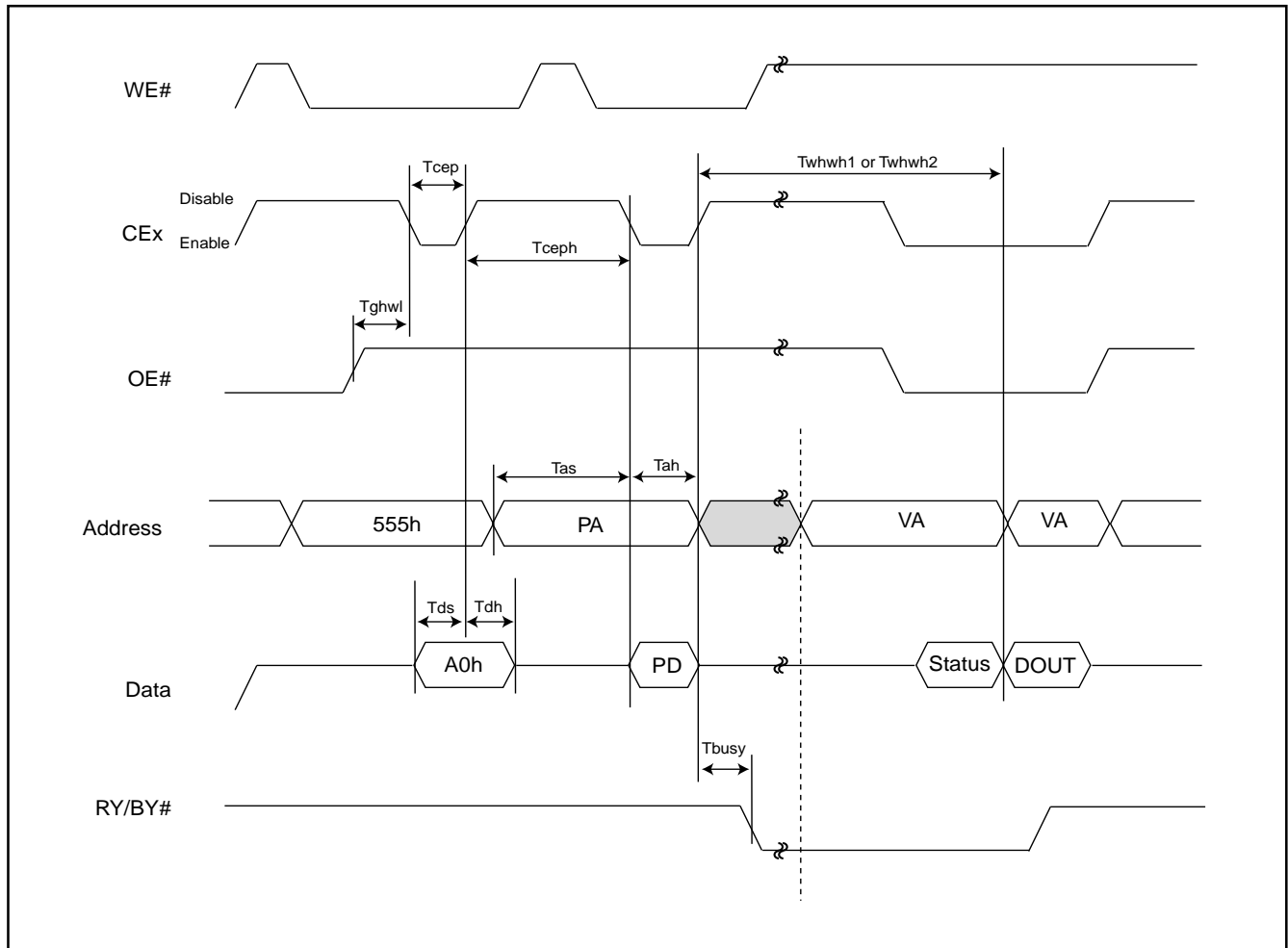


Figure 13. CEx CONTROLLED WRITE TIMING WAVEFORM



SECTOR PROTECT/CHIP UNPROTECT

Figure 14. SECTOR PROTECT/CHIP UNPROTECT WAVEFORM (RESET# Control)

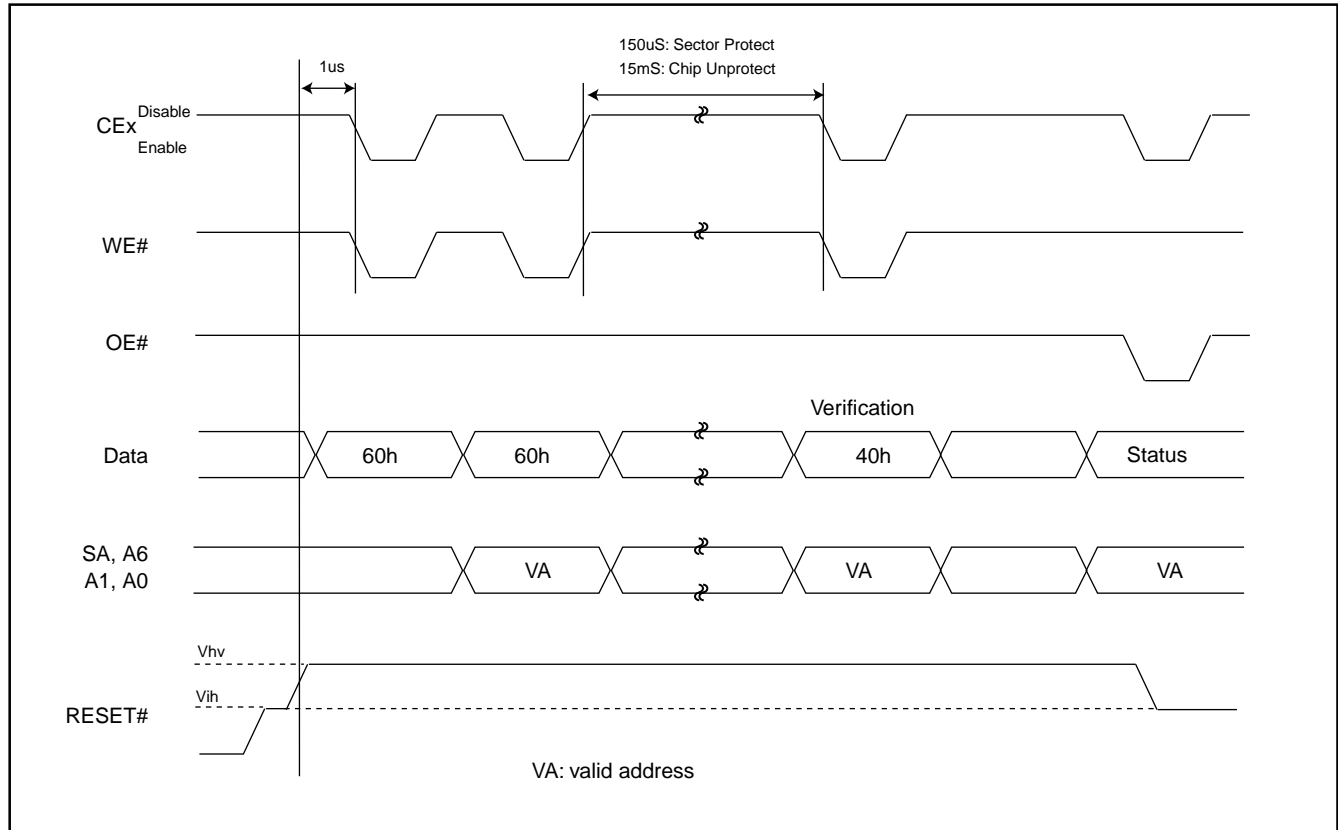


Figure 15-1. IN-SYSTEM SECTOR PROTECT WITH RESET# = Vhv

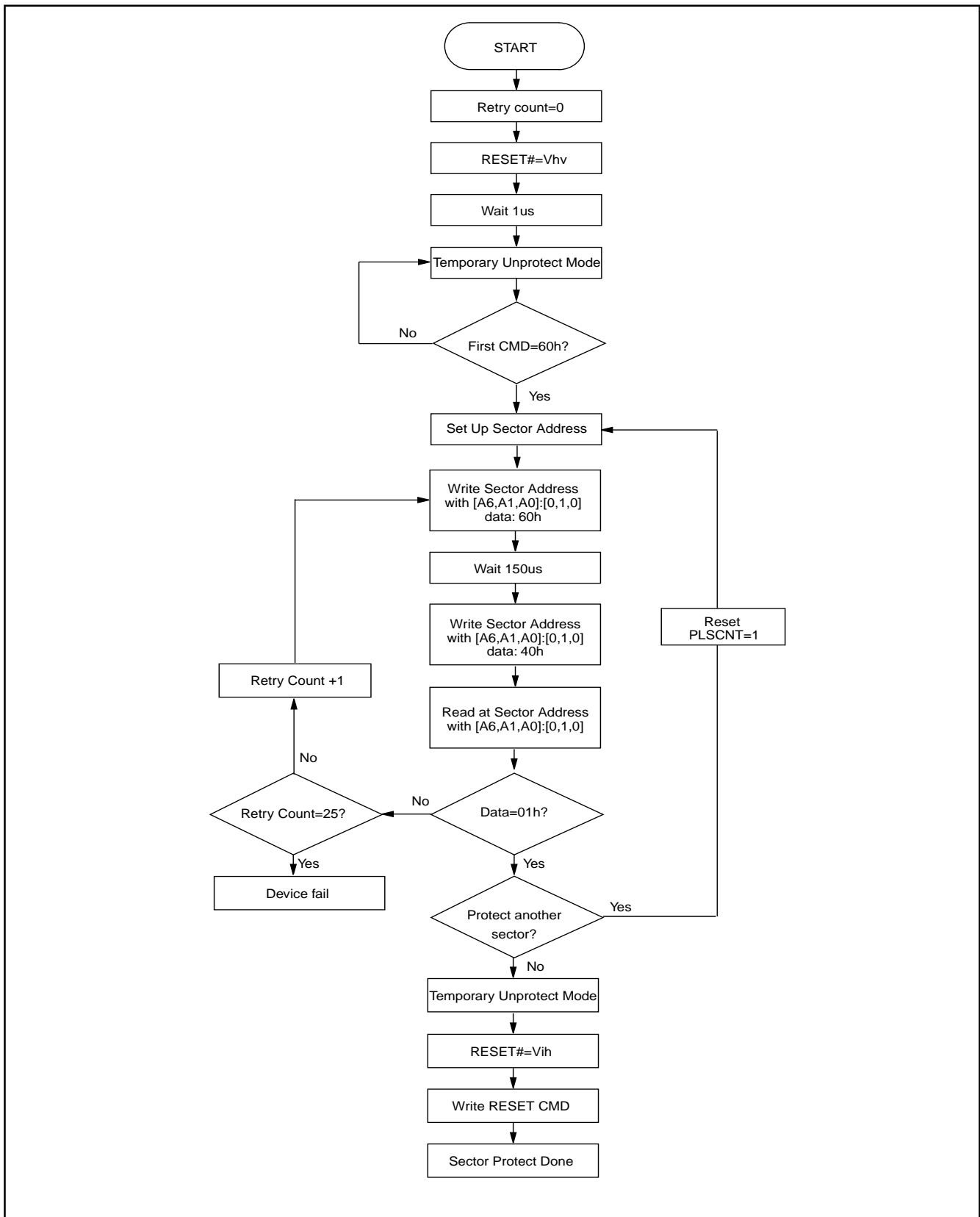
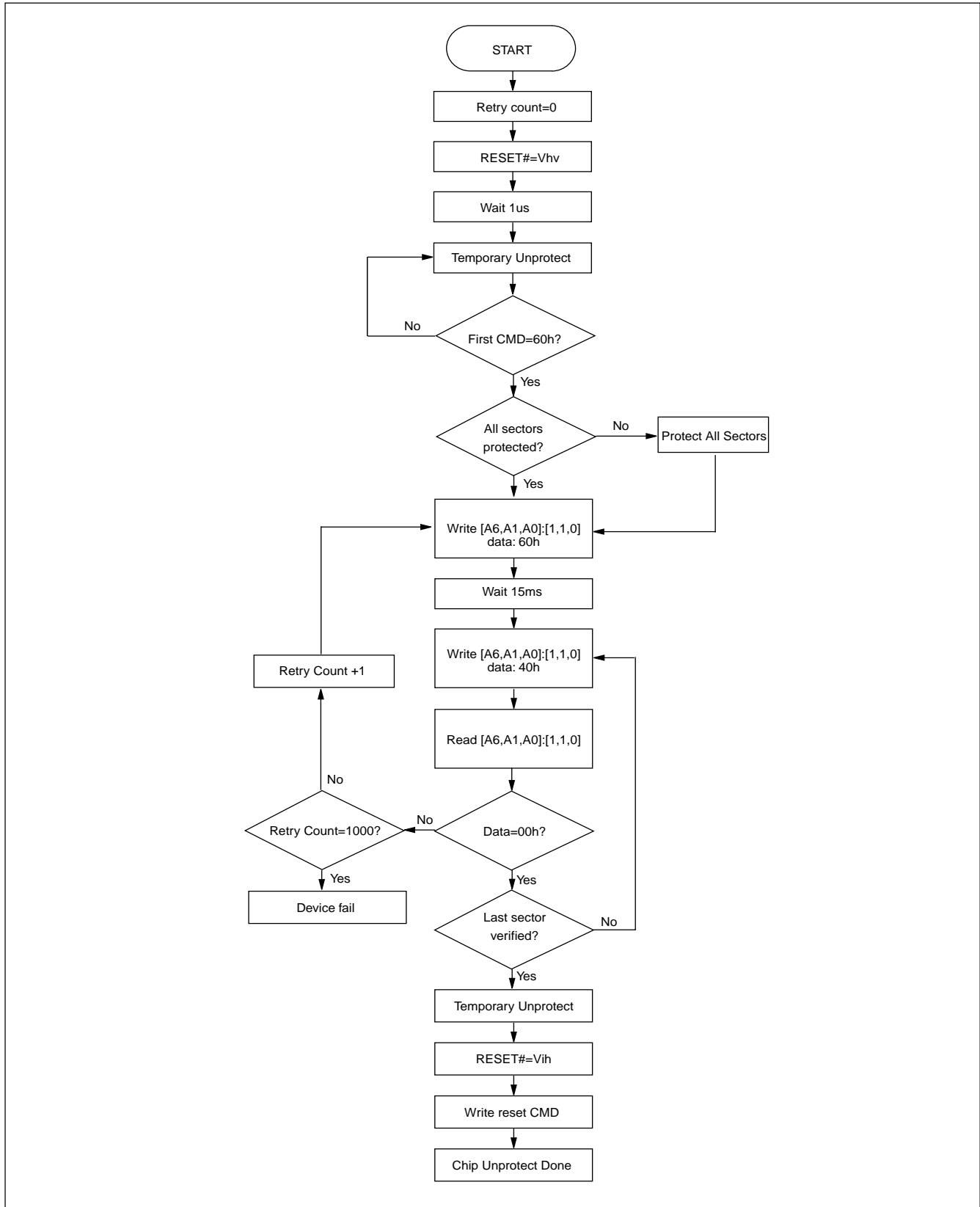


Figure 15-2. CHIP UNPROTECT ALGORITHMS WITH RESET# = Vhv



AC CHARACTERISTICS

| Parameter | Description | Test Setup | All Speed Options | Unit |
|-----------|--------------------------------------|------------|-------------------|------|
| Tvlt | Voltage transition time | Min. | 4 | us |
| Twpp1 | Write pulse width for sector protect | Min. | 100 | ns |
| Twpp2 | Write pulse width for chip unprotect | Min. | 100 | ns |
| Toesp | OE# setup time to WE# active | Min. | 4 | us |

Figure 16. SECTOR PROTECT TIMING WAVEFORM (A9, OE# Control)

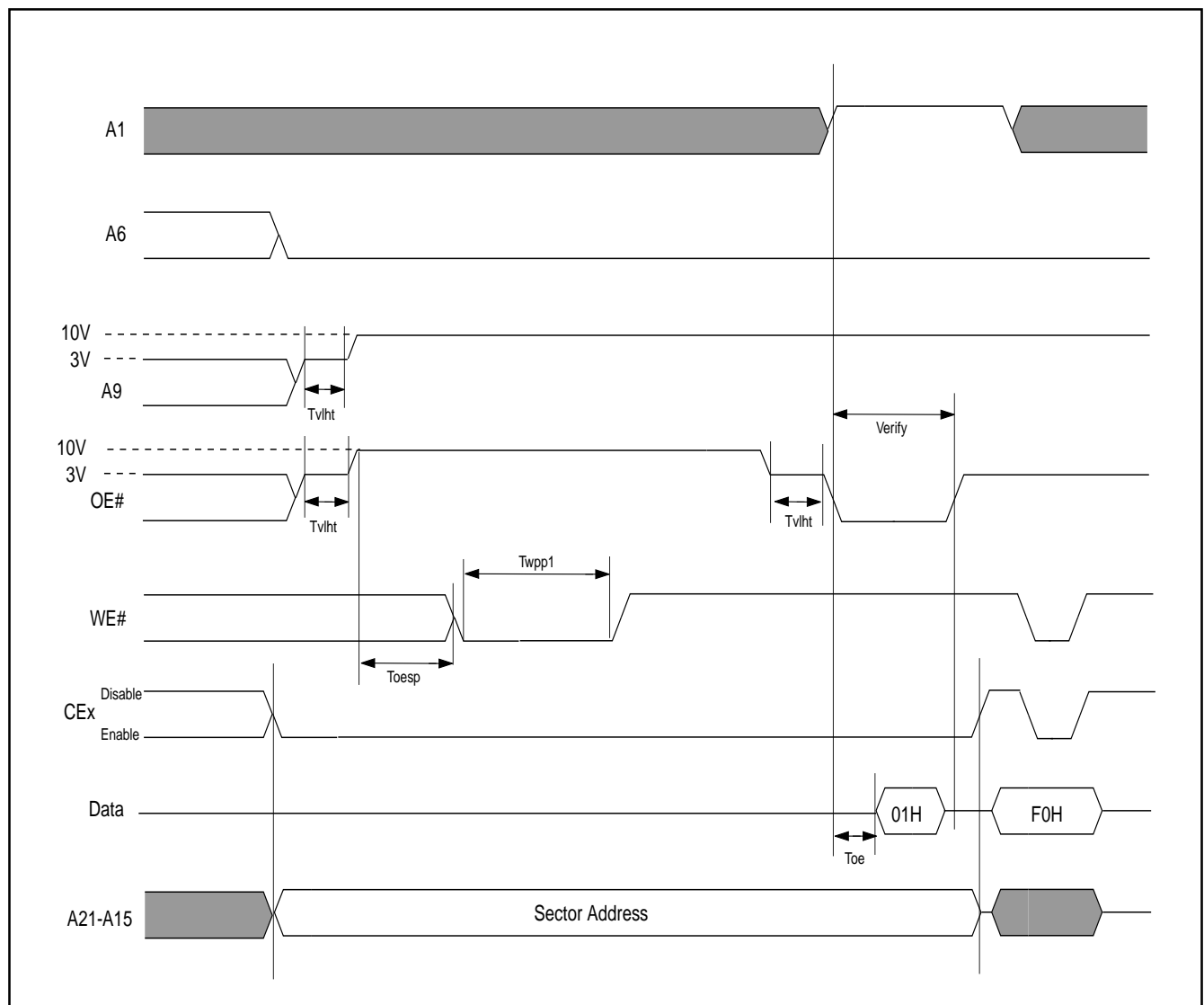


Figure 17. SECTOR PROTECTION ALGORITHM (A9, OE# Control)

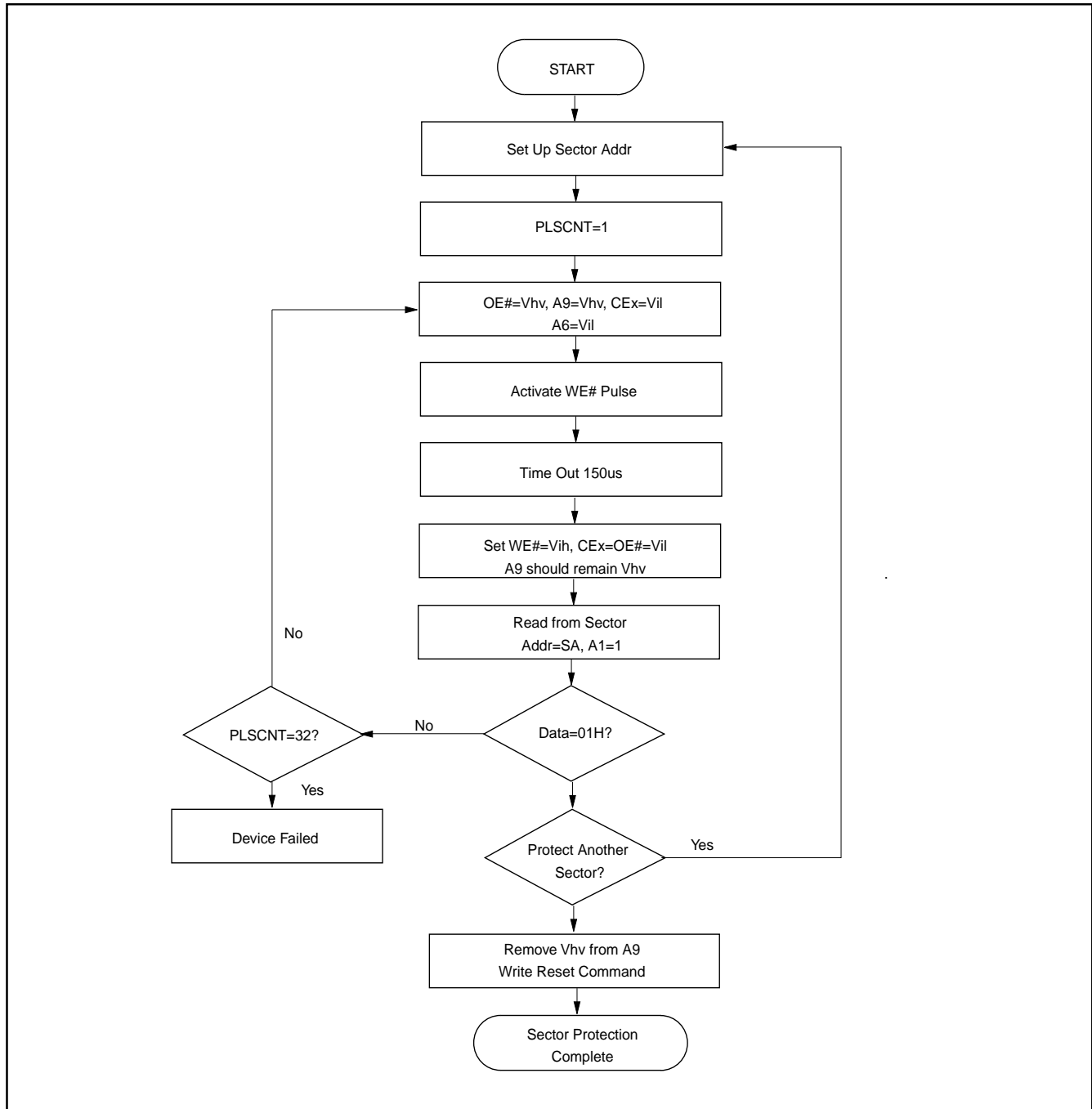


Figure 18. CHIP UNPROTECT TIMING WAVEFORM (A9, OE# Control)

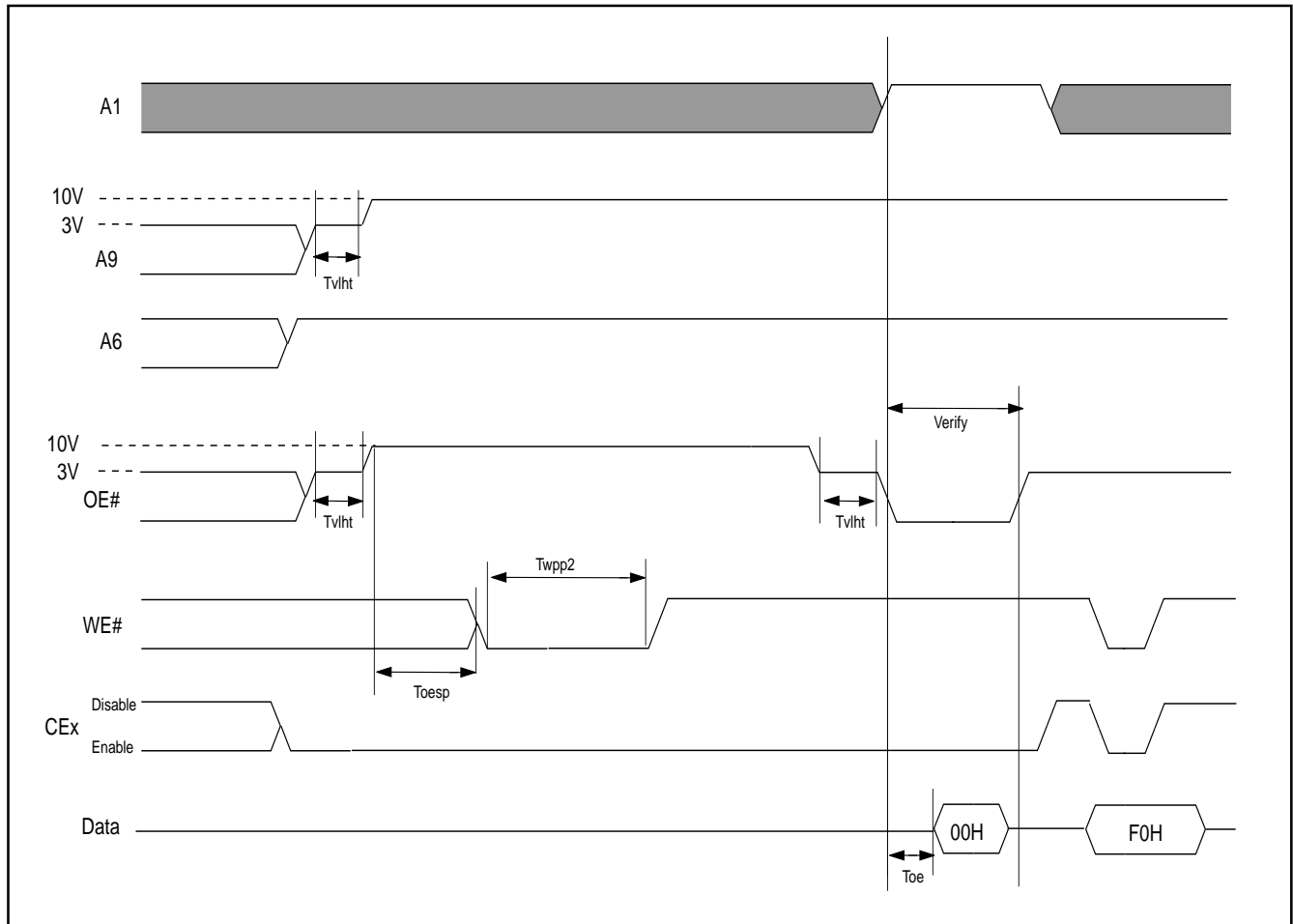
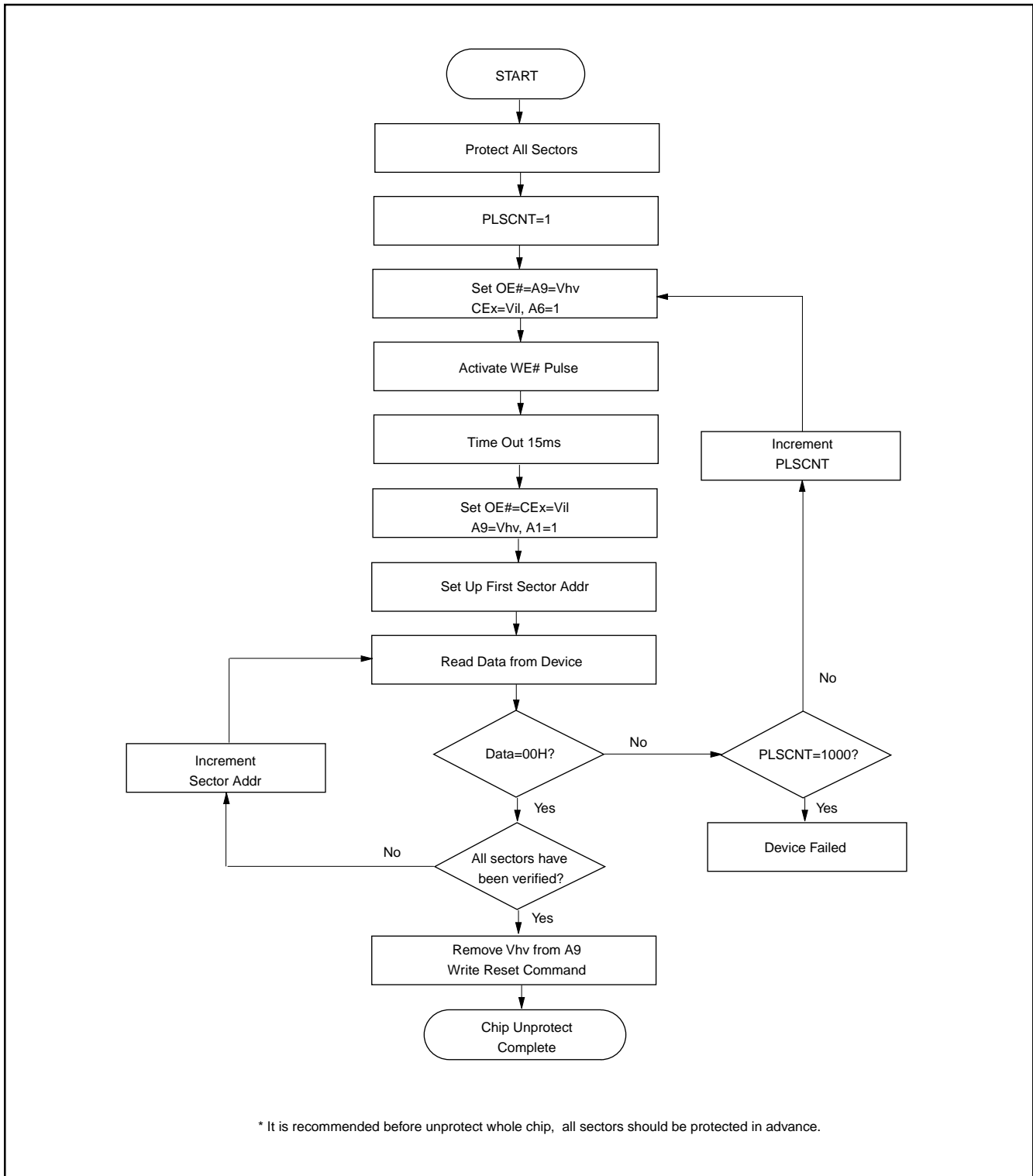


Figure 19. CHIP UNPROTECT FLOWCHART (A9, OE# Control)



AC CHARACTERISTICS

| Parameter | Alt | Description | Condition | Speed | Unit |
|-----------|-------|---|-----------|-------|------|
| Trpvhh | Tvidr | RESET# Rise Time to Vhv and Vhv Fall Time to RESET# | MIN | 500 | ns |
| Tvhhwl | Trsp | RESET# Vhv to WE# Low | MIN | 4 | us |

Figure 20. TEMPORARY SECTOR UNPROTECT WAVEFORMS

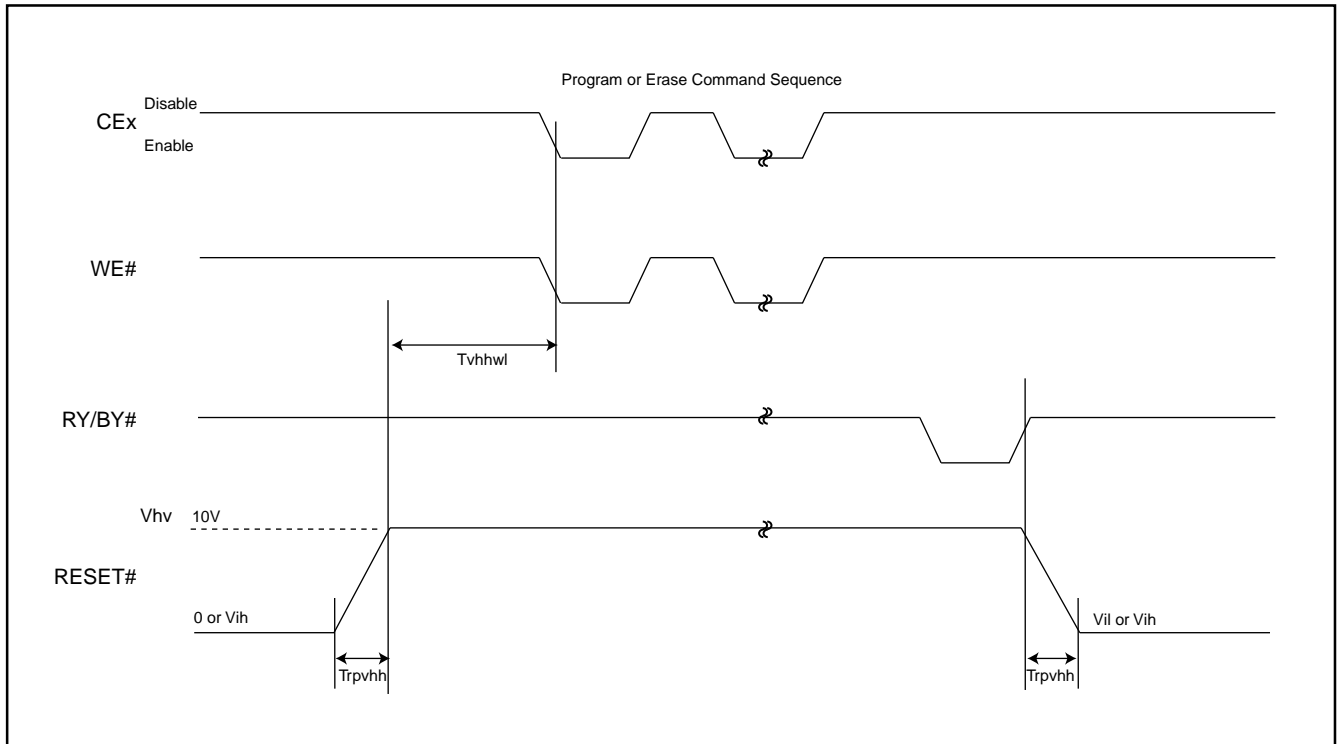
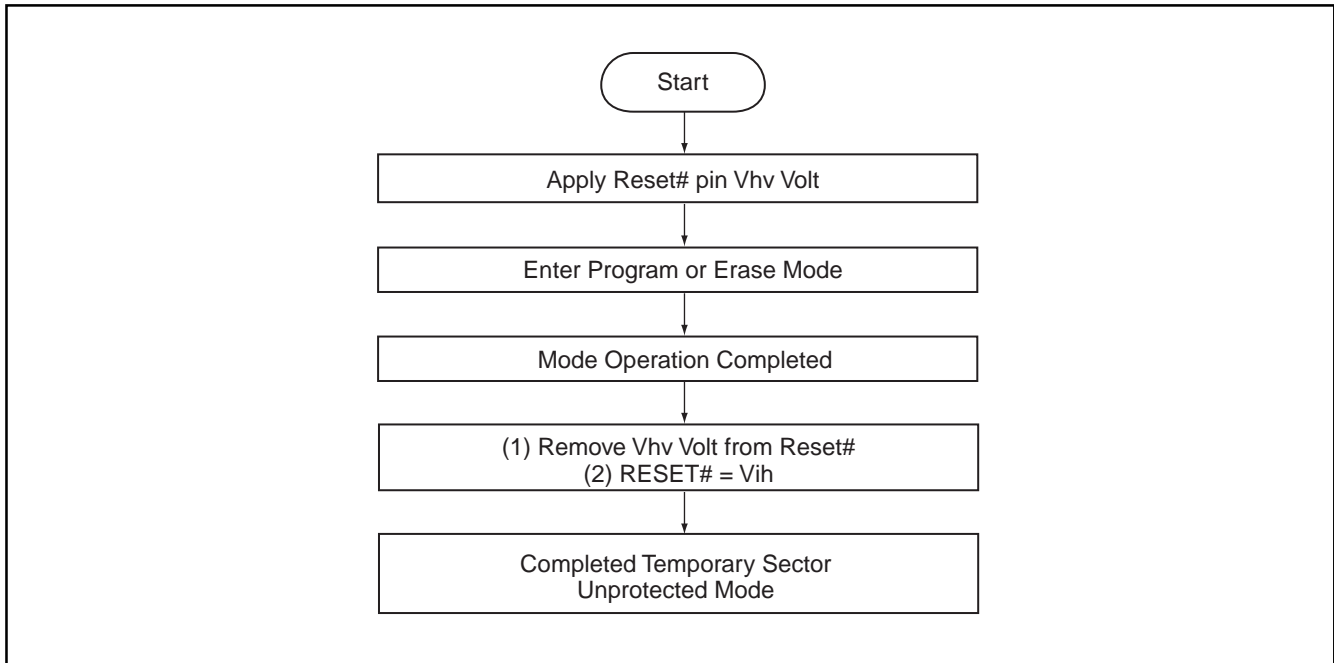
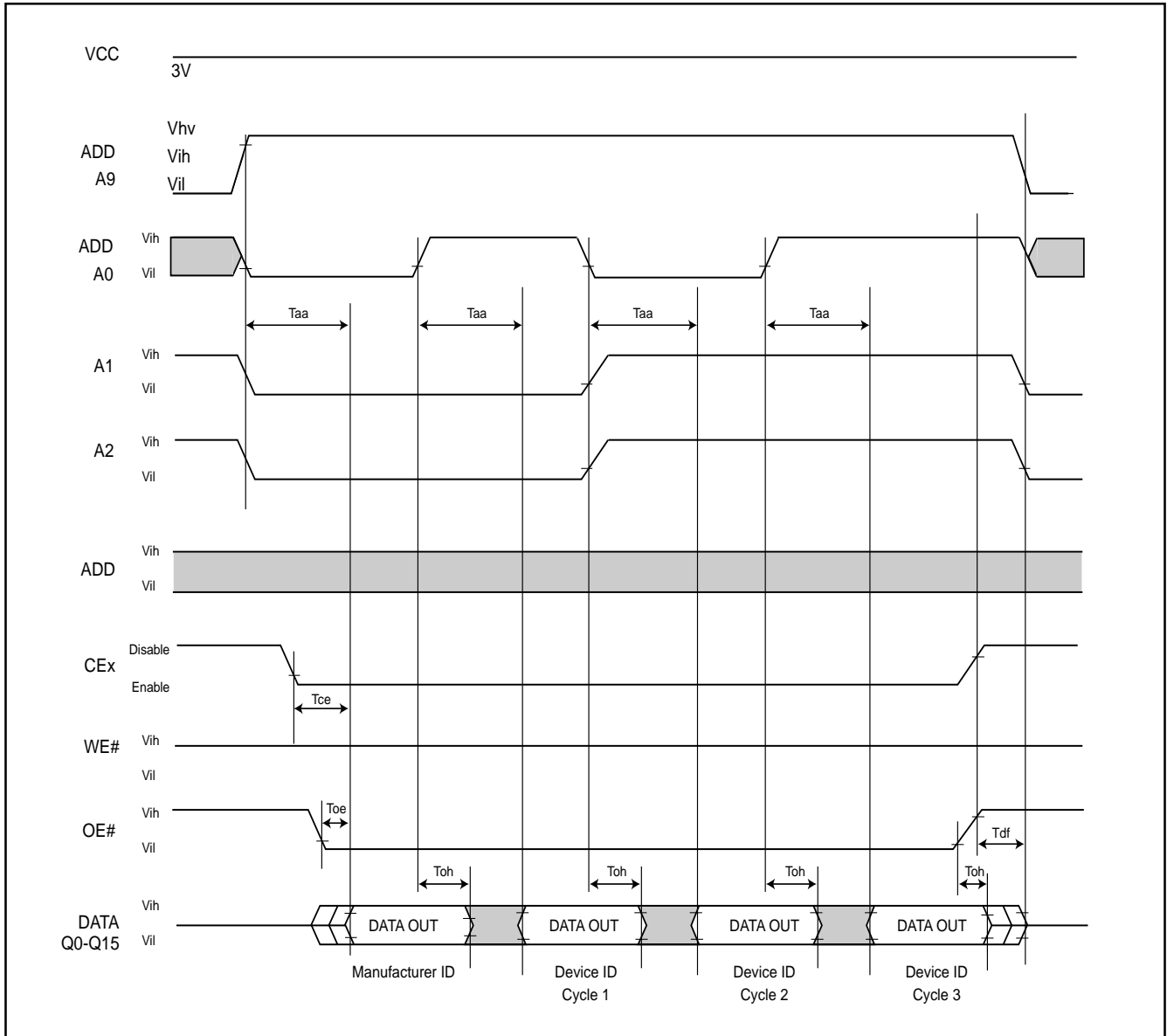


Figure 21. TEMPORARY SECTOR UNPROTECT FLOWCHART**Notes:**

1. Temporary unprotect all protected sectors Vhv=9.5~10.5V.
2. After leaving temporary unprotect mode, the previously protected sectors are again protected.

Figure 22. SILICON ID READTIMING WAVEFORM



WRITE OPERATION STATUS

Figure 23. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

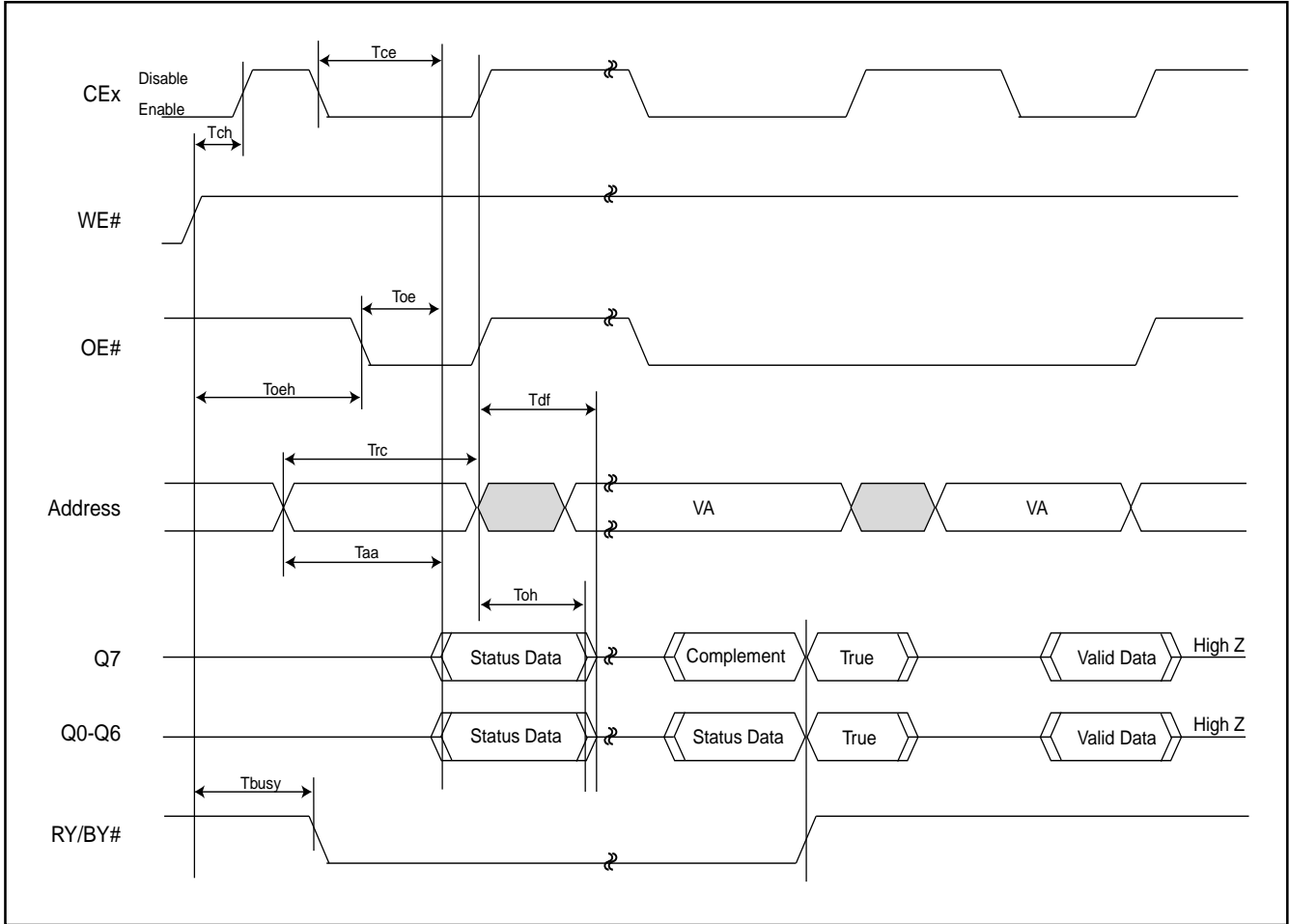
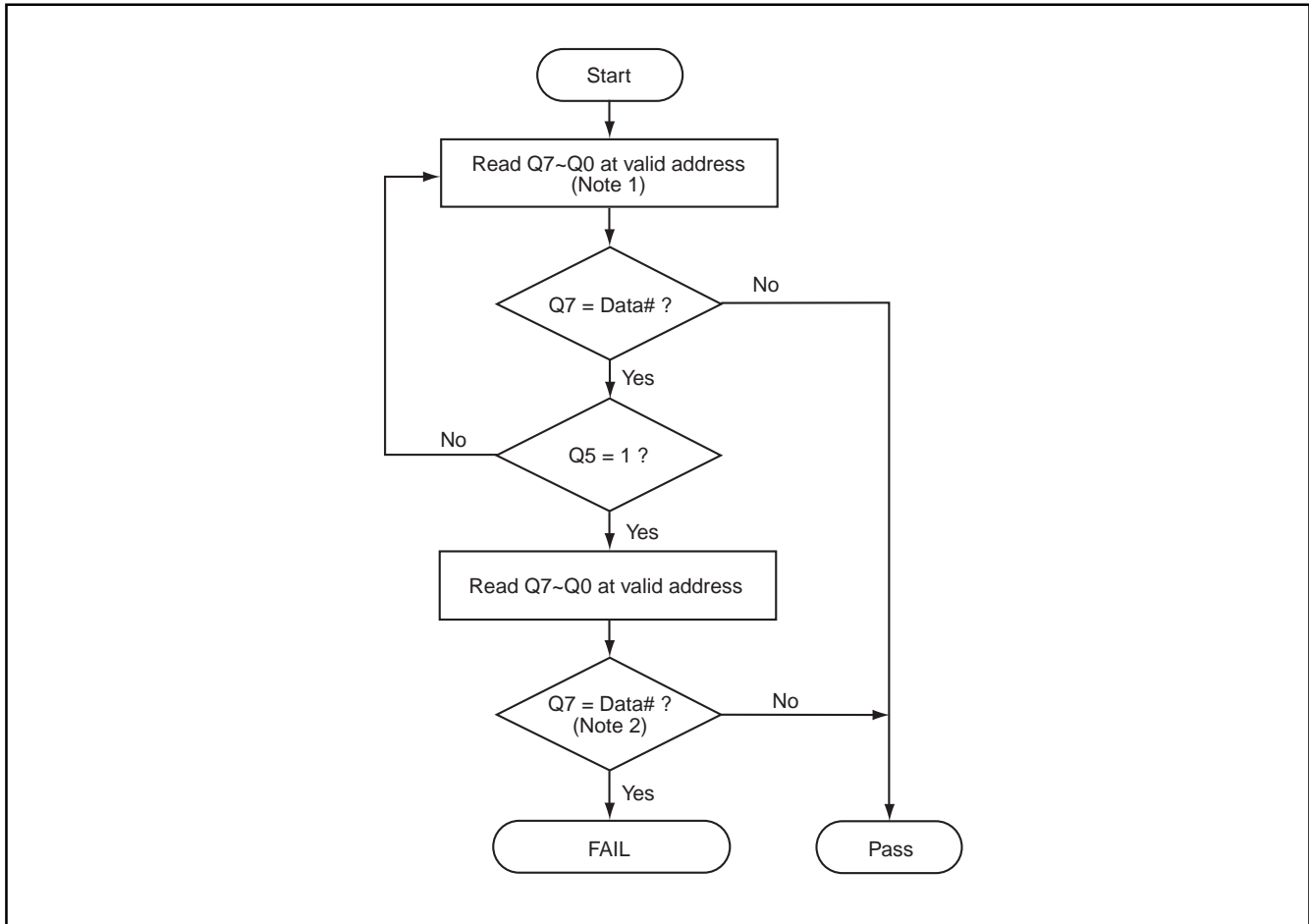


Figure 24. DATA# POLLING ALGORITHM



Notes:

1. For programming, valid address means program address.
For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 25. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

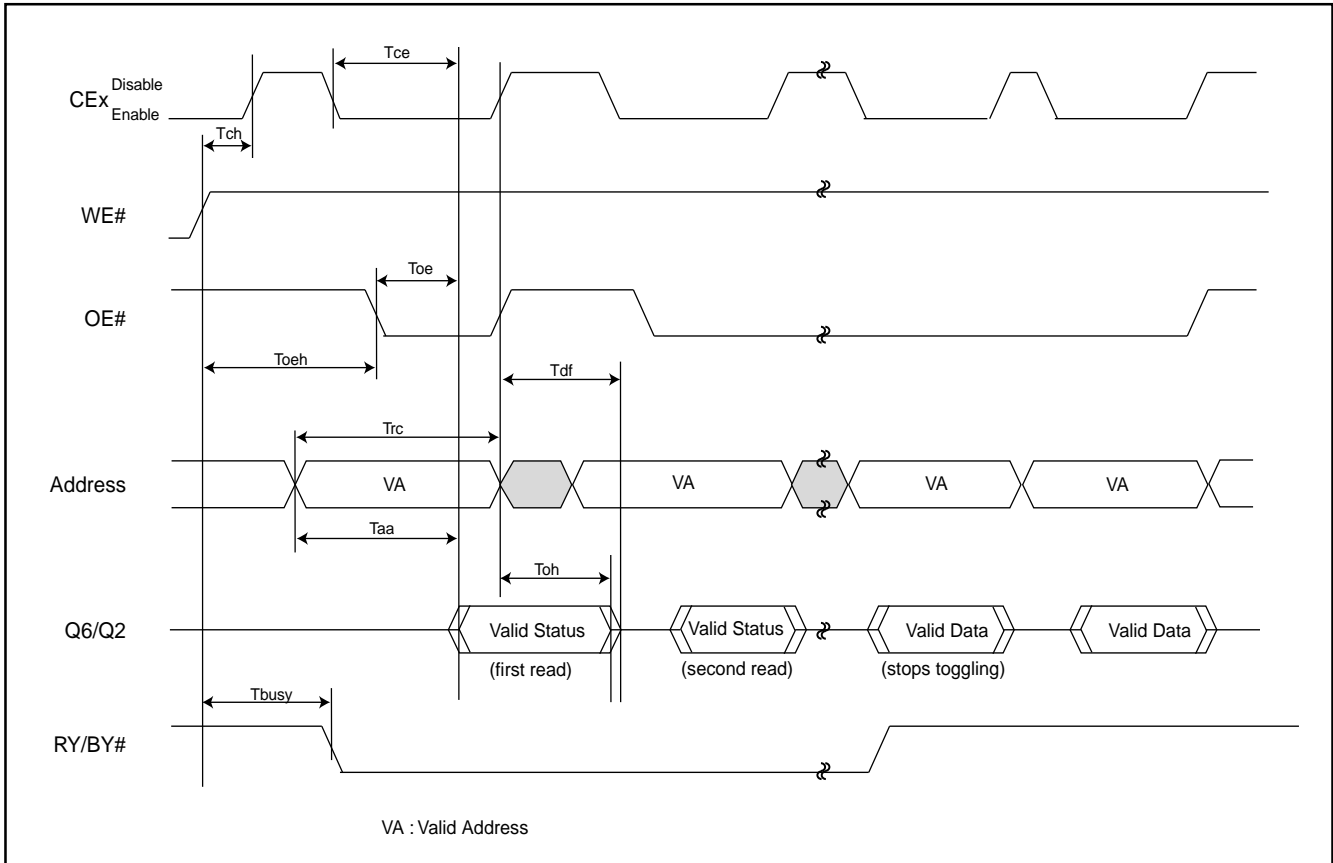
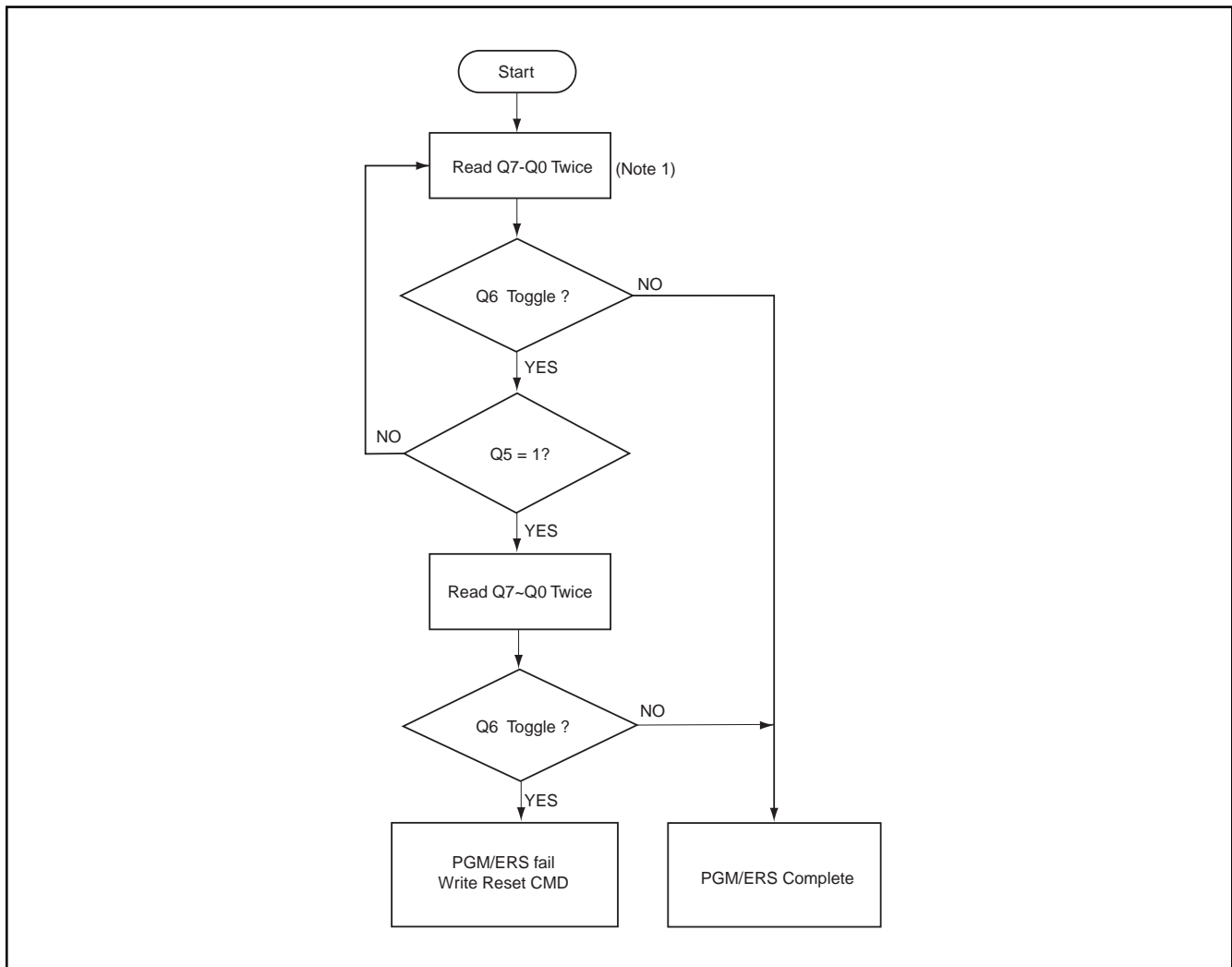
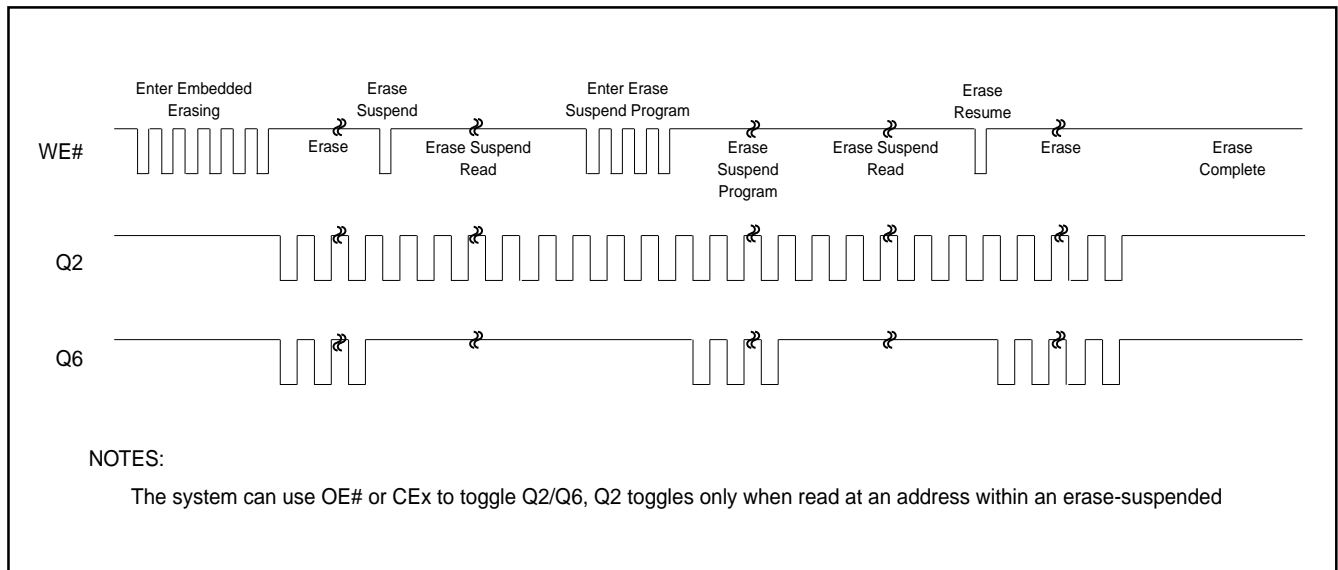


Figure 26. TOGGLE BIT ALGORITHM**Note:**

1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

Figure 27. Q6 versus Q2



RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

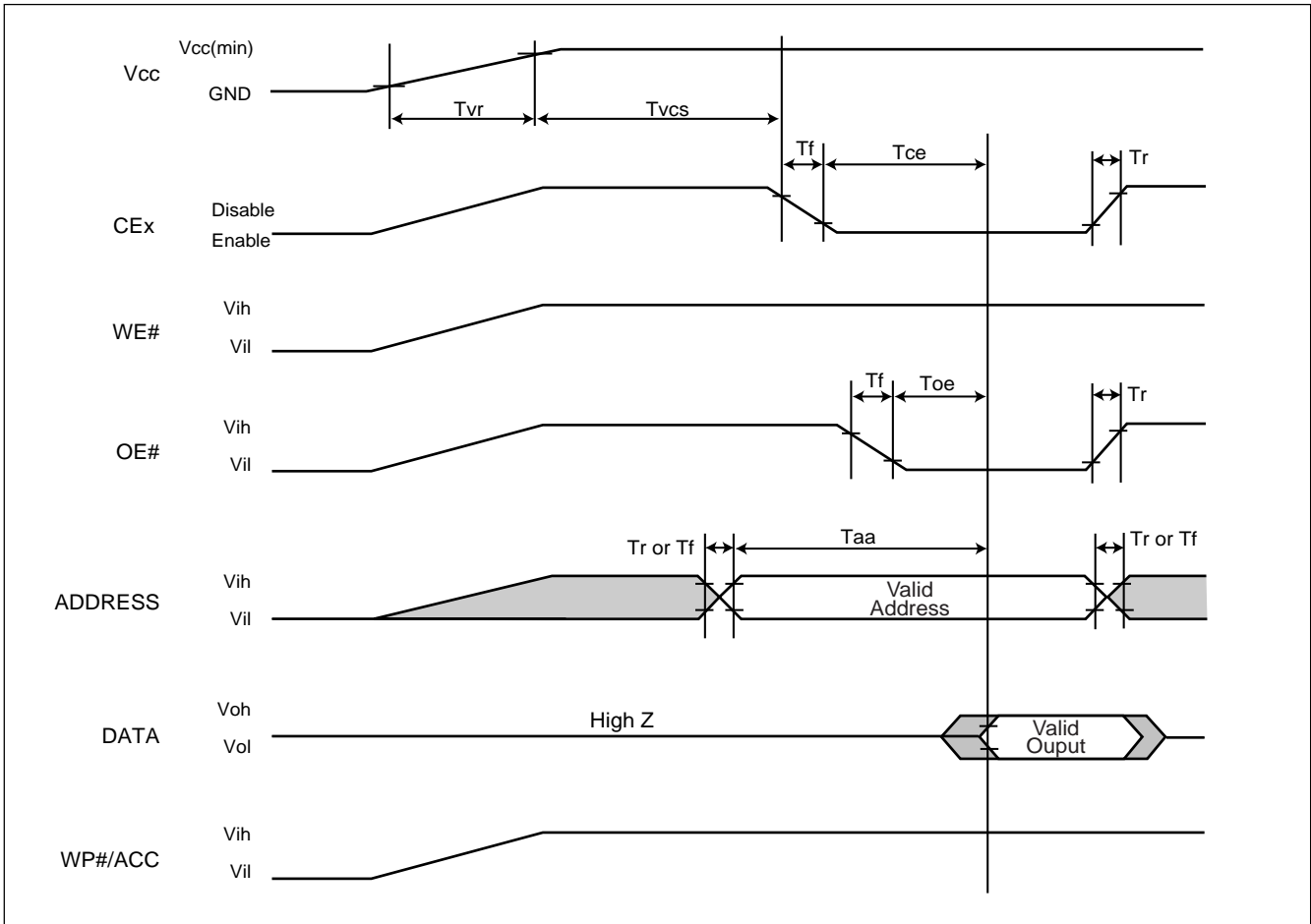


Figure A. AC Timing at Device Power-Up

| Symbol | Parameter | Min. | Max. | Unit |
|-----------|------------------------|------|--------|------|
| T_{vr} | Vcc Rise Time | 80 | 500000 | us/V |
| T_r | Input Signal Rise Time | | 20 | us/V |
| T_f | Input Signal Fall Time | | 20 | us/V |
| T_{vcs} | Vcc Setup Time | 200 | | us |

ERASE AND PROGRAMMING PERFORMANCE

| PARAMETER | LIMITS | | | UNITS |
|------------------------------------|-----------|---------|------|--------|
| | MIN. | TYP.(2) | MAX. | |
| Sector Erase Time | | 0.7 | 2 | sec |
| Chip Erase Time | | 45 | 65 | sec |
| Word Programming Time | | 11 | 360 | us |
| Byte Programming Time | | 9 | 300 | us |
| Accelerated Byte/Word Program Time | | 7 | 210 | us |
| Chip Programming Time | Byte mode | 50 | 160 | sec |
| | Word mode | 45 | 140 | sec |
| Erase/Program Cycles | | 100,000 | | Cycles |

Notes:

1. Typical program and erase times assume the following conditions: 25° C, 3.0V VCC. Programming specifications assume checkboard data pattern.
2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
4. Erase/Program cycles comply with JEDEC JESD-47E & A117A standard.

LATCH-UP CHARACTERISTICS

| | MIN. | MAX. |
|---|--------|-----------|
| Input Voltage voltage difference with GND on WP#/ACC, A9, OE#, RESET# pins | -1.0V | 10.5V |
| Input Voltage voltage difference with GND on all I/O pins | -1.0V | 1.5 x Vcc |
| Vcc current pulse | -100mA | +100mA |
| Includes all pins except Vcc. Test conditions: Vcc = 3.0V, one pin at a time. | | |

PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Set | TYP | MAX | UNIT |
|------------------|-------------------------|----------|-----|-----|------|
| CIN | Input Capacitance | VIN=0 | 6 | 7.5 | pF |
| COUT | Output Capacitance | VOUT=0 | 8.5 | 12 | pF |
| CIN2 | Control Pin Capacitance | VIN=0 | 7.5 | 9 | pF |

Notes:

1. Test conditions TA=25° C, f=1.0MHz.



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MX29LA641D H/L

ORDERING INFORMATION

Please contact Macronix sales for specific information regarding 64-ball BGA (10x13mm) ordering information.



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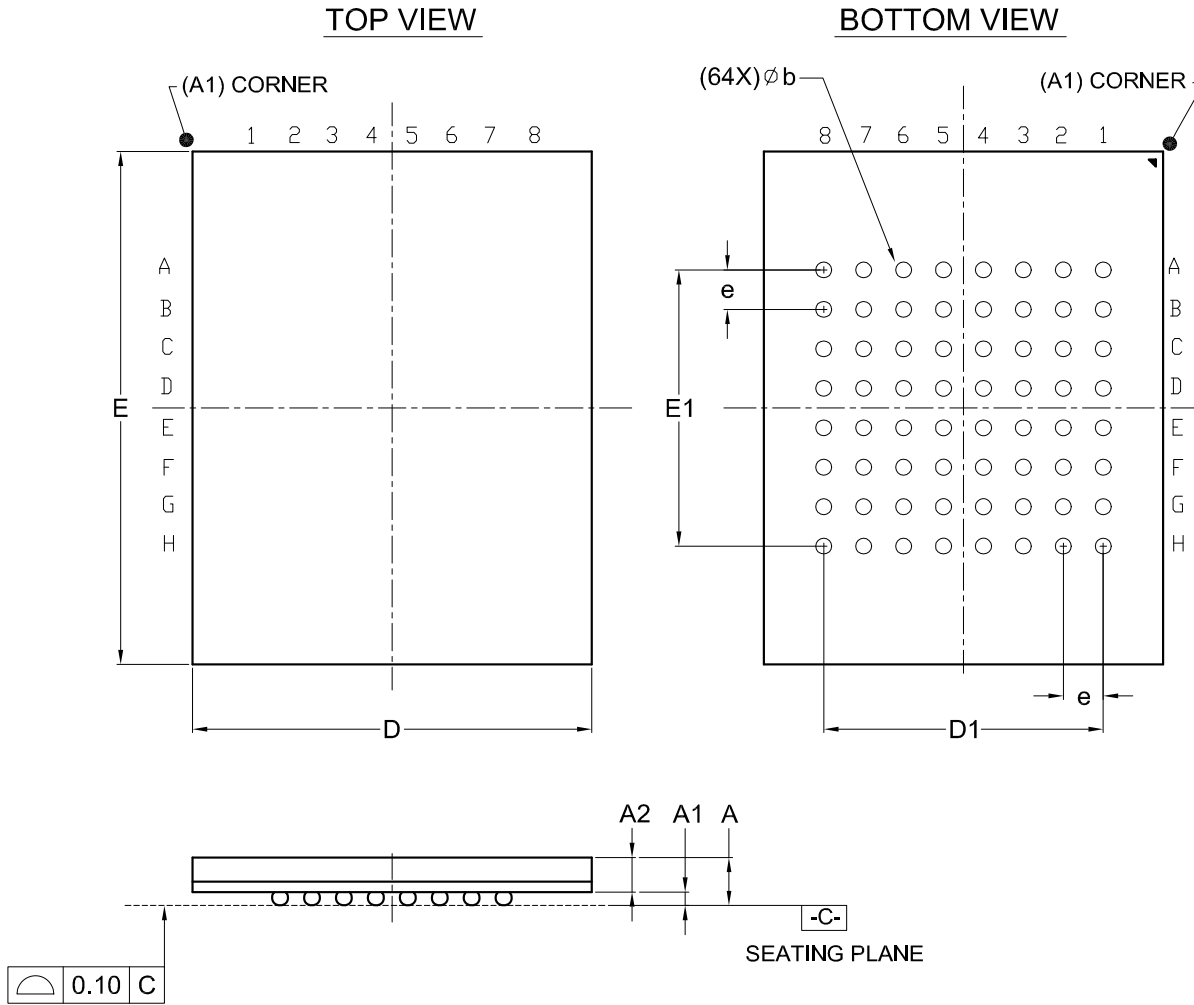
MX29LA641D H/L

PART NAME DESCRIPTION

Please contact Macronix sales for specific information regarding 64-ball BGA (10x13mm) part name description.

PACKAGE INFORMATION

Title: Package Outline for CSP 64BALL(10X13X1.2MM,BALL PITCH 1.00MM,BALL DIAMETER 0.4MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|--------|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| mm | Min. | --- | 0.25 | 0.65 | 0.35 | 9.90 | | 12.90 | | |
| | Nom. | --- | 0.30 | --- | 0.40 | 10.00 | 7.00 | 13.00 | 7.00 | 1.00 |
| | Max. | 1.20 | 0.35 | --- | 0.45 | 10.10 | | 13.10 | | |
| Inch | Min. | --- | 0.010 | 0.026 | 0.014 | 0.390 | | 0.508 | | |
| | Nom. | --- | 0.012 | --- | 0.016 | 0.394 | 0.276 | 0.512 | 0.276 | 0.039 |
| | Max. | 0.047 | 0.014 | --- | 0.018 | 0.398 | | 0.516 | | |

| DWG.NO. | REVISION | REFERENCE | | | ISSUE DATE |
|-----------|----------|-----------|------|--|------------|
| | | JEDEC | EIAJ | | |
| 6110-4220 | 3 | MO-216 | | | 12-15-03 |



REVISION HISTORY

| Revision No. | Description | Page | Date |
|---------------------|--|-------------|-------------|
| 1.0 | 1. Format changed | All | AUG/29/2008 |
| | 2. Corrected WP# function description | P10,11,14 | |
| | 3. Revised Sector Erase Time | P29,58 | |
| | 4. Changed Vhv spec as 9.5V~10.5V | P39 | |
| | 5. Removed "Advanced Information" | P1 | |
| | 6. Revised GENERAL DESCRIPTION | P2 | |
| | 7. Revised AUTOMATIC SELECT OPERATION | P16 | |
| | 8. Revised SOFTWARE COMMAND DEFINITIONS | P17 | |
| 1.1 | 1. Modified table 2-2. 2nd cycle from 1Dh to 13h | P11 | JAN/06/2008 |

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