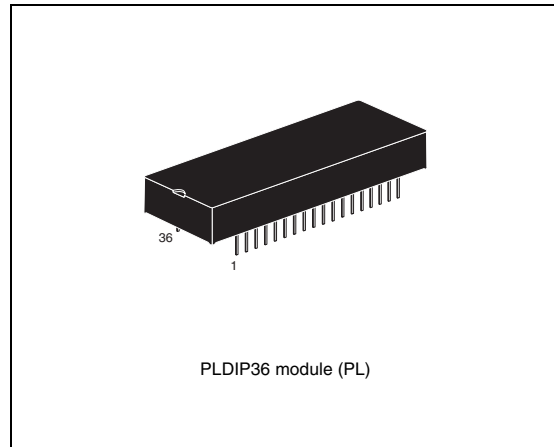# M48Z2M1Y
M48Z2M1V

5 V or 3.3 V, 16 Mbit (2 Mb x 8) ZEROPOWER® SRAM

Features

■ Integrated, ultra low power SRAM, power-fail control circuit, and batteries

■ Conventional SRAM operation; unlimited WRITE cycles

■ 10 years of data retention in the absence of power

■ Automatic power-fail chip deselect and WRITE protection

■ WRITE protect voltages
  (V_{PFD} = Power-fail deselect voltage):
  – M48Z2M1Y: V_{CC} = 4.5 to 5.5 V
    4.2 V ≤ V_{PFD} ≤ 4.5 V
  – M48Z2M1V: V_{CC} = 3.0 to 3.6 V
    2.8 V ≤ V_{PFD} ≤ 3.0 V
    M48Z2M1V not recommended for new design. Contact ST sales office for availability.

■ Batteries are internally isolated until power is applied

■ Pin and function compatible with JEDEC standard 2 Mb x 8 SRAMs

■ RoHS compliant
  – Lead-free second level interconnect

PLDIP36 module (PL)

Contents

List of tables

List of figures

1   Description

The M48Z2M1Y/V ZEROPOWER® RAM is a non-volatile 16,777,216-bit, static RAM organized as 2,097,152 words by 8 bits. The device combines two internal lithium batteries, CMOS SRAMs and a control circuit in a plastic 36-pin DIP, long module.

The ZEROPOWER RAM replaces industry standard SRAMs. It provides the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

Figure 1.   Logic diagram
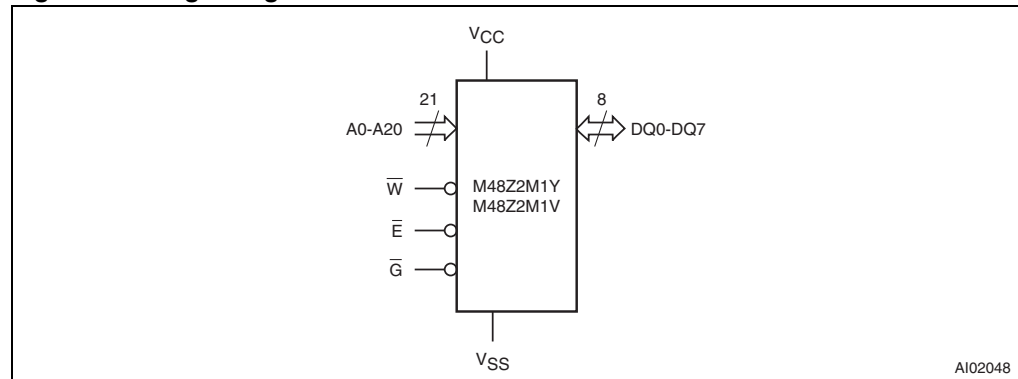
Table 1.   Signal names

A0-A20	Address inputs
DQ0-DQ7	Data inputs / outputs
$\overline{E}$	Chip enable
$\overline{G}$	Output enable
$\overline{W}$	WRITE enable
V_{CC}	Supply voltage
V_{SS}	Ground
NC	Not connected internally

Figure 2.   DIP connections


```
            NC [ 1          36 ] VCC
           A20 [ 2          35 ] A19
           A18 [ 3          34 ] NC
           A16 [ 4          33 ] A15
           A14 [ 5          32 ] A17
           A12 [ 6          31 ] W̄
            A7 [ 7          30 ] A13
            A6 [ 8  M48Z2M1Y 29 ] A8
            A5 [ 9  M48Z2M1V 28 ] A9
            A4 [ 10         27 ] A11
            A3 [ 11         26 ] Ḡ
            A2 [ 12         25 ] A10
            A1 [ 13         24 ] Ē
            A0 [ 14         23 ] DQ7
           DQ0 [ 15         22 ] DQ6
           DQ1 [ 16         21 ] DQ5
           DQ2 [ 17         20 ] DQ4
           VSS [ 18         19 ] DQ3
```

AI02049

Figure 3.   Block diagram

AI02050

2 Operation modes

The M48Z2M1Y/V has its own power-fail detect circuit. The control circuitry constantly monitors the single 5 V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3 V, the control circuitry connects the batteries which sustain data until valid power returns.
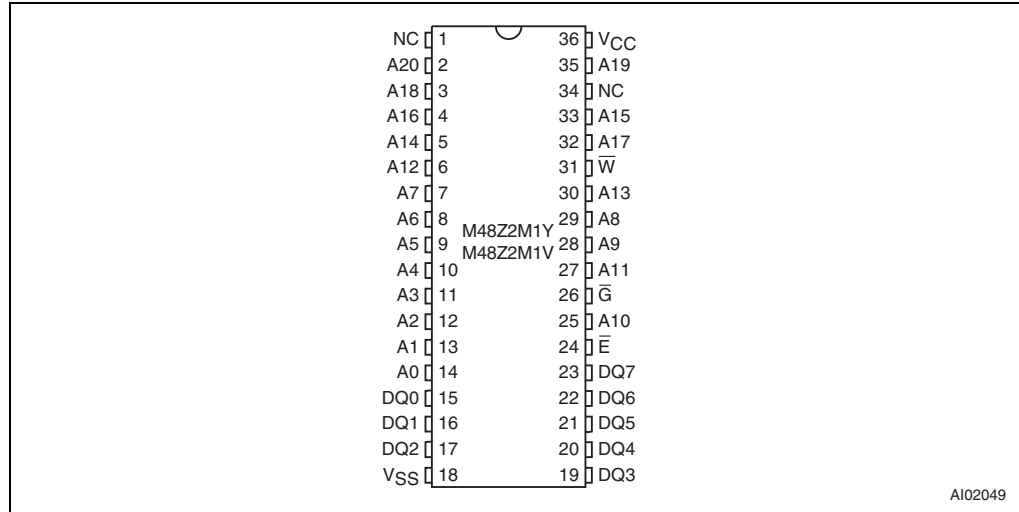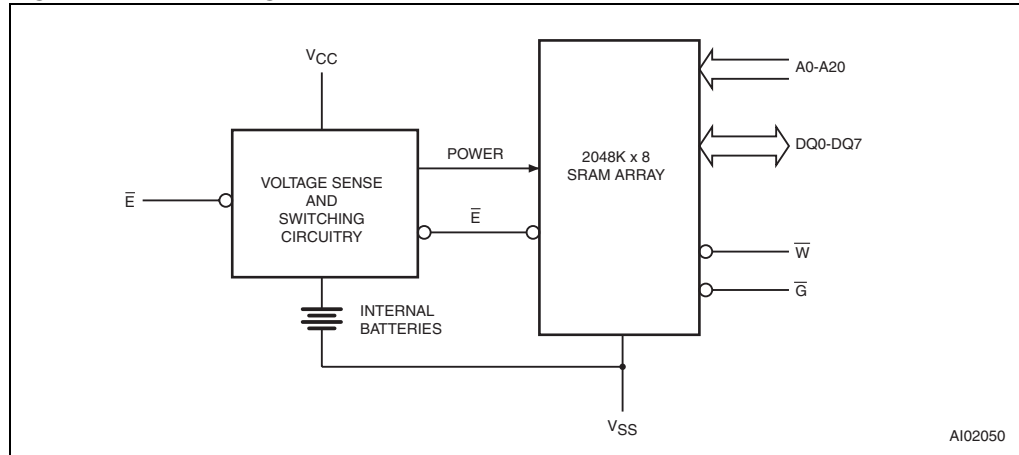
Table 2. Operating modes

| Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	3.0 to 3.6 V or 4.5 to 5.5 V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)[1]	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$[1]	X	X	X	High Z	Battery backup mode

1. See *Table 10 on page 15* for details.

Note: *$X = V_{IH}$ or V_{IL}; V_{SO} = battery backup switchover voltage.*
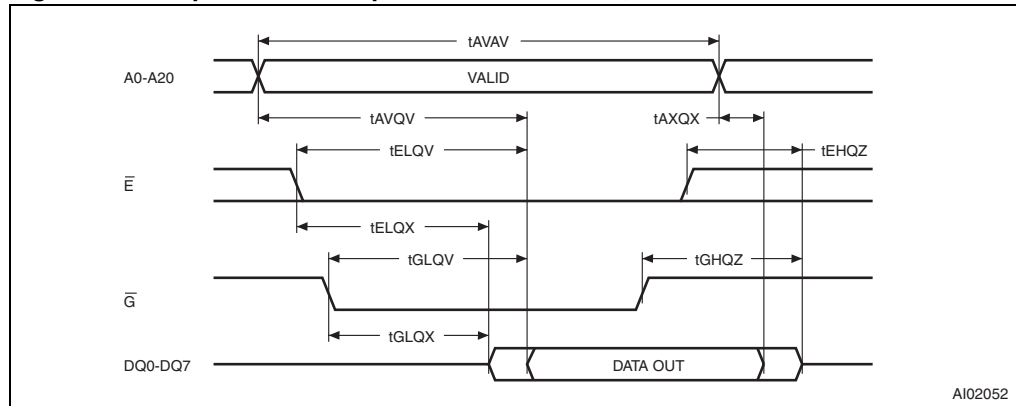
2.1 READ mode

The M48Z2M1Y/V is in the READ mode whenever $\overline{W}$ (WRITE enable) is high and $\overline{E}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 16,777,216 locations in the static storage array. Thus, the unique address specified by the 21 address inputs defines which one of the 2,097,152 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ (chip enable) and $\overline{G}$ (output enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of chip enable access time (t_{ELQV}) or output enable access time (t_{GLQV}). The state of the eight three-state data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the address inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for output data hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 4. Address controlled, READ mode AC waveforms
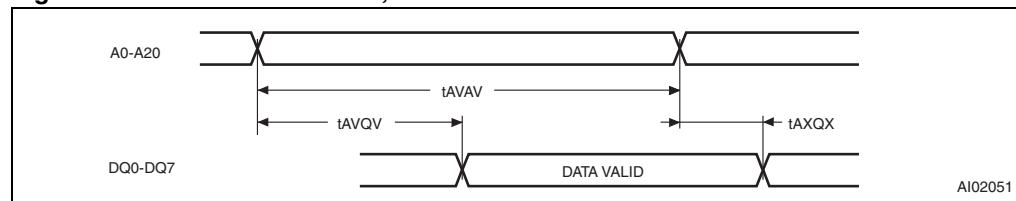
Note: *Chip enable ($\overline{E}$) and output enable ($\overline{G}$) = low, WRITE enable ($\overline{W}$) = high.*

Figure 5.   Chip enable or output enable controlled, READ mode AC waveforms

Note: *WRITE enable ($\overline{W}$) = high.*

Table 3.   READ mode AC characteristics

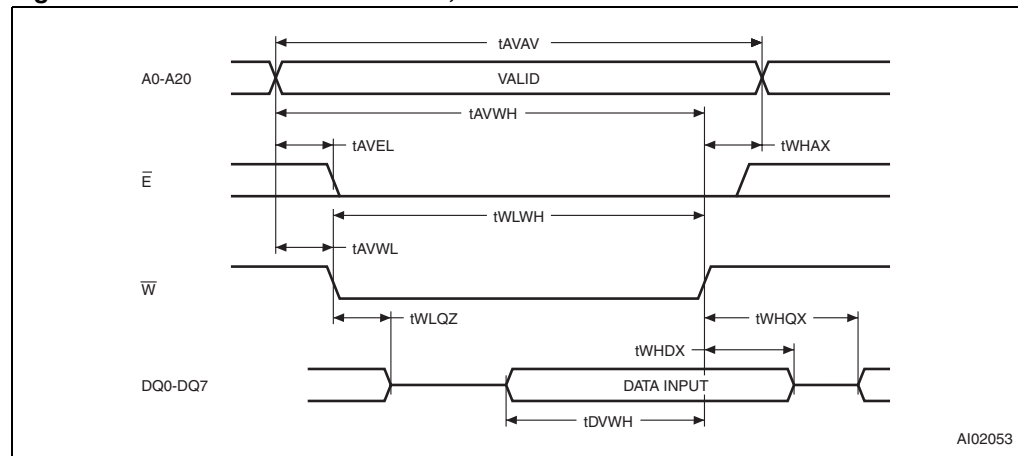| Symbol	Parameter[1]	M48Z2M1Y		M48Z2M1V		Unit
		−70		−85		
		Min	Max	Min	Max	
t_{AVAV}	READ cycle time	70		85		ns
t_{AVQV}[2]	Address valid to output valid		70		85	ns
t_{AXQX}[2]	Address transition to output transition	5		5		ns
t_{EHQZ}[3]	Chip enable high to output Hi-Z		30		35	ns
t_{ELQV}[2]	Chip enable low to output valid		70		85	ns
t_{ELQX}[3]	Chip enable low to output transition	5		5		ns
t_{GHQZ}[3]	Output enable high to output Hi-Z		25		35	ns
t_{GLQV}[2]	Output enable low to output valid		35		45	ns
t_{GLQX}[3]	Output enable low to output transition	5		5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).

2. C_L = 100 pF or 50 pF (see *Figure 9 on page 13*).

3. C_L = 5 pF (see *Figure 9 on page 13*).

2.2 WRITE mode

The M48Z2M1Y/V is in the WRITE mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVEH} or t_{DVWH} prior to the end of WRITE and remain valid for t_{EHDX} or t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 6.   WRITE enable controlled, WRITE mode AC waveforms

Note: Output enable $(\overline{G})$ = high.

Figure 7.   Chip enable controlled, WRITE mode AC waveforms
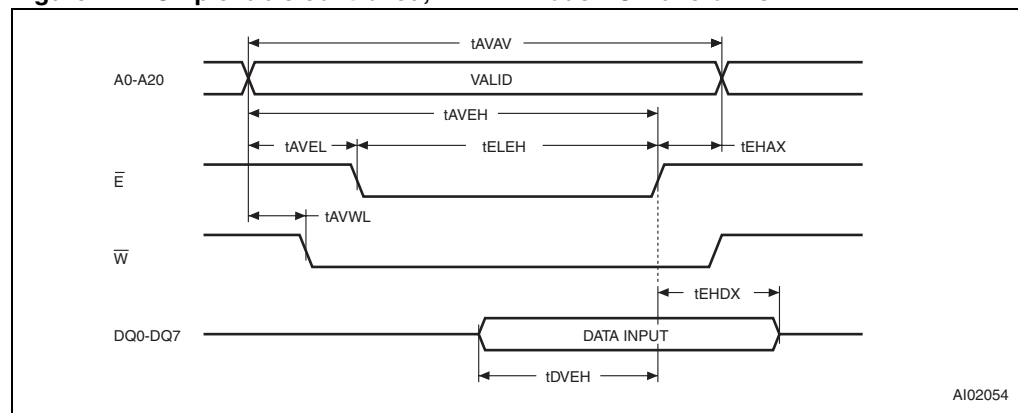
Note: Output enable $(\overline{G})$ = high.

Table 4.   WRITE mode AC characteristics

Symbol	Parameter[1]	M48Z2M1Y		M48Z2M1V		Unit
		−70		−85		
		Min	Max	Min	Max	
t_{AVAV}	WRITE cycle time	70		85		ns
t_{AVEH}	Address valid to chip enable high	65		75		ns
t_{AVEL}	Address valid to chip enable low	0		0		ns
t_{AVWH}	Address valid to WRITE enable high	65		75		ns
t_{AVWL}	Address valid to WRITE enable low	0		0		ns
t_{DVEH}	Input valid to chip enable high	30		35		ns
t_{DVWH}	Input valid to WRITE enable high	30		35		ns
t_{EHAX}	Chip enable high to address transition	15		15		ns
t_{EHDX}	Chip enable high to input transition	10		15		ns
t_{ELEH}	Chip enable low to chip enable high	55		75		ns
t_{WHAX}	WRITE enable high to address transition	5		5		ns
t_{WHDX}	WRITE enable high to input transition	0		0		ns
t_{WHQX}[2][3]	WRITE enable high to output transition	5		5		ns
t_{WLQZ}[2][3]	WRITE enable low to output Hi-Z		25		30	ns
t_{WLWH}	WRITE enable pulse width	55		65		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6V (except where noted).

2. C_L = 5 pF (see *Figure 9 on page 13*).

3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

2.3   Data retention mode

With valid V_{CC} applied, the M48Z2M1Y/V operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "Don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP} write protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

The internal coin cells will maintain data in the M48Z2M1Y/V after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the batteries are disconnected, and the power supply is switched to external V_{CC}. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

For more information on battery storage life refer to the application note AN1012.

2.4 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 µF (as shown in *Figure 8*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 8.   Supply voltage protection
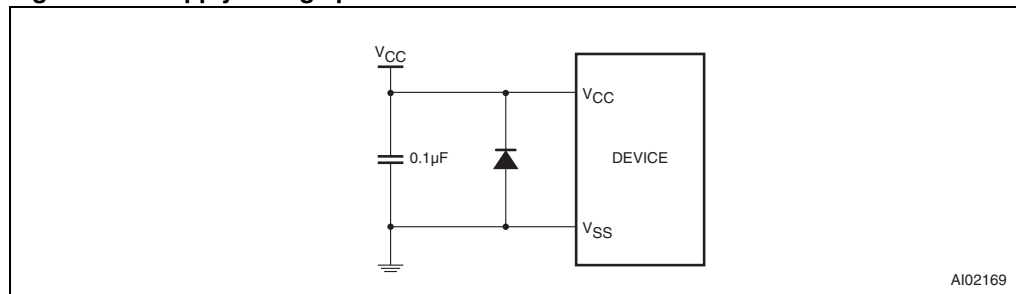
3 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_A	Ambient operating temperature		0 to 70	°C
T_{STG}	Storage temperature (V_{CC} off)		−40 to 85	°C
T_{BIAS}	Temperature under bias		−40 to 85	°C
T_{SLD}[(1)]	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages	M48Z2M1Y	−0.3 to 7	V
		M48Z2M1V	−0.3 to 4.6	V
V_{CC}	Supply voltage	M48Z2M1Y	−0.3 to 7	V
		M48Z2M1V	−0.3 to 4.6	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. Soldering temperature of the IC leads is to not exceed 260 °C for 10 seconds. In order to protect the lithium battery, preheat temperatures must be limited such that the battery temperature does not exceed +85 °C. Furthermore, the devices shall not be exposed to IR reflow.

Caution: *Negative undershoots below −0.3 V are not allowed on any pin while in the battery backup mode.*

4   DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 6.   Operating and AC measurement conditions

Parameter	M48Z2M1Y	M48Z2M1V	Unit
Supply voltage (V_{CC})	4.5 to 5.5	3.0 to 3.6	V
Ambient operating temperature (T_A)	0 to 70	0 to 70	°C
Load capacitance (C_L)	100	50	pF
Input rise and fall times	≤ 5	≤ 5	ns
Input pulse voltages	0 to 3	0 to 3	V
Input and output timing ref. voltages	1.5	1.5	V

Note: *Output Hi-Z is defined as the point where data is no longer driven.*
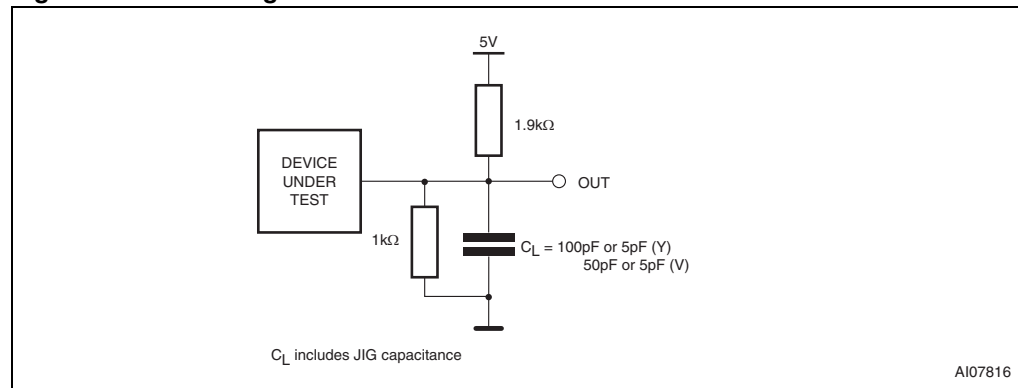
Figure 9.   AC testing load circuit

Table 7.   Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance	-	40	pF
C_{IO}[3]	Input / output capacitance	-	40	pF

1. Effective capacitance measured with power supply at 5 V; sampled only, not 100% tested.

2. Outputs deselected.

3. At 25 °C.

Table 8.   DC characteristics

Sym	Parameter	Test condition[1]	M48Z2M1Y		M48Z2M1V		Unit
			Min	Max	Min	Max	
I_{LI}[2]	Input leakage current	$0\,V \le V_{IN} \le V_{CC}$		±4		±4	µA
I_{LO}[2]	Output leakage current	$0\,V \le V_{OUT} \le V_{CC}$		±4		±4	µA
I_{CC}	Supply current	$\overline{E} = V_{IL}$, Outputs open		140		70	mA
I_{CC1}	Supply current (standby) TTL	$\overline{E} = V_{IH}$		10		2	mA
I_{CC2}	Supply current (standby) CMOS	$\overline{E} \ge V_{CC} - 0.2\,V$		8		1	mA
V_{IL}	Input low voltage		–0.3	0.8	–0.3	0.6	V
V_{IH}	Input high voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1\,mA$		0.4		0.4	V
V_{OH}	Output high voltage	$I_{OH} = -1\,mA$	2.4		2.2		V

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).

2. Outputs deselected.
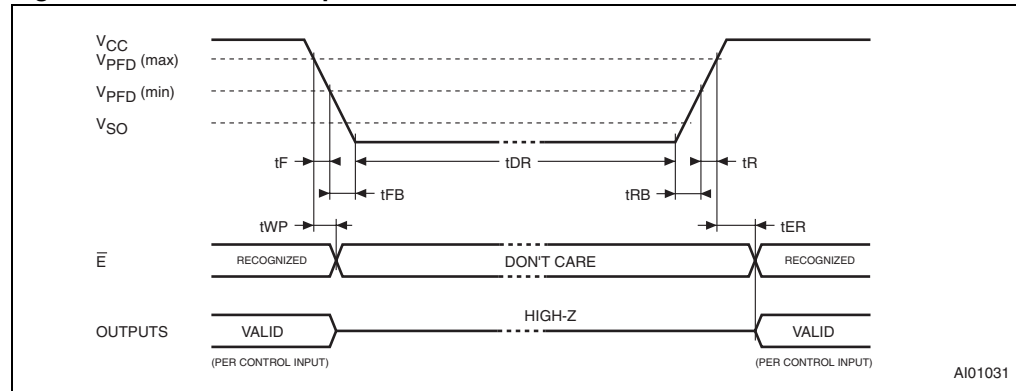
Figure 10. Power down/up mode AC waveforms

Table 9. Power down/up AC characteristics

Symbol	Parameter[1]		Min	Max	Unit
t_{ER}	$\overline{E}$ recovery time		40	120	ms
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time		300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SO} V_{CC} fall time	M48Z2M1Y	10		µs
		M48Z2M1V	150		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time		10		µs
t_{WP}	Write protect time from $V_{CC} = V_{PFD}$	M48Z2M1Y	40	150	µs
		M48Z2M1V	40	250	µs

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).

2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).

3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

**Table 10. Power down/up trip points DC characteristics**

Symbol	Parameter[1][2]		Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	M48Z2M1Y	4.2	4.3	4.5	V
		M48Z2M1V	2.8	2.9	3.0	V
V_{SO}	Battery backup switchover voltage	M48Z2M1Y		3.0		V
		M48Z2M1V		2.45		V
t_{DR}[3]	Expected data retention time		10			YEARS

1. All voltages referenced to V_{SS}.

2. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).

3. At 25 °C; V_{CC} = 0 V.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 11.   PLDIP36 – 36-pin plastic DIP long module, package outline
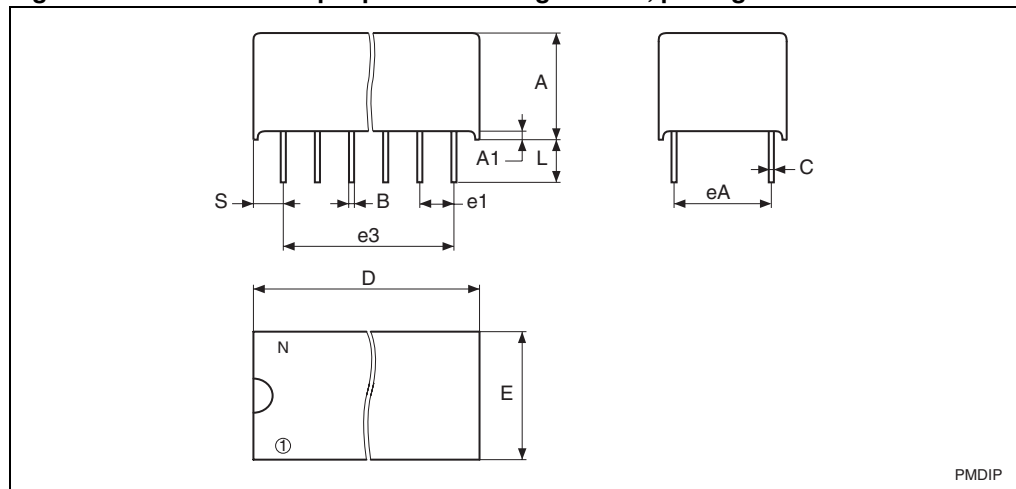
Note: Drawing is not to scale.

Table 11.   PLDIP36 – 36-pin plastic DIP long module, package mechanical data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.3650	0.3748
A1		0.38			0.0150	
B		0.43	0.59		0.0169	0.0232
C		0.20	0.33		0.0079	0.0130
D		52.58	53.34		2.0701	2.1000
E		18.03	18.80		0.7098	0.7402
e1		2.30	2.81		0.0906	0.1106
e3	43.18			1.7		
eA		14.99	16.00		0.5902	0.6299
L		3.05	3.81		0.1201	0.1500
S		4.45	5.33		0.1752	0.2098
N	36			36		

6   Part numbering

Table 12.   Ordering information scheme

Example: M48Z   2M1Y   −70   PL   1

Device type

M48Z

Supply voltage and write protect voltage

2M1Y = V_{CC} = 4.5 to 5.5 V; V_{PFD} = 4.2 to 4.5 V

2M1V = V_{CC} = 3.0 to 3.6 V; V_{PFD} = 2.8 to 3.0 V[1]

Speed

−70 = 70 ns (Y)

−85 = 85 ns (V)[1]

Package

PL = PLDIP36

Temperature range

1 = 0 to 70°C

9[2] = extended temperature

Shipping method

blank = ECOPACK® package, tubes

1.   Not recommended for new design. Contact ST sales office for availability.

2.   Contact ST sales office for availability of extended temperature.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

7 Environmental information

Figure 12. Recycling symbols
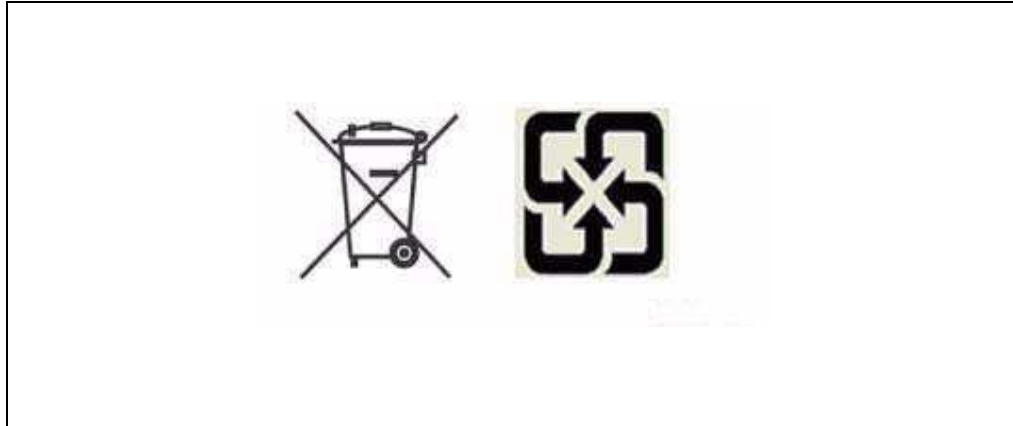
This product contains a non-rechargeable lithium (lithium carbon monofluoride chemistry) button cell battery fully encapsulated in the final product.

Recycle or dispose of batteries in accordance with the battery manufacturer's instructions and local/national disposal and recycling regulations.

Please refer to the following web site address for additional information regarding compliance statements and waste recycling.

Go to www.st.com/nvram, then select "Lithium Battery Recycling" from "Related Topics".

8 Revision history

Table 13.   Document revision history

Date	Revision	Changes
Jul-1999	1	First issue
31-Aug-2000	2	From preliminary data to datasheet
20-Mar-2002	3	Reformatted; temperature information added to tables (*Table 7*, *8*, *3*, *4*, *9*, *10*)
29-May-2002	3.1	Modified "V_{CC} noise and negative going transients" text
28-Mar-2003	3.2	Remove 5 V/5%, add 3 V part (*Figure 1*, *2*, *9*; *Table 5*, *6*, *8*, *2*, *3*, *4*, *9*, *10*, *12*)
02-Jul-2003	3.3	Changed characteristic (*Table 8*)
18-Feb-2005	4	Reformatted; IR reflow update (*Table 5*)
02-Aug-2010	5	Updated *Features*, *Section 3*, *Table 12*; added ECOPACK® text to *Section 5*; added *Section 7: Environmental information*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com