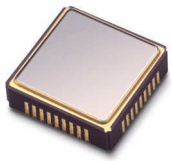
GENERAL DESCRIPTION



The M2050/51/52 is a VCSO (Voltage Controlled SAW Oscillator) based clock PLL designed for FEC clock ratio translation in 10Gb optical systems such as 10GbE 64b/66b. It supports both mapping and de-mapping of 64b/66b encoding and FEC (Forward Error Correction) clock multiplication ratios. The ratios are pin-selected from pre-programming look-up tables.

FEATURES

- **Integrated SAW delay line; Output of 15 to 700 MHz ***
- **Low phase jitter < 0.5 ps rms typical (12kHz to 20MHz or 50Hz to 80MHz)**
- **Pin-selectable PLL divider ratios support 64b/66b and FEC encoding/decoding ratios:**
  - **M2050: Map 10GbE to LAN, 255/238 FEC, or 255/237 FEC**
  - **M2051: De-map 10GbE LAN or 255/238 FEC to 10GbE**
  - **M2052: De-map 255/237 FEC & 255/238 FEC to 10GbE LAN**
- **Scalable dividers provide further adjustment of loop bandwidth as well as jitter tolerance**
- **LVPECL clock output (CML and LVDS options available)**
- **Reference clock inputs support differential LVDS, LVPECL, as well as single-ended LVCMOS, LVTTL**
- **Loss of Lock (LOL) output pin**
- **Narrow Bandwidth control input (NBW Pin)**
- **Hitless Switching (HS) options with or without Phase Build-out (PBO) available; performance conforms with SONET (GR-253) /SDH (G.813) MTIE and TDEV during reference clock reselection**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

PIN ASSIGNMENT (9 x 9 mm SMT)

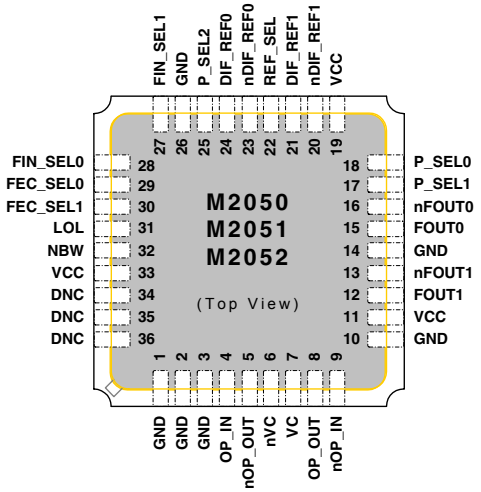


Figure 1: Pin Assignment

Example I/O Clock Frequency Combinations Using M2050 Mapper PLL

Base Input Rate (MHz)[1]	Mapper Ratio Mfec / Rfec (Pin Selectable)	VCSO* and Base Output Rate (MHz)[2]
625.0000	33 / 32	644.5313
625.0000	15 / 14	669.6429
644.5313	15 / 14	690.5692

Table 1: Example I/O Clock Frequency Combinations

Note 1: Input reference clock can be base rate divided by "Mfin".
Note 2: Output rate can be base rate divided by "P".
* Specify VCSO center frequency at time of order.

SIMPLIFIED BLOCK DIAGRAM

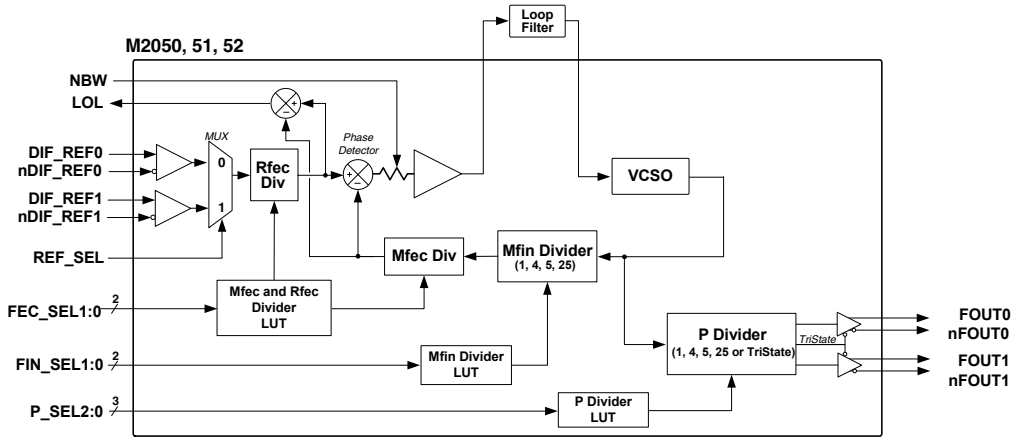


Figure 2: Simplified Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 5, External Loop Filter, on pg. 8.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12 13	FOUT1 nFOUT1	Output	No internal terminator	Clock output pair 1. Differential LVPECL.
15 16	FOUT0 nFOUT0	Output	No internal terminator	Clock output pair 0. Differential LVPECL.
17 18 25	P_SEL1 P_SEL0 P_SEL2	Input	Internal pull-down resistor[1]	Post-PLL , P divider selection. LVCMOS/LVTTL. See Table 7, P Divider Look-Up Table (LUT), on pg. 4.
20	nDIF_REF1	Input	Biased to Vcc/2 [2]	Reference clock input pair 1. Differential LVPECL or LVDS. Resistor bias on inverting terminal supports TTL or LVCMOS.
21	DIF_REF1		Internal pull-down resistor[1]	
22	REF_SEL	Input	Internal pull-down resistor[1]	Reference clock input selection. LVCMOS/LVTTL: Logic 1 selects DIF_REF1, nDIF_REF1. Logic 0 selects DIF_REF0, nDIF_REF0.
23	nDIF_REF0	Input	Biased to Vcc/2 [2]	Reference clock input pair 0. Differential LVPECL or LVDS. Resistor bias on inverting terminal supports TTL or LVCMOS.
24	DIF_REF0		Internal pull-down resistor [1]	
27 28	FIN_SEL1 FIN_SEL0	Input	Internal pull-down resistor[1]	Input clock frequency selection. LVCMOS/LVTTL. See Table 3 Mfin Divider Look-Up Tables (LUT) on pg. 3.
29 30	FEC_SEL0 FEC_SEL1	Input	Internal pull-down resistor[1]	Mfec and Rfec divider value selection. LVCMOS/ LVTTL. See Tables 4, 5,and 6 on pg. 3.
31	LOL	Output		Loss of Lock indicator output. Asserted when internal PLL is not tracking the input reference for frequency and phase. [3] Logic 1 indicates loss of lock. Logic 0 indicates locked condition.
32	NBW	Input	Internal pull-UP resistor[1]	Narrow Bandwidth enable. LVCMOS/LVTTL: Logic 1 - Narrow loop bandwidth, R_{IN} = 2100kΩ. Logic 0 - Wide bandwidth, R_{IN} = 100kΩ.
34, 35, 36	DNC		Do Not Connect.	

Table 2: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-up resistors, see **DC Characteristics** on pg. 10.
Note 2: Biased toVcc/2, with 50kΩ to Vcc and 50kΩ to ground. See **Differential Inputs Biased to VCC/2** in DC Characteristics on pg. 10.
Note 3: See **LVCMOS Output** in DC Characteristics on pg. 10.

DETAILED BLOCK DIAGRAM

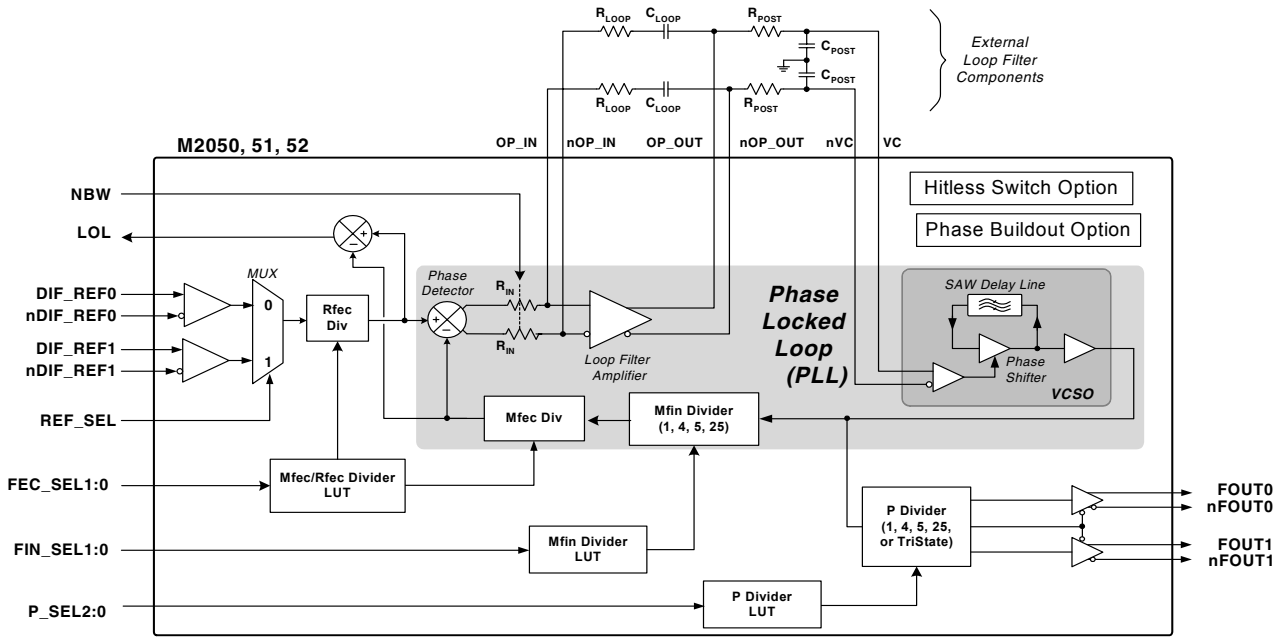


Figure 3: Detailed Block Diagram

DIVIDER SELECTION TABLES

Mfin Divider Look-Up Tables (LUT)

The FIN_SEL1:0 pins select the feedback divider value ("Mfin"). Since the VCSO frequency is fixed, this allows input reference selection. The look-up tables vary by device variant.

M2050/51/52: Mfin Value LUT

FIN_SEL1:0	Mfin Value	Sample Input Reference Freq. (MHz) Options For M2050[1], M2051 & M2052[2]
0 0	25	25.00
0 1	5	125.00
1 0	4	156.25
1 1	1	625.00

Table 3: M2050/51/52: Mfin Value LUT

Note 1: For M2050 with Fvcso = 669.6429
Note 2: For M2051 and M2052 with Fvcso = 625.0000.

Mfec and Rfec Divider Look-Up Tables (LUTs)

The FEC_SEL pins select the Mfec/Rfec divider ratio. The look-up tables vary by device variant. The Mfec and Rfec values also establish phase detector frequency. A lower phase detector frequency improves jitter tolerance and lowers loop bandwidth.

M2050: Map LUT (10GbE to LAN, 255/238 FEC, or 255/237 FEC)

FEC_SEL1:0 1 0	Mfec	Rfec	Description	Base Input Rate (MHz)	Fvcso = Base Output Rate (MHz)
For M2050 with Fvcso = 644.5313 (10GbE to 10GbE LAN rate):					
0 0	33	32	10GbE to 10GbE LAN	625.0000	644.5313
0 1	33	33	10GbE LAN repeater	644.5313	644.5313
For M2050 with Fvcso = 669.6429 (10GbE to 10GbE 255/238 FEC rate):					
1 0	15	14	10GbE to 10GbE 255/238 FEC	625.0000	669.6429
1 1	15	15	10GbE 255/238 FEC repeater	669.6429	669.6429
For M2050 with Fvcso = 690.5692 (10GbE LAN to 10GbE LAN 255/238 FEC):					
1 0	15	14	10GbE LAN to 10GbE LAN 255/238 FEC	644.5313	690.5692
1 1	15	15	10GbE LAN 255/238 FEC repeater	690.5692	690.5692
For M2050 with Fvcso = 693.4830 (10GbE LAN to 10GbE LAN 255/237 FEC):					
0 0	85	79	10GbE LAN to 10GbE LAN 255/237 FEC	644.5313	693.4830
0 1	85	85	10GbE LAN 255/237 FEC repeater	693.4830	693.4830

Table 4: M2050: Map LUT (10GbE to LAN, 255/238 FEC, or 255/237 FEC)

M2051: De-map LUT (10GbE LAN or 255/238 FEC to 10GbE)
Use this option to demap from *either* "10GbE LAN" *or* "10GbE 255/238 FEC" encoded to "10GbE". Also use this option to operate in 10GbE repeater mode.

The de-mapper FEC PLL ratios (in Table 5) enables the **M2051-11-625.0000** *to accept "base" input reference frequencies of:* 625.00MHz *("10GbE"),* 644.5313MHz *("10GbE LAN"), and* 669.6429MHz *("10GbE* 255/238 *FEC").*

FEC_SEL1:0 1 0	Mfec	Rfec	Description	Base Input Rate (MHz)	Fvcso = Base Output Rate (MHz)
***For M2051 with Fvcso* = 625.00**					
0 0	32	33	10GbE LAN to 10GbE	644.5313	625.0000
0 1	32	32	10GbE jitter attenuator	625.0000	625.0000
1 0	28	30	10GbE 255/238 FEC to 10GbE	669.6429	625.0000
1 1	14	15	10GbE 255/238 FEC to 10GbE	669.6429	625.0000

Table 5: M2051: De-map LUT (10GbE LAN or 255/238 FEC to 10GbE)

The Mfec divider value for the first three settings allows one set of passive filter components to be used for all three of these modes.

The fourth setting maps "10GbE 255/238 FEC" using the lowest Mfec value possible. Use this setting to produce the maximum loop bandwidth.

M2052: De-map LUT (255/237 or 255/238 FEC to 10GbE LAN)
This option de-maps from *both* "10GbE LAN 255/237 FEC" *and* "10GbE LAN 255/238 FEC" to "10GbE LAN". Also use this option to operate in 10GbE LAN repeater mode.

The de-mapper FEC PLL ratios (in Table 6) enables the **M2052-11-625.0000** *to accept "base" input reference frequencies of:* 644.5313MHz *("10GbE LAN"),* 690.5692MHz *("10GbE LAN* 255/238 *FEC"), and* 693.4830MHz *("10GbE LAN* 255/237 *FEC").*

FEC_SEL1:0 1 0	Mfec	Rfec	Description	Base Input Rate (MHz)	Fvcso = Base Output Rate (MHz)
***For* M2052 *with Fvcso* = 625.00**					
0 0	79	85	10GbE LAN 255/237 FEC to 10GbE LAN	693.4830	625.0000
0 1	79	79	10GbE LAN jitter attenuator	644.5313	625.0000
1 0	84	90	10GbE LAN 255/238 FEC to 10GbE LAN	690.5692	625.0000
1 1	84	84	10GbE LAN jitter attenuator	644.5313	625.0000

Table 6: M2052: De-map LUT (255/237 or 255/238 FEC to 10GbE LAN)

Use this option for multi-rate de-mapping applications that require one set of PLL passive filter values to operate over *both* "10GbE LAN 255/237 FEC" and "10GbE LAN 255/238 FEC". The Mfec divider value is kept nearly constant to maintain similar loop bandwidth using one set of external filter component values.

P Divider Look-Up Table (LUT)

The P_SEL2:0 pins select the P divider values, which set the output clock frequencies. A P divider of value of 1 will provide a 625.00MHz output when using a 625.00MHz VCSO, for example. P divider values of 4, 5, or 25 are also available, plus a TriState mode. The outputs can be placed into the valid state combinations as listed in Table 7. (The outputs cannot each be placed into any of the five available states independently.)

P_SEL2:0	P Value for FOUT0	P Value for FOUT1	M2050-625.0000 Output Frequency (MHz) FOUT0	FOUT1
0 0 0	25	1	25.00	625.00
0 0 1	25	4	25.00	156.25
0 1 0	1	1	625.00	625.00
0 1 1	4	1	156.25	625.00
1 0 0	5	5	125.00	125.00
1 0 1	4	4	156.25	156.25
1 1 0	5	4	125.00	156.25
1 1 1	TriState	TriState	N/A	N/A

Table 7: P Divider Look-Up Table (LUT)

General Guideline for Mfec and Rfec Divider Selection
When LOL is to be used for system health monitoring, the phase detector frequency should be 5MHz or greater. Low phase detector frequencies make LOL overly sensitive, and higher phase detector frequencies make LOL less sensitive. The LOL pin should not be used during loop timing mode.

FUNCTIONAL DESCRIPTION

The M2050/51/52 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of two selectable input reference clocks.

An internal high "Q" SAW delay line provides low jitter signal performance and establishes the output frequency of the VCSO (Voltage Controlled SAW Oscillator). In a given M2050/51/52 device, the VCSO center frequency is fixed. A common center frequency is 625.00MHz, for 10GbE 64b/66b optical network applications. The VCSO center frequency is specified at time of order (see "Ordering Information" on pg. 12). The VCSO has a guaranteed tuning range of ±120 ppm (commercial temperature grade).

Pin selectable dividers are used within the PLL and for the output clock. This enables tailoring of device functionality and performance. The FEC feedback and reference dividers (the "Mfec Divider" and "Rfec Divider") provide the multiplication ratios necessary to accomodate clock translation for both forward and inverse Forward Error Correction. The Mfec and Rfec

dividers also control the phase detector frequency. The feedback divider (labeled "Mfin Divider") provides the broader division options needed to accomodate various reference clock frequencies.

For example, the **M2051-11-625.0000** *(see "Ordering Information"* on pg. 12*)* has a 625.00MHz VCSO frequency:

- The de-mapper FEC PLL ratios (in Tables 5 and 6) enable the **M2051-11-625.0000** to accept "base" input reference frequencies of: 625.00MHz ("10GbE"), 644.5313MHz ("10GbE LAN"), and 669.6429MHz ("10GbE 255/238 FEC").
- The Mfin feedback divider enables the actual input reference clock to be the base input frequency divided by 1, 4, 5, or 25. Therefore, for the base input frequency of 625.00MHz, the actual input reference clock frequencies can be: 625.00, 156.25, 125.00, and 25.00MHz. (See Table 3 on pg. 3.)

Key to Device Variants and Look-up Table Options

Device Variant	Look-up Table Option	
	Mfin Lookup Table is:	Mfec Look-up Table is:
M2050	Table 3	Table 4 (mapper LUT)
M2051		Table 5 (de-mapper LUT)
M2052		Table 6 (de-mapper LUT)

Table 8: Key to Device Variants and Look-up Table Options

The M2050/51/52 includes a Loss of Lock (LOL) indicator, which provides status information to system management software. A Narrow Bandwidth (NBW) control pin is provided as an additional mechanism for adjusting PLL loop bandwidth without affecting the phase detector frequency.

Options are available for Hitless Switching (HS) with or without Phase Build-out (PBO). Performance conforms with SONET/ SDH MTIE and TDEV during a reference clock reselection.

Allowance for a single-ended input has been facilitated by a unique input resistor bias scheme, which is described next and shown in Figure 4.

Input Reference Clocks

Two clock reference inputs and a selection mux are provided. Either reference clock input can accept a differential clock signal (such as LVPECL or LVDS) or a single-ended clock input (LVCMOS or LVTTL on the non-inverting input).

A single-ended reference clock on the unselected reference input can cause an increase in output clock jitter. For this reason, differential reference inputs are preferred; interference from a differential input on the non-selected input is minimal.

Configuration of single-ended input has been facilitated by biasing nDIF_REF0 and nDEF_REF1 to Vcc/2, with 50kΩ to Vcc and 50kΩ to ground. The input clock structure, and how it is used with either LVCMOS/LVTTL inputs or a DC- coupled LVPECL clock, is shown in Figure 4.

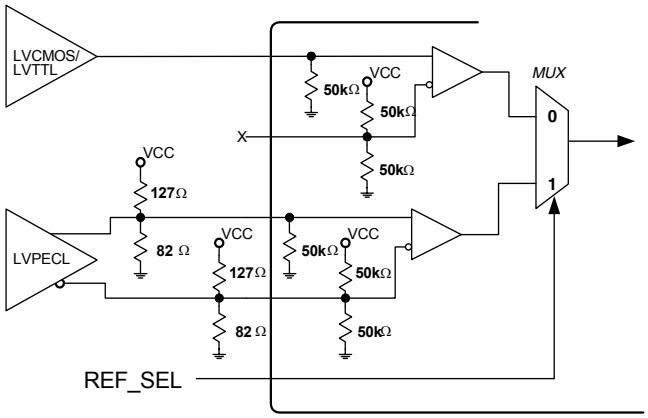


Figure 4: Input Reference Clocks

Differential Inputs

Differential LVPECL inputs are connected to both reference input pins in the usual manner. The external load termination resistors shown in Figure 4 (the 127Ω and 82Ω resistors) is ideally suited for both AC and DC coupled LVPECL reference clock lines. These provide the 50Ω load termination and the VTT bias voltage.

Single-ended Inputs

Single-ended inputs (LVCMOS or LVTTL) are connected to the non-inverting reference input pin (DIF_REF0 or DIF_REF1). The inverting reference input pin (nDIF_REF0 or nDIF_REF1) must be left unconnected.

*In single-ended operation, when the unused inverting input pin (*nDIF_REF0 *or* nDEF_REF1*) is left floating (not connected), the input will self-bias at VCC/2.*

PLL Operation

The M2050/51/52 is a complete clock PLL. It uses a phase detector and configurable dividers to synchronize the output of the VCSO with the selected reference clock.

The PLL will work correctly, meaning it will phase-lock the VCSO output to the input reference clock, when the internal phase detector inputs are able to run at the same frequency. This means the PLL dividers must be set appropriately and a suitable reference frequency must be chosen for the intended output frequency. When the PLL is not set up appropriately, the VCSO is

forced to its upper or lower operating limit which is typically about 250 ppm above or below the VCSO center frequency (no more than 500 ppm above or below).

In normal phase-locked condition, the instantaneous phase error is measured by the phase detector and is converted to charge pump current pulses. These current pulses are then integrated by the external loop filter to create a VCSO control voltage. The loop filter acts as a low pass filter to remove unwanted reference clock jitter above a determined frequency or PLL bandwidth. For reference phase jitter frequencies within the loop bandwidth, phase jitter amplitude is passed on to the output clock according to the PLL loop frequency response curve.
The relationship between the nominal VCSO center frequency (Fvcso), the Mfin divider, the Mfec divider, the Rfec divider, and the input reference frequency (Fin) is:

$$Fvcso = Fin \times Mfin \times \frac{Mfec}{Rfec}$$

The Mfec, Rfec, and Mfin dividers can be set by pin configuration using the input pins FEC_SEL1, FEC_SEL0, FIN_SEL1, and FIN_SEL0.

Post-PLL Divider

The M2050/51/52 also features a post-PLL (P) divider.

Through use of the P divider, the device's output frequency (Fout) can be that of the VCSO (such as 625.00MHz) or the VCSO frequency divided by 4, 5 or 25.

The P_SEL2:0 pins select the value for the P divider. (See Table 7 on pg. 4.)

Accounting for the P divider, the complete relationship between the input clock reference frequency (Fin) and output clock frequency (Fout) is defined as:

$$Fout = \frac{Fvcso}{P} = Fin \times \frac{Mfin \times Mfec}{Rfec \times P}$$

Due to the narrow tuning range of the VCSO (±200ppm), appropriate selection of all of the following are required for the PLL be able to lock: VCSO center frequency, input frequency, and divider selections.

TriState

The TriState feature puts the LVPECL output driver into a high impedance state, effectively disconnecting the driver from the FOUT and nFOUT pins of the device. A logic 0 is then present on the clock net. The impedance of the clock net is then set to 50Ω by the external circuit resistors. (This is in distinction to a CMOS output in TriState, in which case the net goes to a high impedance and the logic value floats.) The 50Ω impedance level of the LVPECL TriState allows manufacturing In-circuit Test to drive the clock net with an external 50Ω generator to validate the integrity of clock net and the clock load.

Any unused output (single-ended or differential) should be left unconnected (floating) in system application. This minimizes output switching current and therefore minimizes noise modulation of the VCSO.

Narrow Bandwidth (NBW) Control Pin

A Narrow Loop Bandwidth control pin (NBW pin) is included to enable adjustment of the PLL loop bandwidth. In wide bandwidth mode (NBW=0), the internal resistor Rin is 100kΩ. With the NBW pin asserted (NBW=1), the internal resistor Rin is changed to 2100kΩ. This lowers the loop bandwidth by a factor of about 21 (approximately 2100 / 100) and lowers the damping factor by a factor of about 4.6 (the square root of 21), assuming the same external loop filter component values.

Loss of Lock Indicator (LOL) Output Pin

Under normal device operation, when the PLL is locked, the LOL Phase Detector drives LOL to logic 0. Under circumstances when the VCSO cannot fully phase lock to the input (as measured by a greater than 4 ns discrepancy between the feedback and reference clock rising edges at the LOL Phase Detector) the LOL output goes to logic 1. The LOL pin will return back to logic 0 when the phase detector error is less than 2 ns. The loss of lock indicator is a low current LVCMOS output.

Guidelines for Using LOL

In a given application, the magnitude of peak-to-peak jitter at the phase detector will usually increase as the Rfec divider is increased. If the LOL pin will be used to detect an unusual clock condition, or a clock fault, the FEC_SEL1:0 pins should be set to provide a phase detector frequency of 5MHz or greater (the phase detector frequency is equal to Fin divided by the Rfec divider). Otherwise, false LOL indications may result. A phase detector frequency of 10MHz or greater is desirable when reference jitter is over 500ps, or when the device is used within a noisy system environment. LOL should not be used when the device is used in a loop timing application.

Optional Hitless Switching and Phase Build-out

The M2050/51/52 is available with a Hitless Switching feature that is enabled during device manufacturing. In addition, a Phase Build-out feature is also offered. These features are offered as device options and are specified by device order code. Refer to “Ordering Information” on pg. 12.

The Hitless Switching feature (with or without Phase Build-out) is designed for applications where switching occurs between two stable system reference clocks. It should not be used in loop timing applications, or when reference clock jitter is greater than 1 ns pk-pk. The Hitless Switching sequence is triggered by the LOL circuit, which is activated by a 4 ns phase transient. This magnitude of phase transient can generated by the CDR (Clock & Data Recovery unit) in loop timing mode, especially during a system jitter tolerance test. It can also be generated by some types of Stratum clock DPLLs (digital PLL), especially those that do not include a post de-jitter APLL (analog PLL).

When the M2050/51/52 is operating in wide bandwidth mode (NBW=0), the optional Hitless Switching function puts the device into narrow bandwidth mode when activated. This allows the PLL to lock the new input clock phase gradually. With proper configuration of the external loop filter, the output clock phase change complies with MTIE and TDEV specifications for GR-253 (SONET) and ITU G.813 (SDH) during input reference clock changes.

The optional proprietary Phase Build-out (PBO) function enables the PLL to absorb most of the phase change of the input clock during reference switching. The PBO function selects a new VCSO clock edge for the PLL Phase Detector feedback clock, selecting the edge closest in phase to the new input clock phase. This reduces re-lock time, the generation of wander, and extra output clock cycles.

The Hitless Switching and Phase Build-out functions are triggered by the LOL circuit. For proper operation, a low phase detector frequency must be avoided. See “Guidelines for Using LOL” on pg. 6 for information regarding the phase detector frequency.

HS/PBO Sequence Trigger Mechanism

The HS function (or the combined HS/PBO function) is armed after the device locks to the input clock reference. Once armed, HS is triggered by the occurance of a Loss of Lock condition. This would typically occur as a consequence of a clock reference failure, a clock failure upstream to the M2050/51/52, or a M2050/51/52 clock reference mux reselection.

HS/PBO Operation

Once triggered, the following HS/PBO sequence occurs:

1. The HS function disables the PLL Phase Detector and puts the device into NBW (narrow bandwidth) mode. The internal resistor Rin is changed to 2100kΩ. See the Narrow Bandwidth (NBW) Control Pin on pg. 6.
2. If included, the PBO function adds to (builds out) the phase in the clock feedback path (in VCSO clock cycle increments) to align the feedback clock with the (new) reference clock input phase.
3. The PLL Phase Detector is enabled, allowing the PLL to re-lock.
4. Once the PLL Phase Detector feedback and input clocks are locked to within 2 nsec for 8 consecutive cycles, a timer (WBW timer) for resuming wide bandwidth (in 175 nsec) is started.
5. When the WBW timer times out, the device reverts to wide loop bandwidth mode (i.e., Rin is returned to 100kΩ) and the HS/PBO function is re-armed.

The LOL pin will indicate lock status on a cycle-to-cycle basis and may be intermittent until PLL phase lock has fully stabilized.

External Loop Filter

To provide stable PLL operation, the M2050/51/52 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 5).

Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here.

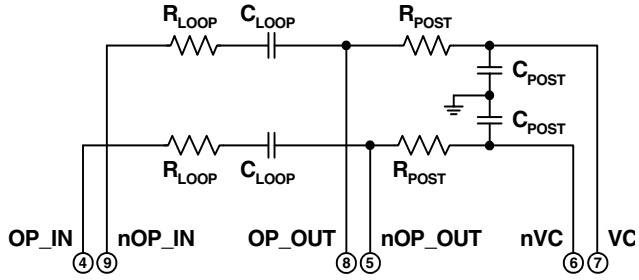


Figure 5: External Loop Filter

PLL bandwidth is affected by the "Mfec" value and the "Mfin" value, as well as the VCSO frequency. The FEC_SEL setting can be used to actively change PLL loop bandwidth in a given application. See "Mfec and Rfec Divider Look-Up Tables (LUTs)" on pg. 3.

See Tables 9, 10, and 11, Example External Loop Filter Component Values, on pg. 8.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

Refer to the M2050/51/52 product web page at www.icst.com/products/summary/m2050-2052.htm for additional product information.

Example External Loop Filter Component Values for M2050-11-644.5313 and M2050-11-669.6429

VCSO Parameters: K_{VCO} = 800kHz/V, R_{IN} = 100kΩ (pin NBW = 0), VCSO Bandwidth = 700kHz.

Device Configuration								Example Loop Filter Component Values				Nominal Performance With Values			
F Ref (MHz)	F VCSO (MHz)	FIN_ ... SEL1:0	FEC_	Mfin	M	R	Phase Det. Freq. (MHz)	R Loop	C Loop	R Post	C Post	PLL Loop Bandwidth	Damping Factor	Passband Peaking (dB)	Post Filter Bandwidth
125.00	644.5313	0 1	0 0	5	33	32	3.9063	61.9kΩ	1.0µF	59.0kΩ	1000pF	577Hz	6.8	0.043	2.7kHz
125.00	669.6429	0 1	1 0	5	15	14	8.9286	44.2kΩ	1.0µF	38.3kΩ	1000pF	908Hz	7.2	0.039	4.1kHz

Table 9: Example External Loop Filter Component Values for M2050-11-644.5313 and M2050-11-669.6429

Example External Loop Filter Component Values for M2051-11-625.0000

VCSO Parameters: K_{VCO} = 800kHz/V, R_{IN} = 100kΩ (pin NBW = 0), VCSO Bandwidth = 700kHz.

Device Configuration								Example Loop Filter Component Values				Nominal Performance With Values			
F Ref (MHz)	F VCSO (MHz)	FIN_ ...SEL1:0	FEC_	Mfin	M	R	Phase Det. Freq. (MHz)	R Loop	C Loop	R Post	C Post	PLL Loop Bandwidth	Damping Factor	Passband Peaking (dB)	Post Filter Bandwidth
644.5313	625.0000	1 1	0 0		32	33	19.5313	28.0kΩ	1.0µF	15.0kΩ	1000pF	1.25kHz	7.0	0.04	10.6kHz

Table 10: Example External Loop Filter Component Values for M2051-11-625.0000

Example External Loop Filter Component Values[1] for M2052-11-644.5313

VCSO Parameters: K_{VCO} = 800kHz/V, R_{IN} = 100kΩ (pin NBW = 0), VCSO Bandwidth = 700kHz.

Device Configuration								Example Loop Filter Component Values				Nominal Performance With Values			
F Ref (MHz)	F VCSO (MHz)	FIN_ ...SEL1:0	FEC_	Mfin	M	R	Phase Det. Freq. (MHz)	R Loop	C Loop	R Post	C Post	PLL Loop Bandwidth	Damping Factor	Passband Peaking (dB)	Post Filter Bandwidth
693.4830	644.5313	1 1	0 0	1	79	85	8.1586	51.0kΩ	1.0µF	33.2kΩ	1000pF	986Hz	8.1	0.031	4.8kHz

Table 11: Example External Loop Filter Component Values for M2052-11-644.5313

Note 1: K_{VCO} , VCSO Bandwidth, Mfin x Mfec Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking. For PLL Simulator software, go to www.icst.com.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 12: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature					
		Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 13: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = F_{OUT} = 622-675MHz, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V	
	I_{CC}	Power Supply Current			175	225	mA	
All Differential Inputs	V_{P-P}	Peak to Peak Input Voltage	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	0.15			V	
	V_{CMR}	Common Mode Input		0.5		V_{CC} - .85	V	
	C_{IN}	Input Capacitance				4	pF	
Differential Inputs with Pull-down	I_{IH}	Input High Current (Pull-down)	DIF_REF0, DIF_REF1			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current (Pull-down)		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistance			50		kΩ	
Differential Inputs Biased to VCC/2 [1]	I_{IH}	Input High Current (Biased) [1]	nDIF_REF0, nDIF_REF1			150	µA	V_{IN} = 0 to 3.456V
	I_{IL}	Input Low Current (Biased) [1]		-150			µA	
	R_{bias}	Biased to Vcc/2 [1]			(Note 1)		kΩ	
All LVCMOS / LVTTL Inputs	V_{IH}	Input High Voltage	REF_SEL, FIN_SEL1, FIN_SEL0, FEC_SEL1, FEC_SEL0, P_SEL2, P_SEL1, P_SEL0, NBW	2		V_{CC} + 0.3	V	
	V_{IL}	Input Low Voltage		-0.3		0.8	V	
	C_{IN}	Input Capacitance				4	pF	
LVCMOS / LVTTL Inputs with Pull-down	I_{IH}	Input High Current (Pull-down)	REF_SEL, FIN_SEL1, FIN_SEL0, FEC_SEL1, FEC_SEL0, P_SEL2, P_SEL1, P_SEL0			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current (Pull-down)		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistance			50		kΩ	
LVCMOS / LVTTL Inputs with Pull-UP	I_{IH}	Input High Current (Pull-UP)	NBW			5	µA	V_{CC} = 3.456V V_{IN} = 0 V
	I_{IL}	Input Low Current (Pull-UP)		-150			µA	
	R_{pullup}	Internal Pull-UP Resistance			50		kΩ	
Differential Outputs	V_{OH}	Output High Voltage	FOUT0, nFOUT0, FOUT1, nFOUT1	V_{CC} - 1.4		V_{CC} - 1.0	V	
	V_{OL}	Output Low Voltage		V_{CC} - 2.0		V_{CC} - 1.7	V	
	V_{P-P}	Peak to Peak Output Voltage [2]		0.4		0.85	V	
LVCMOS Output	V_{OH}	Output High Voltage	LOL	2.4		V_{CC}	V	I_{OH}= 1mA
	V_{OL}	Output Low Voltage		GND		0.4	V	I_{OL}= 1mA

Note 1: Biased to Vcc/2, with 50kΩ to Vcc and 50kΩ to ground. See Figure 4, Input Reference Clocks, on pg. 5
Note 2: Single-ended measurement. See Figure 6, Output Rise and Fall Time, on pg. 11.

Table 14: DC Characteristics

ELECTRICAL SPECIFICATIONS (CONTINUED)

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = F_{OUT} = 622-675MHz, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
	F_{IN}	Input Frequency	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	10		700	MHz	
	F_{OUT}	Output Frequency	FOUT0, nFOUT0, FOUT1, nFOUT1	15		700	MHz	
	APR	VCSO Absolute Pull-Range	Commercial	±120	±200		ppm	
			Industrial	±50	±150		ppm	
PLL Loop Constants [1]	K_{VCO}	VCO Gain			800		kHz/V	
	R_{IN}	Internal Loop Resistor	Wide Bandwidth		100		kΩ	
			Narrow Bandwidth		2100		kΩ	
	BW_{VCSO}	VCSO Bandwidth			700		kHz	
Phase Noise and Jitter	Φ n	Single Side Band Phase Noise @625.00MHz	1kHz Offset		-72		dBc/Hz	Fin=25.00 MHz Mfin=25, Mfec=Rfec
			10kHz Offset		-94		dBc/Hz	
			100kHz Offset		-123		dBc/Hz	
	J(t)	Jitter (rms) @625.00MHz	12kHz to 20MHz		0.25	0.5	ps	
			50kHz to 80MHz		0.25	0.5	ps	
	odc	Output Duty Cycle [2] FOUT0, nFOUT0, FOUT1, nFOUT1	P = 5 or 25	35	40	65	%	
			P = 1 or 4	40	50	60	%	
	t_R	Output Rise Time [2]	FOUT0, nFOUT0, FOUT1, nFOUT1	200	450	500	ps	20% to 80%
	t_F	Output Fall Time [2]		200	450	500	ps	20% to 80%

Table 15: AC Characteristics

Note 1: Parameters needed for PLL Simulator software; see Tables 9, 10, and 11, Example External Loop Filter Component Values, on pg. 8.
Note 2: See Parameter Measurement Information on pg. 11.

PARAMETER MEASUREMENT INFORMATION

Output Rise and Fall Time

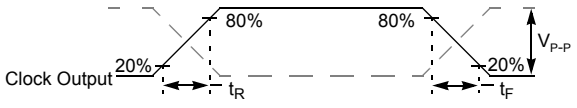


Figure 6: Output Rise and Fall Time

Output Duty Cycle

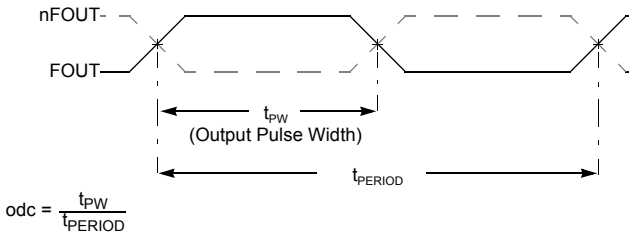


Figure 7: Output Duty Cycle

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:

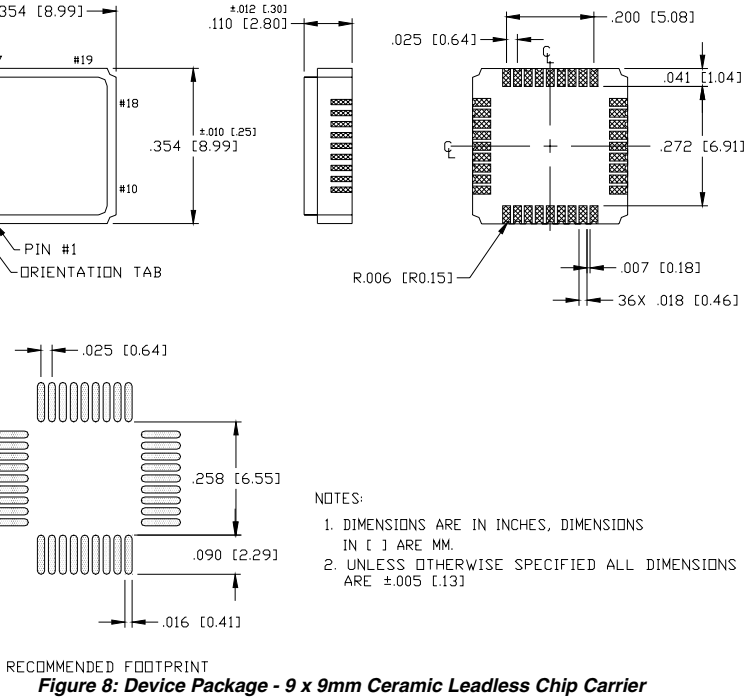


Figure 8: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

Part Numbering Scheme

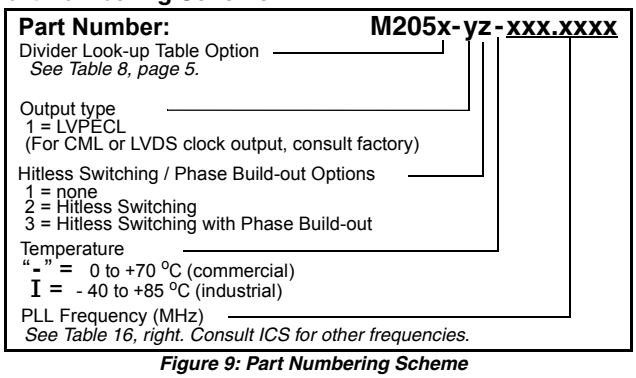


Figure 9: Part Numbering Scheme

Standard VCSO Output Frequencies (MHz)*

622.0800	669.3120
625.0000	669.3266
627.3296	669.6429
644.5313	670.8386
666.5143	672.1600
669.1281	690.5692

Table 16: Standard VCSO Output Frequencies

Note *: Fout can equal Fvcso divided by: 1, 4, 5, or 25.

Consult ICS for the availability of other PLL frequencies.

Example Part Numbers

VCSO Frequency (MHz)	Temperature	Order Part Number (Examples)
625.0000	commercial	**M2051-11-625.0000** or **M2052-11-625.0000**
	industrial	**M2051-11I625.0000** or **M2052-11I625.0000**
644.5313	commercial	**M2050-11-644.5313**
	industrial	**M2050-11I644.5313**

Table 17: Example Part Numbers