

M/A-COM X-Band Gain/Phase Control MMIC

8.0 –11.0 GHz

MA03501D

Features

- ◆ 8.0 to 11.0 GHz Operation
- ◆ 6-bit Phase Shifter and 5-bit Attenuator
- ◆ Serial Control Input
- ◆ 50 Ω Input and Output Impedance
- ◆ Self-Aligned MSAG[®] MESFET Process

Primary Applications

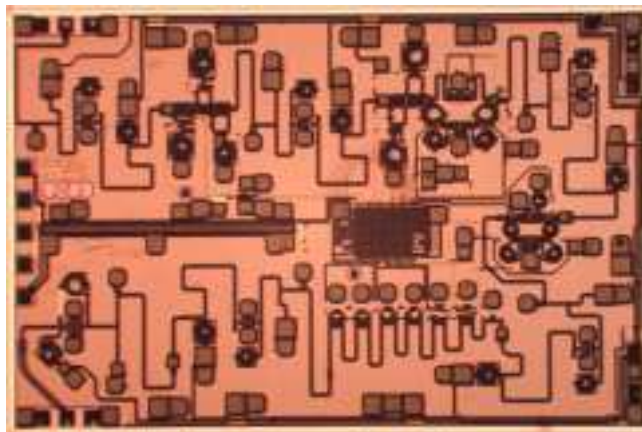
- ◆ Radar Systems

Description

The MA03501D is a serial control input phase shifter/attenuator/buffer amplifier MMIC. The on-chip serial to parallel converter circuitry allows for control of the 6 phase and 5 attenuation bits using a single TTL/CMOS compatible input. This product is fully matched to 50 ohms on both the input and output.

Each device is 100% RF tested on wafer to ensure performance compliance. The part is fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG[®]) MESFET Process.

8.0-11.0 GHz Serial Input Control MMIC



Electrical Characteristics: $T_B = 25^\circ\text{C}^1$, $Z_0 = 50\Omega$, $V_{DD} = 5\text{V}$, $V_{GG} = -4\text{V}$, $V_{EE} = -4.0$

Parameter	Symbol	Minimum	Typical	Maximum	Units
Bandwidth	f	8.0		11.0	GHz
Gain	Gn	13	18	22.5	dB
1-dB Compression Point	P1dB		21		dBm
Input Return Loss	IRL	10	16		dB
Output Return Loss	ORL	10	16		dB
Attenuation Range (5-bits, 0.75dB step)			23		dB
RMS Attenuation Error (Uncorrected)			0.2		dB
0.75 dB Attenuator Bit		0.5	0.8	1.0	dB
1.5 dB Attenuator Bit		1.0	1.5	2.0	dB
3 dB Attenuator Bit		2.4	3.0	3.6	dB
6 dB Attenuator Bit		5.0	6.0	7.0	dB
12 dB Attenuator Bit		10.8	12	13.2	dB

1. T_B = MMIC Base Temperature

Electrical Characteristics: $T_B = 25^\circ\text{C}$, $Z_0 = 50\Omega$, $V_{DD} = 5\text{V}$, $V_{GG} = -4\text{V}$, $V_{EE} = -4.0$

Parameter	Symbol	Minimum	Typical	Maximum	Units
Phase Shift Range (6 bits, 5.6 degree step)			354		Deg
RMS Phase Error (Uncorrected)			2		Deg
5.6 Degree Bit		4.0	5.3	7.0	Deg
11.25 Degree Bit		8.0	11.0	13.0	Deg
22.5 Degree Bit		19.0	22.0	24.0	Deg
45 Degree Bit		40.0	44.0	47.0	Deg
90 Degree Bit		85.0	90.0	95.0	Deg
180 Degree Bit		170	180	190	Deg
Gain Variation over all Phase Shifter settings			+/-1.0		dB
Output Third Order Intercept Point	OTOI		26		dBm
Noise Figure	NF		10		dB
Drain Supply Current	I_{DD}	160	275	500	mA
Gate Supply Current	I_{GG}		1	10	mA
Digital Power Supply Current	I_{EE}		10	20	mA
Input Logic High Current			0.5		mA
Input Logic Low Current			0.1		mA
Timing Delay-Enable Signal to Bit Change			25		nS

Absolute Maximum Conditions ¹

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	12	dBm
Drain Supply Voltage	V_{DD}	8.0	V
Gate Supply Voltage	V_{GG}	-6.0	V
Quiescent Drain Current (No RF)	I_{DQ}	500	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	2.5	W
Digital Power Supply Voltage	V_{EE}	-6.0	V
Junction Temperature	T_j	180	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to +150	$^\circ\text{C}$

1. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.

Specifications subject to change without notice.

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Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	V_{DD}	4.0	5.0	6.0	V
Gate Voltage	V_{GG}	-4.5	-4.0	-3.5	V
Digital Power Supply Voltage	V_{EE}	-4.2	-4.0	-3.8	V
Input Logic High Voltage	V_{IH}	3.0	3.5	5.0	V
Input Logic Low Voltage	V_{IL}	0.0	0.0	0.4	V
Clock Frequency	F_{CLK}		20		MHz
Junction Temperature	T_J			150	°C
MMIC Base Temperature	T_B			Note 2	°C

2. Maximum MMIC Base Temperature = $150^{\circ}\text{C} - 31.8^{\circ}\text{C/W} * V_{DD} * I_{DQ}$

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply $V_{GG} = -4\text{ V}$, $V_{EE} = -4\text{ V}$, $V_{DD} = 0\text{ V}$.
2. Ramp V_{DD} to desired voltage, typically 5 V.
3. Adjust V_{GG} to set I_{DQ} , (approximately @ -4 V).
4. Set RF input.
5. Power down in reverse. Turn gate voltage off last.



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Typical Small Signal Characteristics ($V_{DD}=5V$, $V_{GG}=-4V$)

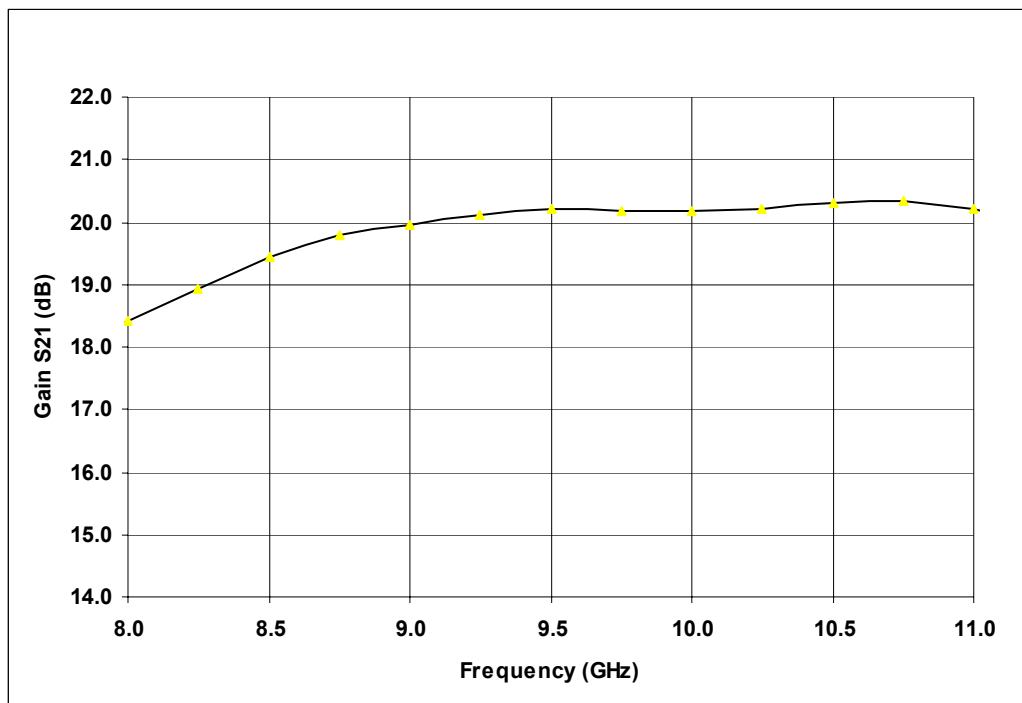


Figure 1. Gain

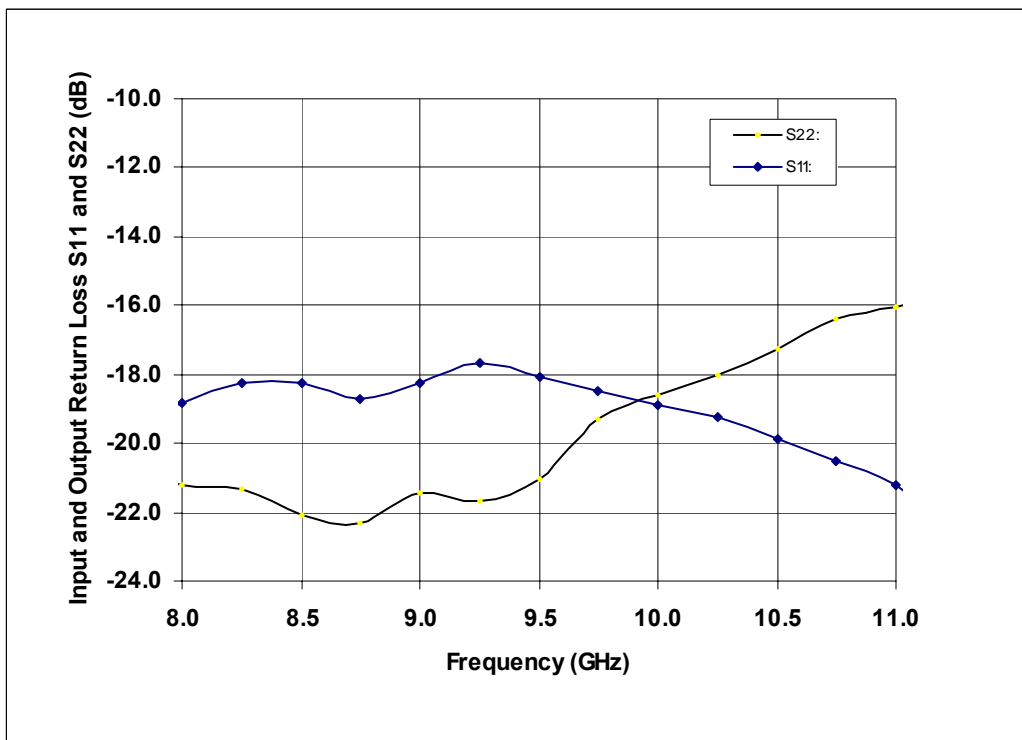


Figure 2. Input and Output Match

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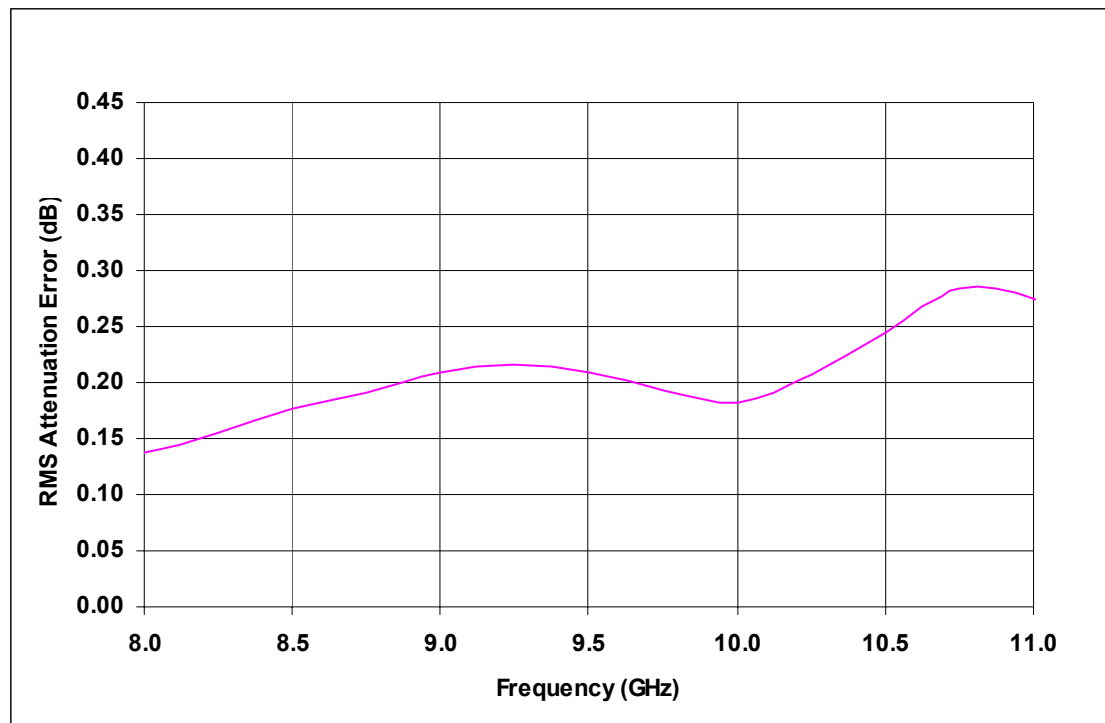


Figure 3. RMS Attenuation Error

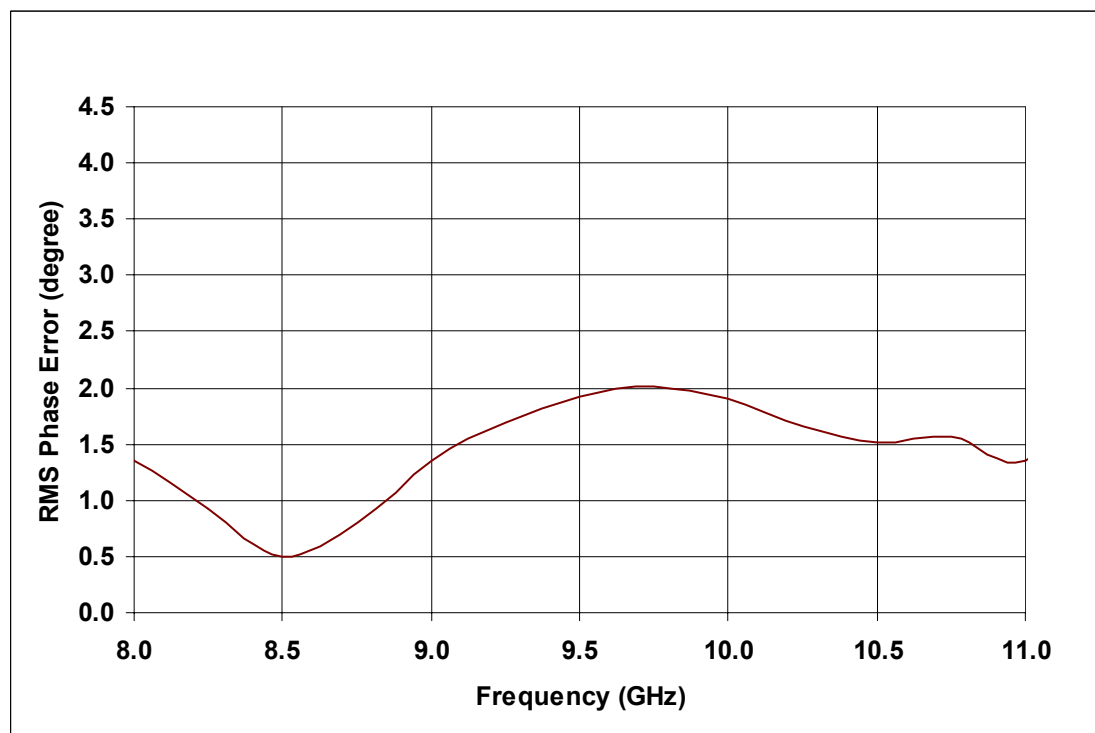


Figure 4. RMS Phase Error

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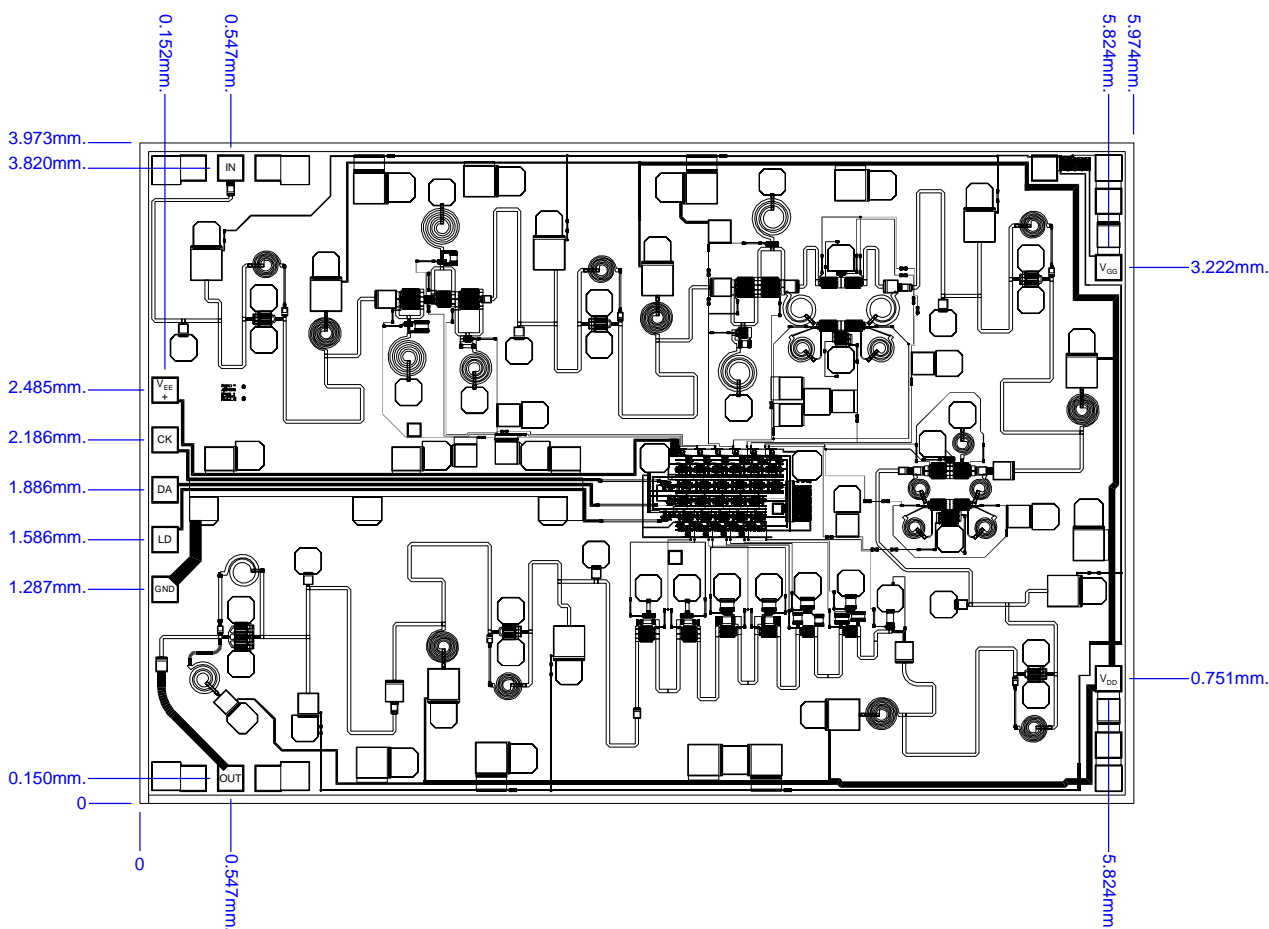
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Mechanical Information

Chip Size: 5.974 x 3.973 x 0.075 mm (236 x 157 x 3 mils)



Bond Pad Dimensions

Pad	Size (µm)	Size (mils)
RF In and Out	150 x 150	6 x 6
DC Supply Voltages	150 x 150	6 x 6
DC Control Voltages	150 x 150	6 x 6

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Assembly and Bonding Diagram

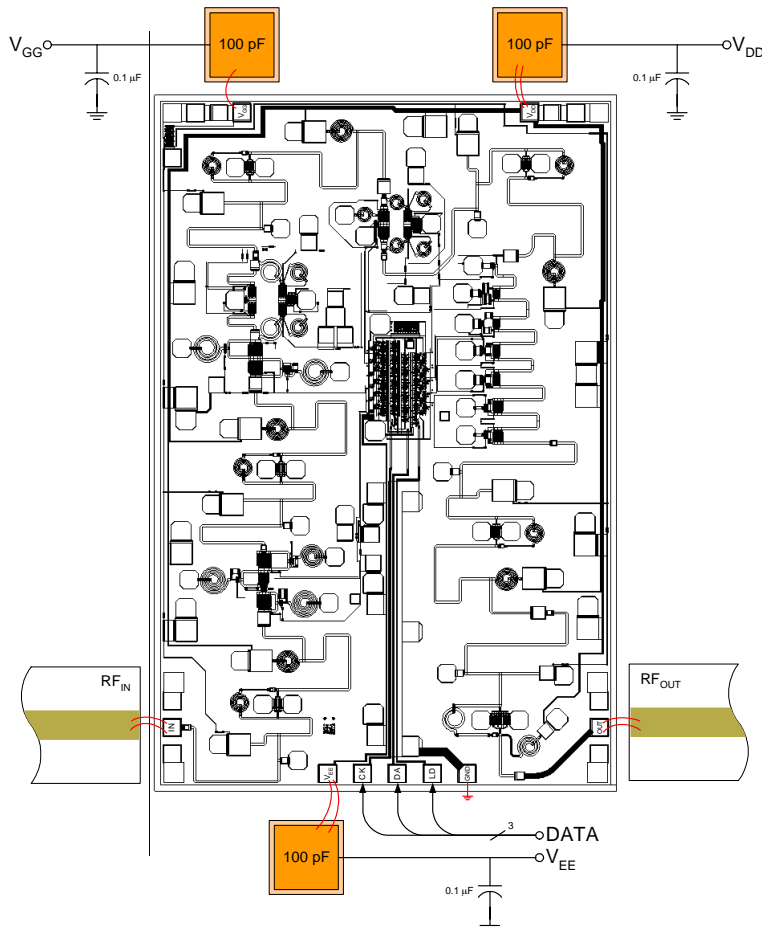


Figure 5. Recommended bonding diagram.
Support circuitry typical of MMIC characterization fixture for CW testing.



Assembly Instructions:

Die attach: Use AuSn (80/20) 1-2 mil. preform solder. Limit time @ 300°C to less than 5 minutes.

Wirebonding: Bond @ 160°C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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