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1. General Description

HE84761 is a member of 8-bit Micro-controller series developed by King Billion Electronics. There are 3 LCD configurations: 32COM x 96SEG, 48 COM x 80 SEG and 64 COM x 64 SEG available by mask option. 24 LCD segment driver pins are multiplexed with I/O pins to provide flexibility of wide variety of combinations to suit the needs of applications. The built-in LCD power supply is equipped with voltage charge pump to generate the high voltage required by the high duty LCD driver, bias voltage generating circuit and input voltage regulator circuit to supply stable LCD display effect over the wide battery life. The built-in OP comparator can be used with (light, voice, temperature, humility) sensor or battery low detection. Built-in two-channel sinusoidal wave generator can be used to generate telecom tones such as DTMF tone dialing signal, Caller Alerting Signal (CAS) tone, FSK signal as well other tones with frequencies ranging from 1 ~ 4095 Hz. A 7-bit current type D/A converter and PWM device provide the complete speech output mechanism. The 256K byte ROM and 4K byte RAM can be used as the storage of large speech data, graphic, text, etc. It is ideal for applications such as Translator, Data Bank, Educational Toy, Digital Voice Recording System, Short Message Service phone, etc.

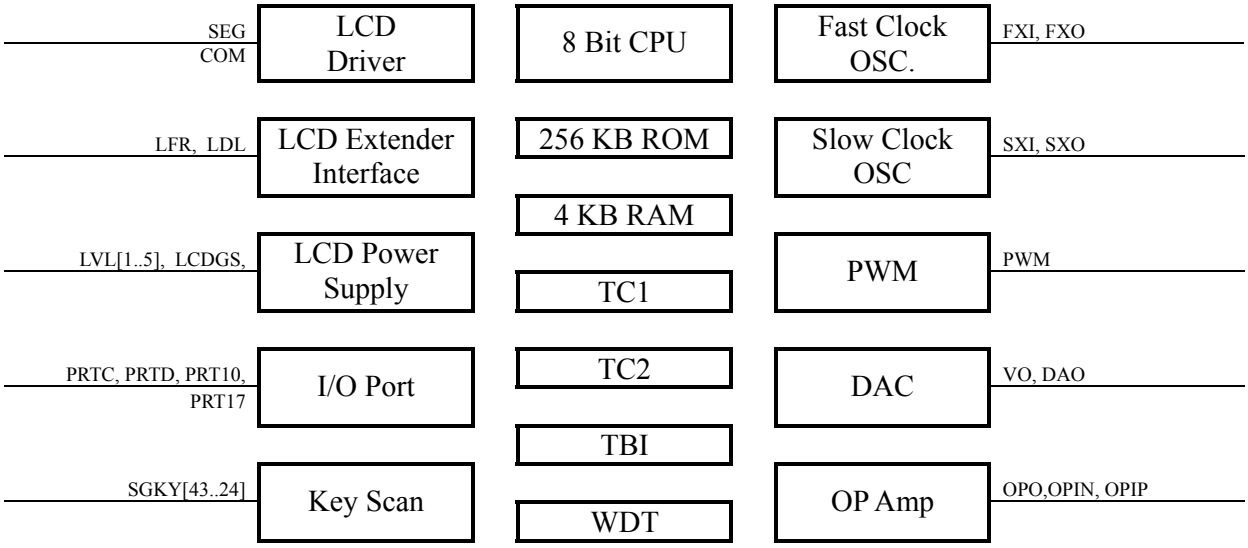
The instruction set of HE80000 series is easy to learn and simple to use. Only 32 instructions with four addressing modes are provided. Most of instructions take only 3 oscillator clocks to execute. The performance and low power consumption make it suitable for battery-powered applications such as translator, data bank, educational toy, digital voice recorder, etc.

2. Features

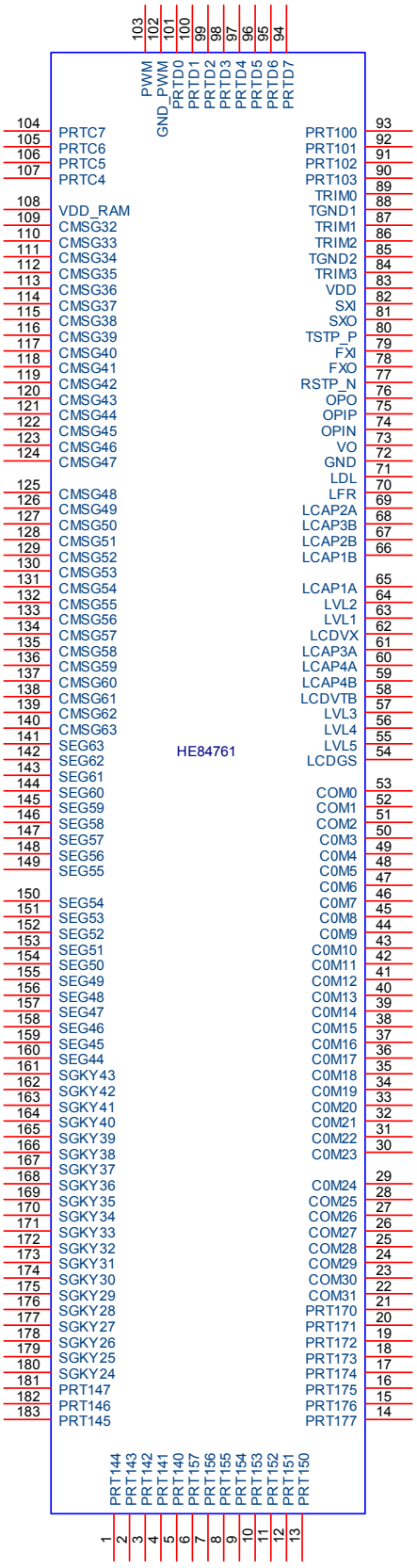
- ✓ Operation Voltage: 2.4V ~ 3.6V
- ✓ Internal ROM: 256 KB
- ✓ Internal RAM: 4 KB
- ✓ Dual Clock System: Fast clock: 32768 ~ 8M Hz
  Slow clock: 32768 Hz
- ✓ 4 operation modes: Fast, Slow, Idle, and Sleep modes.
- ✓ 16 ~ 40 bit bi-directional general purpose I/O ports with push-pull or open-drain output type selectable for each I/O pin by mask option.
- ✓ Built-in 4x20 hardware keyboard scan circuit (multiplexed with LCD SEG pin) helps to reduce the pin counts as well as the firmware effort.
- ✓ Three LCD configurations: 32COM x 96SEG, 48 COM x 80 SEG and 64 COM x 64 SEG.
- ✓ Built-in LCD power supply with input voltage regulator, voltage charge pump and bias voltage generating circuit.
- ✓ LCD Segment Extender Interface to connect with KDS80.
- ✓ One 7-bit current type D/A with mask option to select different output current to prevent signal saturation.
- ✓ Built-in RC oscillator, accuracy at ±5%, maximum frequency up to around 10 MHz
- ✓ Single-ended Pulse Width Modulation output for alternate voice output.
- ✓ Built-in OP comparator.
- ✓ Built-in Power on Reset circuit.
- ✓ Two external interrupts and three internal timer interrupts.
- ✓ Two 16-bit timers and one Time-Base timer.

- ✓ Watch Dog Timer to prevent deadlock condition.
- ✓ Instruction set: 32 instructions with 4 addressing modes.

3. Functional Block Diagram



4. Pin Description

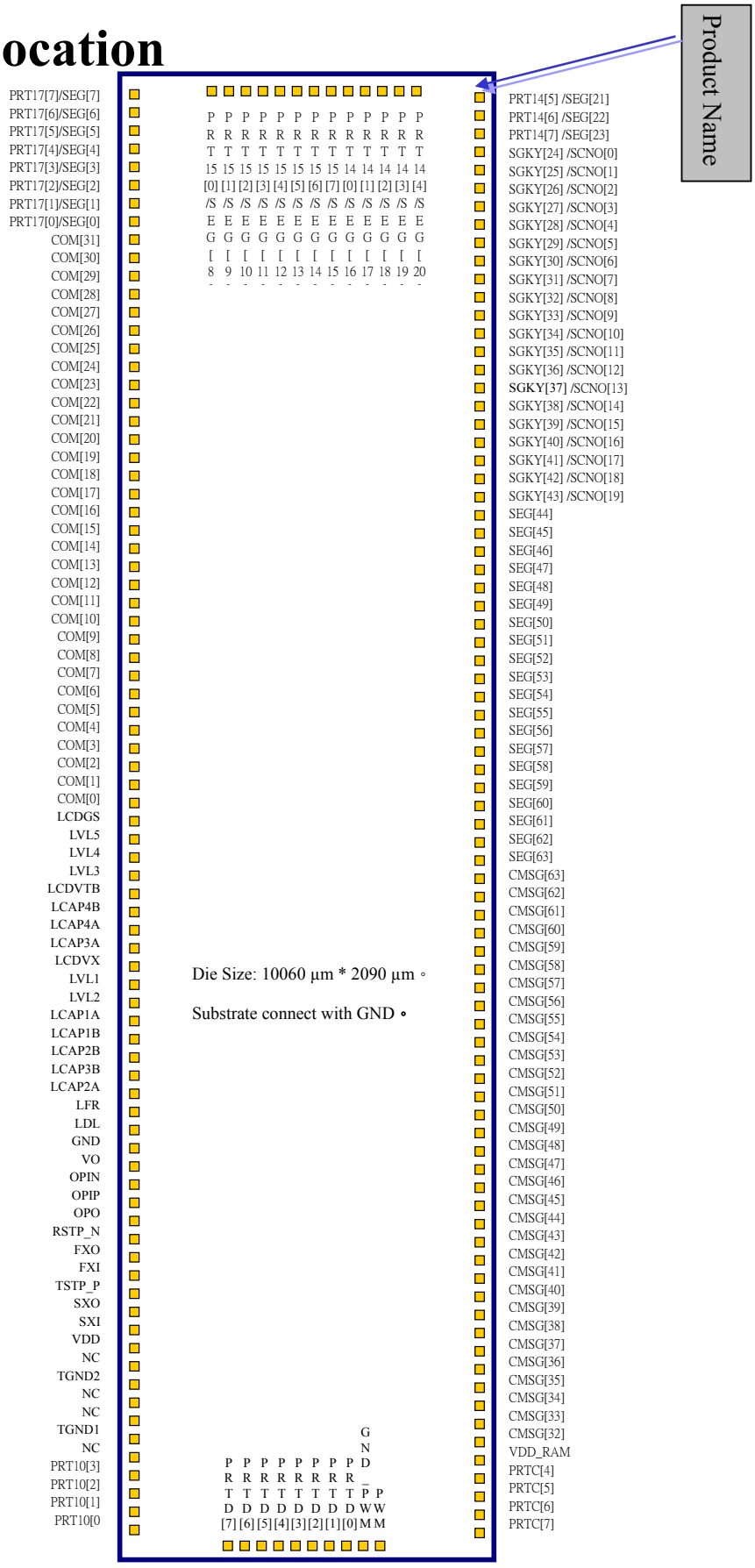


Pin Name	Pin #	I/O	Description
PRT14[7..0]	181~183, 1 ~ 5	B/O	8-bit bi-directional I/O port 14 is shared with LCD segment pads SEG[23..16]. The function of the pad can be selected individually by mask options MO_LIO14[7..0]. (‘1’ for LCD and ‘0’ for I/O). The output type of I/O pad can also be selected by mask option MO_14PP[7..0] (1 for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, “1” must be outputted before reading.
PRT15[7..0]	6 ~ 13	B/O	8-bit bi-directional I/O port 15 is shared with LCD segment pads SEG[16..8]. The function of the pad can be selected individually by mask options MO_LIO15[7..0]. (‘1’ for LCD and ‘0’ for I/O). The output type of I/O pad can also be selected by mask option MO_15PP[7..0] (1 for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, “1” must be outputted before reading.
PRT17[7..0]	14 ~ 21	B/O	8-bit bi-directional I/O port 17 is shared with LCD segment pads SEG[7..0]. The function of the pad can be selected individually by mask options MO_LIO17[7..0]. (‘1’ for LCD and ‘0’ for I/O). The output type of I/O pad can also be selected by mask option MO_17PP[7..0] (1 for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, “1” must be outputted before reading.
COM[31..0]	22~53	O	LCD COMMON Driver pads.
LCDGS	54	B	LCD Voltage setting. Adjust Resistor between LCDGS and LVL2 to set LVL5.
LVL5	55	B	LCD Bias Voltage 5
LVL4	56	B	LCD Bias Voltage 4
LVL3	57	B	LCD Bias Voltage 3
LCDVTB	58	B	Charge Pump Capacitor Pin
LCAP4B	59	B	Charge Pump Capacitor Pin.
LCAP4A	60	B	Charge Pump Capacitor Pin
LCAP3A	61	B	Charge Pump Capacitor Pin
LCDVX	62	B	Charge Pump Capacitor Pin
LVL1	63	B	LCD Bias Voltage 1
LVL2	64	B	LCD Bias Voltage 2
LCAP1A	65	B	Charge Pump Capacitor Pin
LCAP1B	66	B	Charge Pump Capacitor Pin
LCAP2B	67	B	Charge Pump Capacitor Pin
LCAP3B	68	B	Charge Pump Capacitor Pin
LCAP2A	69	B	Charge Pump Capacitor Pin
LFR	70	O	LCD frame signal for interfacing with LCD segment extender KDS80.
LDL	71	O	LCD data load pin for interfacing with LCD segment extender KDS80.
GND	72	P	Power ground Input.
VO	73	O	DAC Output.
OPIN	74	I	Inverting input of OP Amp. Set the bit 0 (OP = 1) of VOC register to turn on OP comparator.
OPIP	75	I	Non-inverting input of OP Amp.
OPO	76	O	Output of OP Amp.
RSTP_N	77	I	System Reset input pin. Level trigger, active low on this pin will put the chip in reset state.
FXO, FXI	78, 79	O, B	External fast clock pin. Two types of oscillator can be selected by MO_FXTAL (‘0’ for RC type and ‘1’ for crystal type). For RC type oscillator, one resistor needs to be connected between FXI and GND. For crystal oscillator, one crystal needs to be placed between FXI and FXO. Please refer to application circuit for details.

Pin Name	Pin #	I/O	Description
TSTP_P	80	I	Test input pin. Please bond this pad and reserve a test point on PCB for debugging. But for improving ESD, please connect this point with zero Ohm resistor to GND.
SXO, SXI	81, 82	O, I	External slow clock pins. Slow clock is clock source for LCD display, TIMER1, Time-Base and other internal blocks. Both crystal and RC oscillator are provided. The slow clock type can be selected by mask option MO_SXTAL. Choose '0' for RC type and '1' for crystal oscillator.
VDD	83	P	Positive power Input. 0.1 µF decoupling capacitors should be placed as close to IC VDD and GND pads as possible for best decoupling effect.
TGND2	85	P	Power Ground Input. The TGND2 should connect with GND pin.
TGND1	88	P	Power Ground Input. The TGND1 should connect with GND pin.
PRT10[3:0]	90~93	B	4-bit bi-directional I/O port 10. The output type of I/O pad can also be selected by mask option MO_10PP[3..0] ('1' for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O pad as input pad, "1" must be outputted before reading. PRT10[0] is shared with DTMFO of DTMF generator. PRT10[1] is multiplexed with KEYTONE output.
PRTD[7..0]	94~101	B	8-bit bi-directional I/O port D. The output type of I/O pad can also be selected by mask option MO_DPP[7..0] ('1' for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, '1' must be outputted before reading the pin. PRTD[7..2] can be used as wake-up pins. PRTD[7..6] can be as external interrupt sources.
GND_PWM	102	O	Dedicated Ground for PWM output.
PWM	103	O	The PWM output can drive speaker or buzzer directly. Set the bit2 of VOC register as one to turn on PWM. Using VDD & PWM to drive output device.
PRTC[7:4]	104~107	B	8-bit bi-directional I/O port C. The output type of I/O pad can also be selected by mask option MO_CPP[7..0] ('1' for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, '1' must be outputted before reading the pin. PRTC[7:4] is shared with Key Scan Dedicated Input SCNI[3:0]. The Key Scan function can be disabled by clearing MO_LCDKEY mask option to '0'.
VDD_RAM	108	P	Dedicated power input for RAM
CMSG[32..63]	109~140	O	COM[32..63] pads are shared with SEG[95..64] outputs. The functions of the pads to be COM drivers or SEG drivers can be selected by mask option MO_COM[1..0]. Please refer to LCD driver configuration for details.
SEG[63..44]	141~160	O	LCD segment SEG[63..44] outputs.
SGKY[43..24]	161~180	O	LCD segments share pads with key scan out SCNO[19..0]. The key scan function of these pins can be disabled by mask option clearing MO_LCDKEY to '0', then SGKY[43..24] function as LCD segment driver only. Setting MO_LCDKEY to '1' will turn on the key scan function.

I: Input, O: Output, B: Bidirectional, P: Power.

5. Pad Location



PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	PRT14[4]	X= -5005.80	Y= 667.00	93	PRT10[0]	X= 4799.90	Y= -970.45
2	PRT14[3]	X= -5005.80	Y= 552.00	94	PRTD[7]	X= 4904.30	Y= -568.35
3	PRT14[2]	X= -5005.80	Y= 437.00	95	PRTD[6]	X= 4904.30	Y= -453.35
4	PRT14[1]	X= -5005.80	Y= 322.00	96	PRTD[5]	X= 4904.30	Y= -338.35
5	PRT14[0]	X= -5005.80	Y= 207.00	97	PRTD[4]	X= 4904.30	Y= -223.35
6	PRT15[7]	X= -5005.80	Y= 92.00	98	PRTD[3]	X= 4904.30	Y= -108.35
7	PRT15[6]	X= -5005.80	Y= -23.00	99	PRTD[2]	X= 4904.30	Y= 6.65
8	PRT15[5]	X= -5005.80	Y= -138.00	100	PRTD[1]	X= 4904.30	Y= 121.65
9	PRT15[4]	X= -5005.80	Y= -253.00	101	PRTD[0]	X= 4904.30	Y= 236.65
10	PRT15[3]	X= -5005.80	Y= -368.00	102	GND_PWM	X= 4904.30	Y= 351.65
11	PRT15[2]	X= -5005.80	Y= -483.00	103	PWM	X= 4904.30	Y= 466.66
12	PRT15[1]	X= -5005.80	Y= -598.00	104	PRTC[7]	X= 4737.30	Y= 969.25
13	PRT15[0]	X= -5005.80	Y= -713.00	105	PRTC[6]	X= 4622.30	Y= 969.25
14	PRT17[7]	X= -4635.10	Y= -970.45	106	PRTC[5]	X= 4507.30	Y= 969.25
15	PRT17[6]	X= -4520.10	Y= -970.45	107	PRTC[4]	X= 4392.30	Y= 969.25
16	PRT17[5]	X= -4405.10	Y= -970.45	108	VDD_RAM	X= 4177.30	Y= 969.25
17	PRT17[4]	X= -4290.10	Y= -970.45	109	CMSG[32]	X= 4062.31	Y= 969.25
18	PRT17[3]	X= -4175.10	Y= -970.45	110	CMSG[33]	X= 3947.30	Y= 969.25
19	PRT17[2]	X= -4060.10	Y= -970.45	111	CMSG[34]	X= 3832.30	Y= 969.25
20	PRT17[1]	X= -3945.10	Y= -970.45	112	CMSG[35]	X= 3717.30	Y= 969.25
21	PRT17[0]	X= -3830.10	Y= -970.45	113	CMSG[36]	X= 3602.30	Y= 969.25
22	COM[31]	X= -3715.10	Y= -970.45	114	CMSG[37]	X= 3487.30	Y= 969.25
23	COM[30]	X= -3600.10	Y= -970.45	115	CMSG[38]	X= 3372.30	Y= 969.25
24	COM[29]	X= -3485.10	Y= -970.45	116	CMSG[39]	X= 3257.30	Y= 969.25
25	COM[28]	X= -3370.10	Y= -970.45	117	CMSG[40]	X= 3142.30	Y= 969.25
26	COM[27]	X= -3255.10	Y= -970.45	118	CMSG[41]	X= 3027.30	Y= 969.25
27	COM[26]	X= -3140.10	Y= -970.45	119	CMSG[42]	X= 2912.30	Y= 969.25
28	COM[25]	X= -3025.10	Y= -970.45	120	CMSG[43]	X= 2797.30	Y= 969.25
29	COM[24]	X= -2910.10	Y= -970.45	121	CMSG[44]	X= 2682.30	Y= 969.25
30	COM[23]	X= -2695.10	Y= -970.45	122	CMSG[45]	X= 2567.30	Y= 969.25
31	COM[22]	X= -2580.10	Y= -970.45	123	CMSG[46]	X= 2452.30	Y= 969.25
32	COM[21]	X= -2465.10	Y= -970.45	124	CMSG[47]	X= 2337.30	Y= 969.25
33	COM[20]	X= -2350.10	Y= -970.45	125	CMSG[48]	X= 2122.30	Y= 969.25
34	COM[19]	X= -2235.10	Y= -970.45	126	CMSG[49]	X= 2007.30	Y= 969.25
35	COM[18]	X= -2120.10	Y= -970.45	127	CMSG[50]	X= 1892.30	Y= 969.25
36	COM[17]	X= -2005.10	Y= -970.45	128	CMSG[51]	X= 1777.30	Y= 969.25
37	COM[16]	X= -1890.10	Y= -970.45	129	CMSG[52]	X= 1662.30	Y= 969.25
38	COM[15]	X= -1775.10	Y= -970.45	130	CMSG[53]	X= 1547.31	Y= 969.25
39	COM[14]	X= -1660.10	Y= -970.45	131	CMSG[54]	X= 1432.30	Y= 969.25
40	COM[13]	X= -1545.10	Y= -970.45	132	CMSG[55]	X= 1317.30	Y= 969.25
41	COM[12]	X= -1430.10	Y= -970.45	133	CMSG[56]	X= 1202.30	Y= 969.25
42	COM[11]	X= -1315.10	Y= -970.45	134	CMSG[57]	X= 1087.30	Y= 969.25
43	COM[10]	X= -1200.10	Y= -970.45	135	CMSG[58]	X= 972.30	Y= 969.25
44	COM[9]	X= -1085.10	Y= -970.45	136	CMSG[59]	X= 857.30	Y= 969.25
45	COM[8]	X= -970.10	Y= -970.45	137	CMSG[60]	X= 742.30	Y= 969.25

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
46	COM[7]	X= -855.10	Y= -970.45	138	CMSG[61]	X= 627.30	Y= 969.25
47	COM[6]	X= -740.10	Y= -970.45	139	CMSG[62]	X= 512.30	Y= 969.25
48	COM[5]	X= -625.10	Y= -970.45	140	CMSG[63]	X= 397.30	Y= 969.25
49	COM[4]	X= -510.10	Y= -970.45	141	SEG[63]	X= 282.30	Y= 969.25
50	COM[3]	X= -395.10	Y= -970.45	142	SEG[62]	X= 167.30	Y= 969.25
51	COM[2]	X= -280.10	Y= -970.45	143	SEG[61]	X= 52.30	Y= 969.25
52	COM[1]	X= -165.10	Y= -970.45	144	SEG[60]	X= -62.70	Y= 969.25
53	COM[0]	X= -50.10	Y= -970.45	145	SEG[59]	X= -177.70	Y= 969.25
54	LCDGS	X= 165.35	Y= -969.70	146	SEG[58]	X= -292.70	Y= 969.25
55	LVL5	X= 280.35	Y= -969.70	147	SEG[57]	X= -407.70	Y= 969.25
56	LVL4	X= 395.35	Y= -969.70	148	SEG[56]	X= -522.70	Y= 969.25
57	LVL3	X= 510.35	Y= -969.70	149	SEG[55]	X= -637.70	Y= 969.25
58	LCDVTB	X= 625.35	Y= -969.70	150	SEG[54]	X= -852.69	Y= 969.25
59	LCAP4B	X= 740.35	Y= -969.70	151	SEG[53]	X= -967.69	Y= 969.25
60	LCAP4A	X= 855.35	Y= -969.70	152	SEG[52]	X= -1082.69	Y= 969.25
61	LCAP3A	X= 970.35	Y= -969.70	153	SEG[51]	X= -1197.69	Y= 969.25
62	LCDVX	X= 1085.35	Y= -969.70	154	SEG[50]	X= -1312.69	Y= 969.25
63	LVL1	X= 1200.35	Y= -969.70	155	SEG[49]	X= -1427.69	Y= 969.25
64	LVL2	X= 1315.35	Y= -969.70	156	SEG[48]	X= -1542.69	Y= 969.25
65	LCAP1A	X= 1430.35	Y= -969.70	157	SEG[47]	X= -1657.69	Y= 969.25
66	LCAP1B	X= 1695.35	Y= -969.70	158	SEG[46]	X= -1772.69	Y= 969.25
67	LCAP2B	X= 1810.35	Y= -969.70	159	SEG[45]	X= -1887.69	Y= 969.25
68	LCAP3B	X= 1925.35	Y= -969.70	160	SEG[44]	X= -2002.69	Y= 969.25
69	LCAP2A	X= 2040.35	Y= -969.70	161	SGKY[43]	X= -2117.69	Y= 969.25
70	LFR	X= 2154.90	Y= -970.45	162	SGKY[42]	X= -2232.69	Y= 969.25
71	LDL	X= 2269.90	Y= -970.45	163	SGKY[41]	X= -2347.69	Y= 969.25
72	GND	X= 2384.90	Y= -970.45	164	SGKY[40]	X= -2462.69	Y= 969.25
73	VO	X= 2499.90	Y= -970.45	165	SGKY[39]	X= -2577.69	Y= 969.25
74	OPIN	X= 2614.90	Y= -970.45	166	SGKY[38]	X= -2692.69	Y= 969.25
75	OPIP	X= 2729.90	Y= -970.45	167	SGKY[37]	X= -2807.69	Y= 969.25
76	OPO	X= 2844.90	Y= -970.45	168	SGKY[36]	X= -2922.69	Y= 969.25
77	RSTP_N	X= 2959.90	Y= -970.45	169	SGKY[35]	X= -3037.69	Y= 969.25
78	FXO	X= 3074.90	Y= -970.45	170	SGKY[34]	X= -3152.69	Y= 969.25
79	FXI	X= 3189.90	Y= -970.45	171	SGKY[33]	X= -3267.69	Y= 969.25
80	TSTP_P	X= 3304.90	Y= -970.45	172	SGKY[32]	X= -3382.69	Y= 969.25
81	SXO	X= 3419.90	Y= -970.45	173	SGKY[31]	X= -3497.69	Y= 969.25
82	SXI	X= 3534.90	Y= -970.45	174	SGKY[30]	X= -3612.69	Y= 969.25
83	VDD	X= 3649.90	Y= -970.45	175	SGKY[29]	X= -3727.69	Y= 969.25
84	NC	X= 3764.90	Y= -970.45	176	SGKY[28]	X= -3842.69	Y= 969.25
85	TGND2	X= 3879.90	Y= -970.45	177	SGKY[27]	X= -3957.69	Y= 969.25
86	NC	X= 3994.90	Y= -970.45	178	SGKY[26]	X= -4072.69	Y= 969.25
87	NC	X= 4109.90	Y= -970.45	179	SGKY[25]	X= -4187.69	Y= 969.25
88	TGND1	X= 4224.90	Y= -970.45	180	SGKY[24]	X= -4302.69	Y= 969.25
89	NC	X= 4339.90	Y= -970.45	181	PRT14[7]	X= -4417.69	Y= 969.25
90	PRT10[3]	X= 4454.90	Y= -970.45	182	PRT14[6]	X= -4532.69	Y= 969.25
91	PRT10[2]	X= 4569.90	Y= -970.45	183	PRT14[5]	X= -4647.69	Y= 969.25

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
92	PRT10[1]	X= 4684.90	Y= -970.45				

6. LCD RAM Map

There are 3 LCD configurations as determined by mask option MO_COM. The RAM Maps of all four different LCD configurations are as the following: The functions of CMSG[79..32] are different in each configuration as listed in the following table.

MO_COM[1:0]	Configuration	CMSG[63..48]	CMSG[47..32]
00	32 x 96	SEG[64..79]	SEG[80..96]
01	48 x 80	SEG[64..79]	COM[47..32]
10	64 x 64	COM[63..48]	COM[47..32]
11	reserved	reserved	reserved

COMXSEG	32X96	48X80	64X64
CMSG32	SEG95	COM32	COM32
CMSG33	SEG94	COM33	COM33
CMSG34	SEG93	COM34	COM34
CMSG35	SEG92	COM35	COM35
CMSG36	SEG91	COM36	COM36
CMSG37	SEG90	COM37	COM37
CMSG38	SEG89	COM38	COM38
CMSG39	SEG88	COM39	COM39
CMSG40	SEG87	COM40	COM40
CMSG41	SEG86	COM41	COM41
CMSG42	SEG85	COM42	COM42
CMSG43	SEG84	COM43	COM43
CMSG44	SEG83	COM44	COM44
CMSG45	SEG82	COM45	COM45
CMSG46	SEG81	COM46	COM46
CMSG47	SEG80	COM47	COM47
CMSG48	SEG79	SEG79	COM48
CMSG49	SEG78	SEG78	COM49
CMSG50	SEG77	SEG77	COM50
CMSG51	SEG76	SEG76	COM51
CMSG52	SEG75	SEG75	COM52
CMSG53	SEG74	SEG74	COM53
CMSG54	SEG73	SEG73	COM54
CMSG55	SEG72	SEG72	COM55
CMSG56	SEG71	SEG71	COM56
CMSG57	SEG70	SEG70	COM57
CMSG58	SEG69	SEG69	COM58
CMSG59	SEG68	SEG68	COM59
CMSG60	SEG67	SEG67	COM60
CMSG61	SEG66	SEG66	COM61
CMSG62	SEG65	SEG65	COM62
CMSG63	SEG64	SEG64	COM63

32 COM：

Page 7,6	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]	SEG [71:64]	SEG [79:72]	SEG [87:80]	SEG [95:88]
COM0	7E0H	7C0H	7A0H	780H	760H	740H	720H	700H	6E0H	6C0H	6A0H	680H
COM1	7E1H	7C1H	7A1H	781H	761H	741H	721H	701H	6E1H	6C1H	6A1H	681H
:	:	:	:	:	:	:	:	:	:	:	:	:
COM15	7EFH	7CFH	7AFH	78FH	76FH	74FH	72FH	70FH	6EFH	6CFH	6AFH	68FH
COM16	7F0H	7D0H	7B0H	790H	770H	750H	730H	710H	6F0H	6D0H	6B0H	690H
:	:	:	:	:	:	:	:	:	:	:	:	:
COM30	7FEH	7DEH	7BEH	79EH	77EH	75EH	73EH	71EH	6FEH	6DEH	6BEH	69EH
COM31	7FFH	7DFH	7BFH	79FH	77FH	75FH	73FH	71FH	6FFH	6DFH	6BFH	69FH

48 COM：

Page 7,6	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]	SEG [71:64]	SEG [79:72]
COM0	7C0H	780H	740H	700H	6C0H	680H	640H	600H	5C0H	580H
COM1	7C1H	781H	741H	701H	6C1H	681H	641h	601H	5C1H	581H
:	:	:	:	:	:	:	:	:	:	:
COM15	7CFH	78FH	74FH	70FH	6CFH	68FH	64FH	60FH	5CFH	58FH
COM16	7D0H	790H	750H	710H	6D0H	690H	650H	610H	5D0H	590H
:	:	:	:	:	:	:	:	:	:	:
COM31	7DFH	79FH	75FH	71FH	6DFH	69FH	65FH	61FH	5DFH	59FH
COM32	7E0H	7A0H	760H	720H	6E0H	6A0H	660H	620H	5E0H	5A0H
:	:	:	:	:	:	:	:	:	:	:
COM46	7EEH	7AEH	76EH	72EH	6EEH	6AEH	66EH	62EH	5EEH	5AEH
COM47	7EFH	7AFH	76FH	72FH	6EFH	6AFH	66FH	62FH	5EFH	5AFH

64 COM：

Page 7	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	Page 6	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]
COM0	7C0H	780H	740H	700H	COM0	6C0H	680H	640H	600H
COM1	7C1H	781H	741H	701H	COM1	6C1H	681H	641H	601H
:	:	:	:	:	:	:	:	:	:
COM15	7CFH	78FH	74FH	70FH	COM15	6CFH	68FH	64FH	60FH
COM16	7D0H	790H	750H	710H	COM16	6D0H	690H	650H	610H
:	:	:	:	:	:	:	:	:	:
COM31	7DFH	79FH	75FH	71FH	COM31	6DFH	69FH	65FH	61FH
COM32	7E0H	7A0H	760H	720H	COM32	6E0H	6A0H	660H	620H
:	:	:	:	:	:	:	:	:	:
COM47	7EFH	7AFH	76FH	72FH	COM47	6EFH	6AFH	66FH	62FH
COM48	7F0H	7B0H	770H	730H	COM48	6F0H	6B0H	670H	630H
:	:	:	:	:	:	:	:	:	:
COM62	7FEH	7BEH	77EH	73EH	COM62	6FEH	6BEH	67EH	63EH
COM63	7FFH	7BFH	77FH	73FH	COM63	6FFH	6BFH	67FH	63FH

7. LCD Power Supply

The built-in LCD power supply is equipped with input voltage regulator, voltage charge pump and bias voltage generating circuit with active buffer instead of passive resistor voltage dividing network. The input voltage is regulated to LVL2 using the internally generated reference voltage. LVL2 can be adjusted by resistor between LCDGS and LVL2.

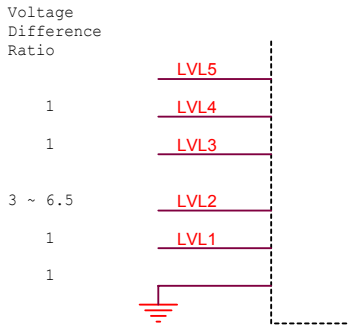
LVL2 adjustment guideline: First, the level of VDD must be 0.3 volt higher than LVL2 even at the end of battery life for the regulator to function properly. For example, if the VDD is expected to drop to 2.2 volts

when battery is low, then the level of LVL2 can only be set at 1.9 volts max.

Voltage charge pump: The LVL2 is then pumped to LVL5 based on the bias setting of MO_LBSR[3..0]. The formula for LVL5 is:

LVL5 = LVL2 / 2 x (1/Bias)

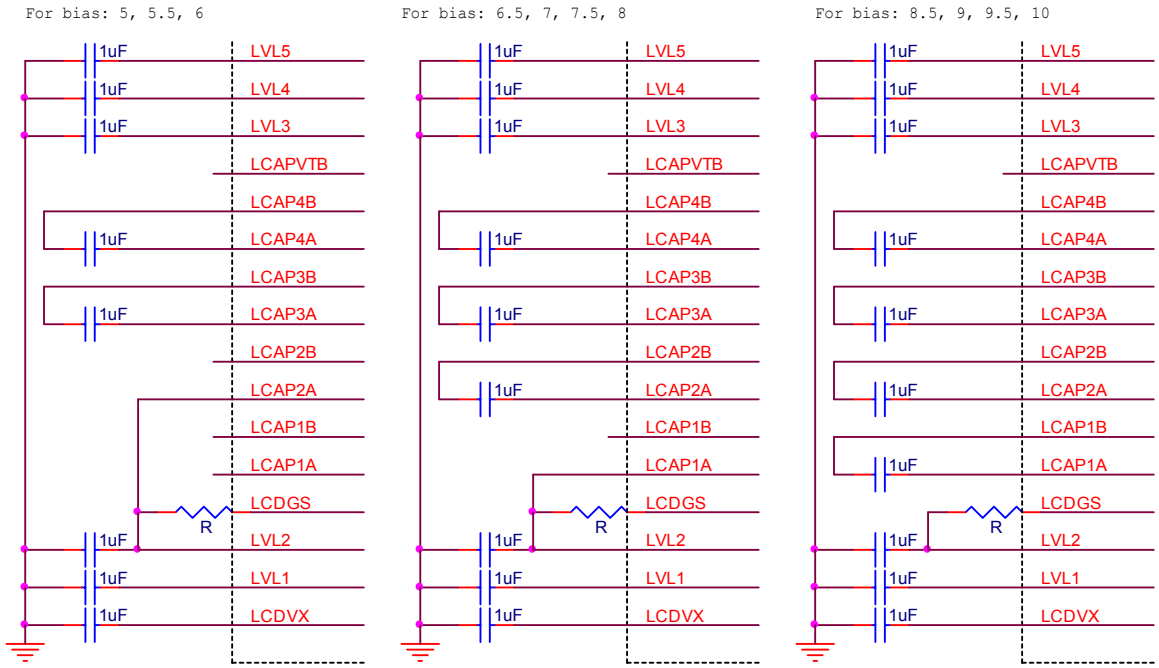
The potential difference between bias voltages LVL1 ~ LVL5 is determined by the bias settings, too.



For example, if the bias setting is 1/7 bias and LVL2 is 2 volts, the LVL5 will be pumped to 7 volts when the load is light.

	Bias	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0
Min. VDD	LVL2	LVL5 = LCD Panel Operating Voltage										
2.70	2.40	6.00	6.60	7.20	7.80	8.40						
2.60	2.30	5.75	6.33	6.90	7.48	8.05						
2.50	2.20	5.50	6.05	6.60	7.15	7.70	8.25					
2.40	2.10	5.25	5.78	6.30	6.83	7.35	7.88	8.40				
2.30	2.00	5.00	5.50	6.00	6.50	7.00	7.50	8.00	8.50			
2.20	1.90	4.75	5.23	5.70	6.18	6.65	7.13	7.60	8.08	8.55		
2.10	1.80	4.50	4.95	5.40	5.85	6.30	6.75	7.20	7.65	8.10	8.55	
2.00	1.70	4.25	4.68	5.10	5.53	5.95	6.38	6.80	7.23	7.65	8.08	8.5

Please note that external connections of charge pump capacitors must be made according to the bias setting, too. Please use the following figure as reference when designing application circuit and LVL5 must be lower than 8.5 volts to prevent chip from breaking down.



Different duties require different bias settings. There is some reference correspondence between the Duty and Bias Setting. However, it is better to use it as starting point and adjust it with real LCD panel connected to it to determine the final setting. The relationship between the duty and bias setting is just for reference as following:

Duty Cycle	Normal Bias	Alternative Bias
32 duty	1/7	1/7.5
48 duty	1/8	1/7.5, 1/8.5
64 duty	1/9	1/8.5, 1/9.5

The bias setting is made by mask option MO_LBSR[3..0].

MO_LBSR[3:0]	Bias Setting
0000	undefined
0001	1/5
0010	1/5.5
0011	1/6
0100	1/6.5
0101	1/7
0110	1/7.5
0111	1/8
1000	1/8.5
1001	1/9
1010	1/9.5
1011	1/10
1100	1/10.5
1101	1/11
1110	1/11.5

1111	1/12

7.1. LCDC Control register

The gray scale of the LCD driver can be adjusted by GRAY field of LCD. The LCD panel can be blanked by setting the BLANK field of LCDC register. LCD driver can be totally turned off by clearing LCDE bit of LCDC.

LCDC	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Field	-	-	-	GRAY			BLANK	LCDE
Reset	-	-	-	-	-	-	1	0

Field	Value	Function
GRAY	000	LCD is darkest.
	111	LCD is lightest.
BLANK	0	normal display
	1	LCD display blanked. The COM signals of LCD driver output inactive levels (LVL4 and LVL1) while SEG signals output normal display patterns.
LCDE	0	LCD driver disabled, LCD driver has no output signal.
	1	LCD driver Enabled

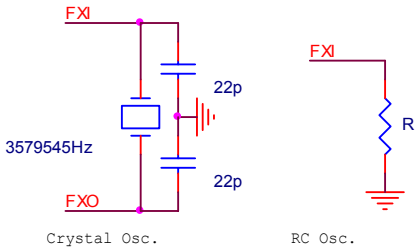
Please note that LCD driver must be turned off before the MCU goes into sleep mode. In other words, user must clear the bit 0 (LCDE bit) of LCDC to turn off LCD driving circuit before setting bit6 of OP1 to enter sleep mode. Large current might happen if the procedure is not followed.

Please note that LCD driver uses slow clock as clock source. The LCD display would not display normally if it worked in Fast clock only mode as the LCD refresh action would be too fast.

8. Oscillators

The MCU is equipped with two clock sources with a variety of selections on the types of oscillators to choose from. So that system designer can select oscillator types based on the cost target, timing accuracy requirements etc. Crystal, Resonator or the RC oscillator can be used as fast clock source, components should be placed as close to the pins as possible. The type of oscillator used is selected by mask option MO_FXTAL.

MO_FXTAL	Fast clock type
0	RC Oscillator.
1	Crystal Oscillator.



The RC oscillator has a built-in capacitor. An external resistor is needed to connect from FXI to GND to determine the oscillation frequency. The capacitance of internal RC oscillator is selected by mask option MO_RCAP[2..0].

MO_RCAP[2..0]	Internal RC Cap. OSC. (pF)
000	2
001	4
010	7
011	14
100	20
101	40
110	50
111	60

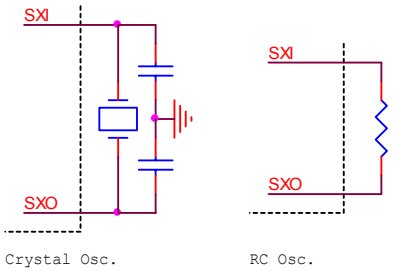
The following table shows the combinations of R and C, and the resulting frequency. Please note that oscillation frequency in the table only represents oscillation frequencies of certain samples. The actual oscillation frequency may vary up to ±15% from lot to lot due to process parameter variations. User must take this into consideration when using this chip in applications.

Ring Oscillator Frequency Table

R(K ohm)\C (pF)	40	20	14	7	4	2	
30.20	0.8	1.5	2.0	3.0	4.0	5.0	MHz
19.92	1.2	2.2	2.8	4.4	5.6	7.0	MHz
9.98	2.3	4.0	5.1	7.5	9.4	11.4	MHz

Two types of oscillator, crystal and RC, can be used as slow clock by mask option MO_SXTAL. If used for time keeping function or other applications that required the accurate timing, crystal oscillator is recommended. If the timing accuracy is not important, then RC type oscillator can be used to reduce cost.

MO_SXTAL	Slow clock type
0	R/C oscillator
1	Crystal oscillator



With two clock sources available, the system can switch among operation modes of Fast, Slow, Idle, and Sleep modes by the setting of OP1 and OP2 registers as shown in tables below to suit the needs of application such as power saving, etc.

OP1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	DRDY	STOP	SLOW	INTE	T2E	T1E	Z	C
Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	-	-

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			
Mode	R/W	R	R	R/W	W	W	W	W
Reset	0	-	-	0	-	-	-	-

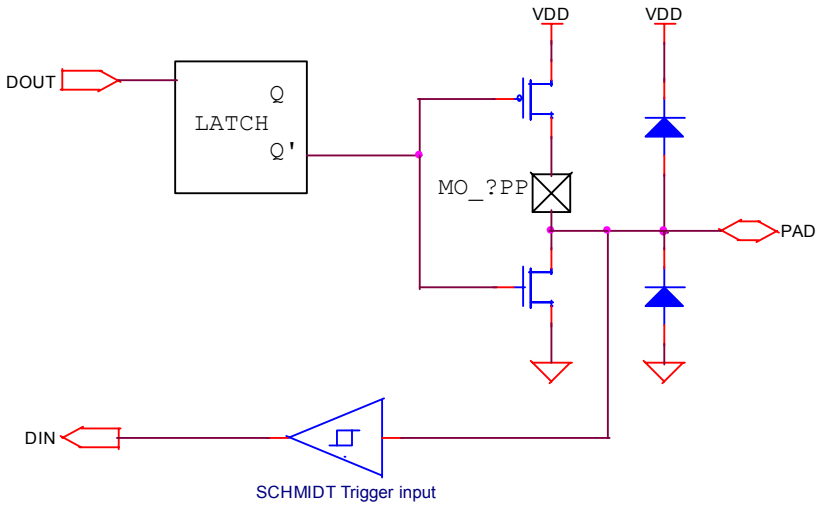
If the dual clock mode is used, the LCD display, Timer1 and Timer Base will derive its clock source from slow clock while the other blocks will operate with the fast clock.

9. General Purpose I/O

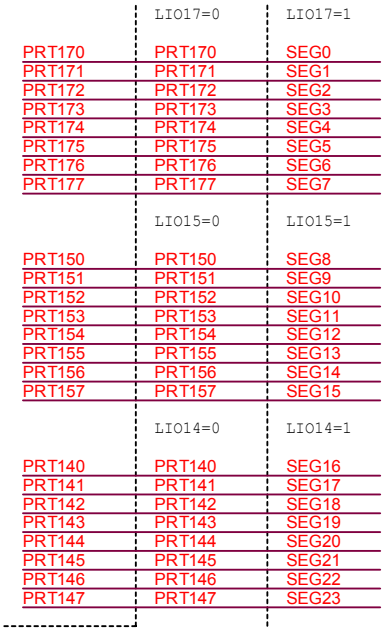
There are three dedicated general purpose I/O port, PRTC[4..7], PRTD and PRT10[0..3], while PRT14, PRT15 and PRT17 are multiplexed with LCD segment driver pins. All the I/O Ports are bi-directional and of non- tri-state output structure. The output has weak sourcing (50 μA) and stronger sinking (1 mA) capability and each can be configured as push-pull or open-drain output structure individually by mask option.

When the I/O port is used as input, the weakly high sourcing can be used as weakly pull-up. Open drain can be used if the pull-up is not required and let the external driver to drive the pin. Please note that a floating pad could cause more power consumption since the noise could interfere with the circuit and cause the input to toggle. A '1' needs to be written to port first before reading the input data from the I/O pin. If the PMOS is used as pull-up, care should be taken to avoid the constant power drain by DC path between pull-up and external circuit.

The input port has built-in Schmidt trigger to prevent it from chattering. Hysteresis level of Schmidt trigger is 1/3*VDD.



As pads of PRT14, PRT15 and PRT17 are shared with LCD segment driver, the function of the pads is determined by mask options.



Following table is the setting for MO_LIO?[...] and MO_?PP[...] and others related to LCD display setting and pin assignment features.

MO_LIO?[…]	MO_?PP[...]	I/O Port	LCD Pin
0	0	Open-drain output	--
0	1	Push-pull output	--
1	0	--	xx
1	1	--	LCD Display

--: Function not available.

xx: Displayable, but may have abnormal leakage current, do not use.

10. Key Scan Circuit

The built-in 4x20 hardware keyboard scan circuit helps to reduce the pin counts where application requires large key matrix and high LCD pixel count as well as the firmware effort. As key-scan pins are shared with LCD segment and PRTC4 ~ PRTC7 pins, it is advisable to put resistors between segment pins and key matrix to avoid shorting the segment pins when two or more keys in the same row are pressed simultaneously. Two key can be detected simultaneously and the first detected key code is stored in KEY0 register and the second in KEY1 register respectively. The key code for each key location is listed in the following table.

Key Loc	SCNI0	SCNI1	SCNI2	SCNI3
SCNO0	0x80	0xA0	0xC0	0xE0
SCNO1	0x81	0xA1	0xC1	0xE1
SCNO2	0x82	0xA2	0xC2	0xE2
SCNO3	0x83	0xA3	0xC3	0xE3
SCNO4	0x84	0xA4	0xC4	0xE4
SCNO5	0x85	0xA5	0xC5	0xE5
SCNO6	0x86	0xA6	0xC6	0xE6
SCNO7	0x87	0xA7	0xC7	0xE7
SCNO8	0x88	0xA8	0xC8	0xE8
SCNO9	0x89	0xA9	0xC9	0xE9
SCNO10	0x8A	0xAA	0xCA	0xEA
SCNO11	0x8B	0xAB	0xCB	0xEB
SCNO12	0x8C	0xAC	0xCC	0xEC
SCNO13	0x8D	0xAD	0xCD	0xED
SCNO14	0x8E	0xAE	0xCE	0xEE
SCNO15	0x8F	0xAF	0xCF	0xEF
SCNO16	0x90	0xB0	0xD0	0xF0
SCNO17	0x91	0xB1	0xD1	0xF1
SCNO18	0x92	0xB2	0xD2	0xF2
SCNO19	0x93	0xB3	0xD3	0xF3

KEY0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x22	R	Row Index		Column Index				

KEY1	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x23	R	Row Index		Column Index				

The bit 7 of KEY0 and KEY1 is repeat indicator when the same key is scanned for the second time, the R bit will be cleared to indicate the key is not released yet.

The key-scan function can be turned on/off by mask option MO_LCDKEY.

MO_LCDKEY	SGKY[43..24] Function
0	as SEG only

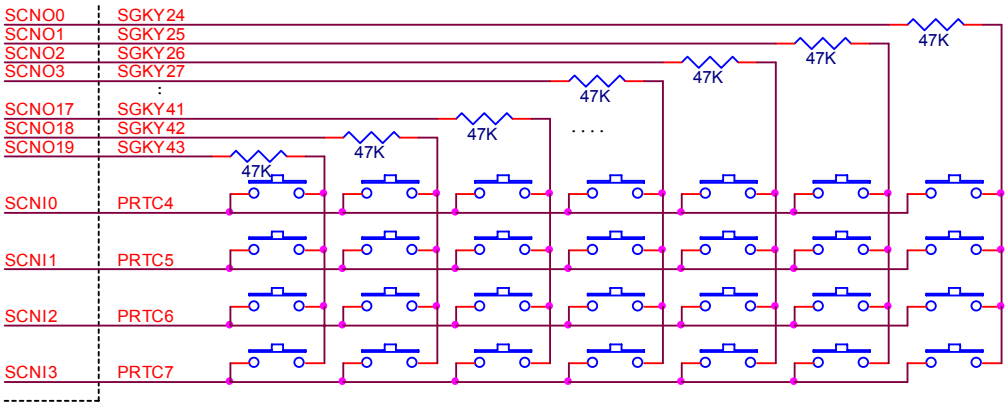
1	as SEG as well as KEY_SCAN

The pulse width of key-scan signal can be selected by mask options MO_SNCK[1..0].

MO_SNCK[1..0]	Key Scan Pulse Width
00	0.5 sck
01	1 sck
10	1.5 sck
11	2 sck

The strength of key-scan signal can also be selected by mask options MO_SNCK[1..0].

MO_SCDRV[1..0]	Key Scan Signal Strength
00	weakest
01	
10	
11	strongest

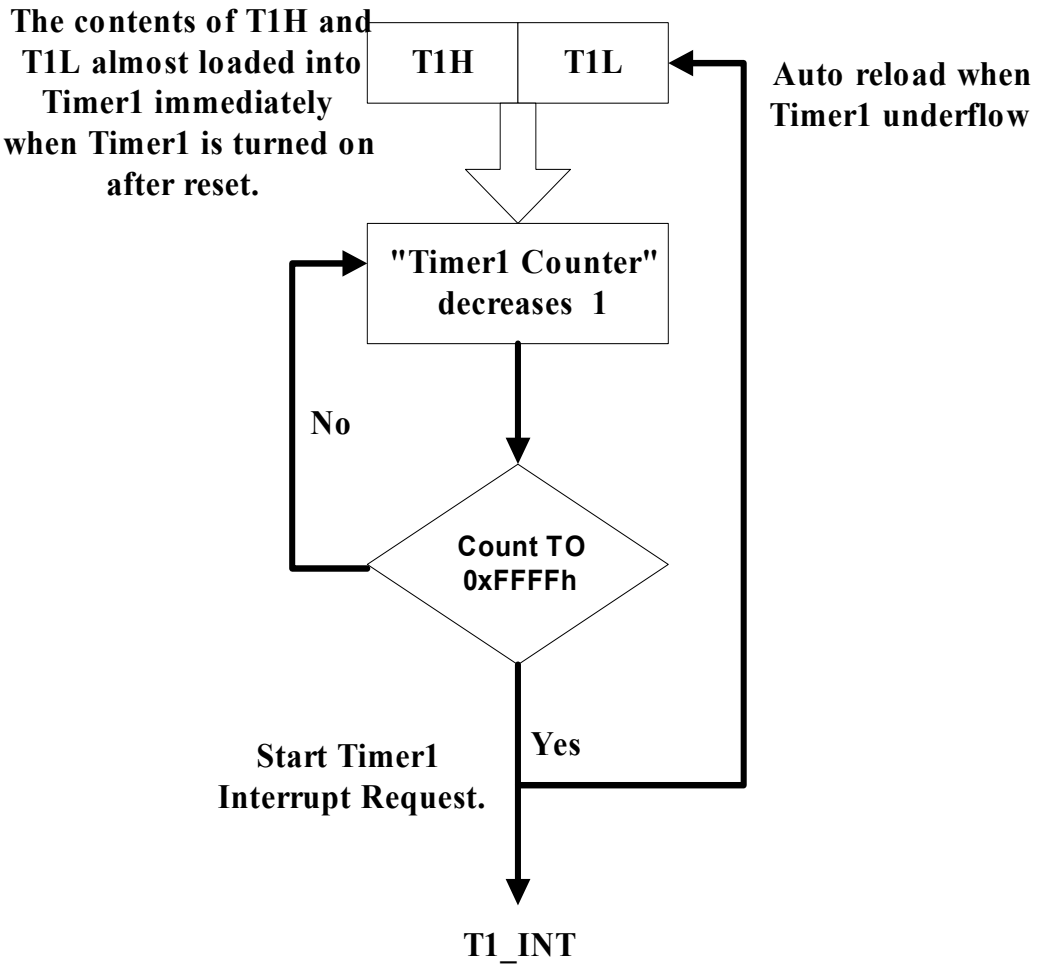


11. Timer1

The Timer1 consists of two 8-bit write-only preload registers T1H and T1L and 16-bit down counter. If Timer1 is enabled, the counter will decrement by one with each incoming clock pulse. Timer1 interrupt will be generated when the counter underflows - counts down to FFFFH. And the counter will be automatically reloaded with the value of T1H and T1L.

The clock source of Timer1 is derived from slow clock “SCK” at dual clock or slow clock only mode. And it comes from the fast clock “FCK” at fast clock only mode.

Please note that the interrupt is generated when counter counts from 0000H to FFFFH. If the value of T1H and T1L is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this moment, interrupt will be generated immediately and value of T1H and T1L will be loaded since it counts to FFFFH. So the T1H and T1L value should be set before enabling Timer1.



The Timer1 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC1_IER	2	R/W	0: TC1 interrupt is disabled. (default) 1: TC1 interrupt is enabled.
T1L	0x03	T1L[7:0]	7~0	W	Low byte of TC1 pre-load value
T1H	0x04	T1H[7:0]	7~0	W	High byte of TC1 pre-load value
OP1	0x09	TC1E	2	R/W	0: TC1 is disabled. (default) 1: TC1 is enabled.

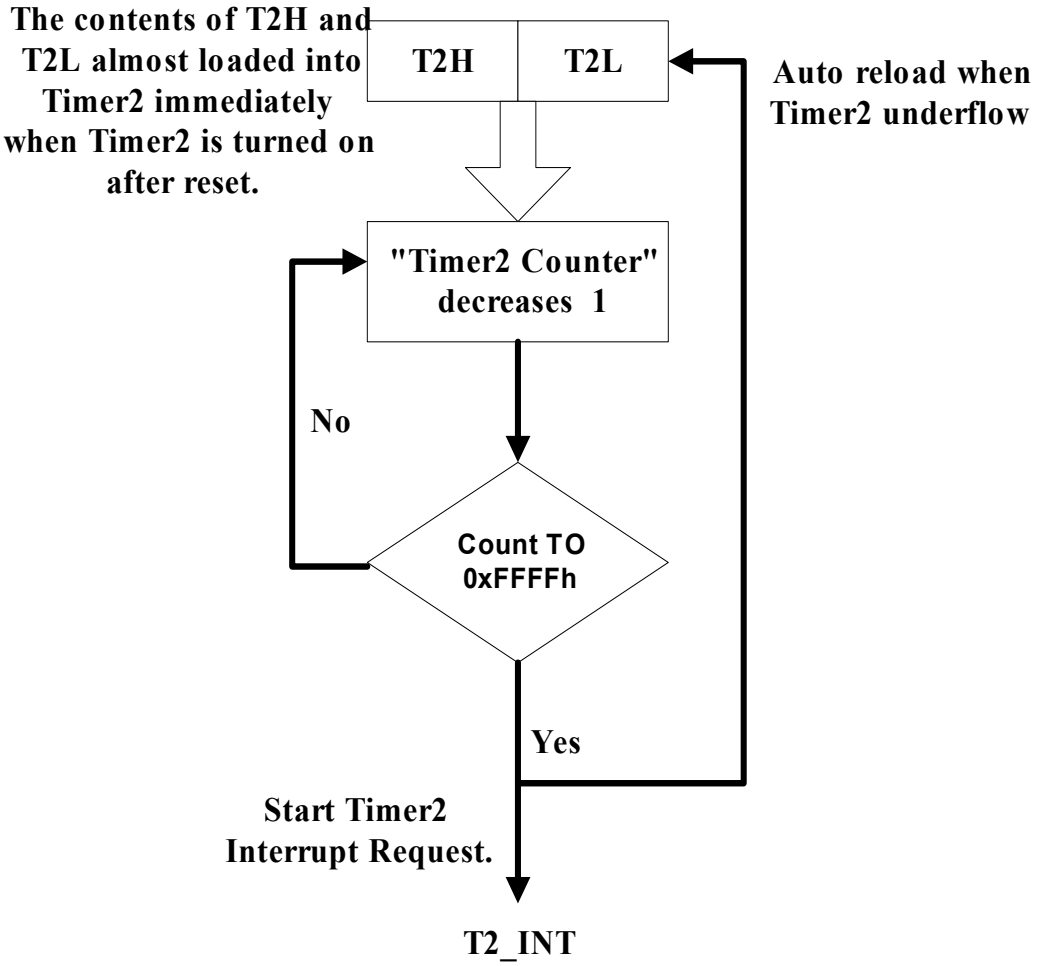
12. Timer2

Timer2 is similar in structure to Timer1 except that clock source of Timer2 comes from the system clock "Fsys"/1.5. The system clock "Fsys" varies depending on the operation modes of the MCU.

The Timer2 consists of two 8-bit write-only preload registers T2H and T2L and 16-bit down counter. If Timer2 is enabled, counter will decrement by one with each incoming clock pulse. Timer2 interrupt will be generated when the counter underflows - counts down to FFFFH. And it will be automatically reloaded

with the value of T2H and T2L.

Please note that the interrupt signal is generated when counter counts from 0000H to FFFFH. If the value of counter is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this time, the interrupt will be generated immediately and value of T2H and T2L will be loaded since the counter counts to FFFFH. So the T2H and T2L value should be set before enabling Timer2.



The Timer2 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC2_IER	1	R/W	0: TC2 interrupt is disabled. (default) 1: TC2 interrupt is enabled.
T2L	0x05	T2L[7:0]	7~0	W	Low byte of TC2 pre-load value
T2H	0x06	T2H[7:0]	7~0	W	High byte of TC2 pre-load value
OP1	0x09	TC2E	3	R/W	0: TC2 is disabled. (default) 1: TC2 is enabled.

13. Time Base Interrupt

The TB timer is used to generate time-out interrupt at fixed period. The time-out frequency of TB is determined by dividing slow clock with a factor selected in OP2[3..0]. TBE (Time Base Enable) bit controls enable or disable of the circuit.

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			
Mode	R/W	R	R	R/W	W	W	W	W
Reset	0	-	-	0	-	-	-	-

TBE	Function
0	Disable Time Base
1	Enable Time Base

For example, if the slow clock is 32768 Hz, then the interrupt frequency is as shown in following table.

TBS[3..0]	Interrupt Frequency
0000	16.384 KHz
0001	8.192 KHz
0010	4.096 KHz
0011	2.048 KHz
0100	1.024 KHz
0101	512 Hz
0110	256 Hz
0111	128 Hz
1000	64 Hz
1001	32 Hz
1010	16 Hz
1011	8 Hz
1100	4 Hz
1101	2 Hz
1110	1 Hz
1111	0.5 Hz

14. Watch Dog Timer

Watch Dog Timer (WDT) is designed to reset system automatically prevent system dead lock caused by abnormal hardware activities or program execution. WDT needs to be enabled in Mask Option.

MO_WDTE	Function
0	WDT disable
1	WDT enable

To use WDT function, “CLRWDT” instruction needs to be executed in every possible program path when the program runs normally in order to clears the WDT counter before it overflows, so that the

program can operate normally. When abnormal conditions happen to cause the MCU to divert from normal path, the WDT counter will not be cleared and reset signal will be generated.

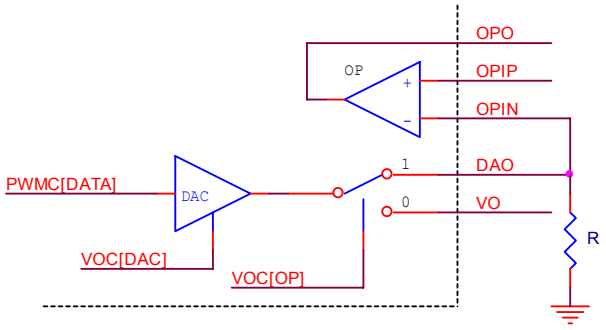
WDT is the enabling signal generated by calculating 32768-clock overflow. Reset Register content is same as TC1 (Timer1 clock), which uses the same clock count source. WDT function can be generated in Normal, Slow and Idle Mode. However, WDT will not function during Sleep Mode (as the TC1 clock has stopped.)

15. Digital-to-Analog Converter

The Digital-to-Analog converter (DAC) converts 7-bit unsigned speech data written to PWMC data register to proportional current.

PWMC register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA & PWM Data	0	DA and PWM output value						
Control	1	PWM O/P driver			-	-	-	PWME

There are two output paths for the DAC. Either VO or DAO can be selected as output port of DAC by VOC register when it is enabled. The VO output is primarily intended for speech generation, although it is not necessary so, while the DAO output path can be used in conjunction with built-in OP comparator to function as an Analog-to-Digital Converter as required in applications such as speech recording, speech recognition or sensor interfaces.



The DAC is enabled by DAC bit of VOC register. Please note that the DAC bit of VOC register will be automatically cleared when the system enter Idle or Sleep mode. So it needs to be set again when returning to Normal mode.

VOC register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	-	-	-	-	-	PWM	DAC	OP
Reset	-	-	-	-	-	0	0	0

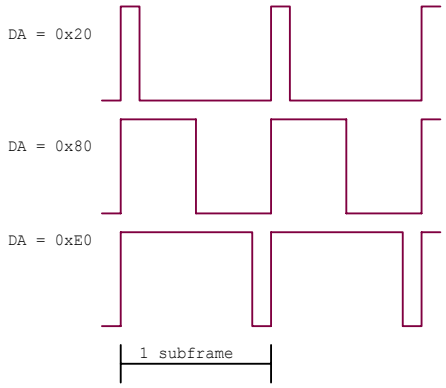
Bit	Name	Value	Function description
1	DAC	1	DA Enable
		0	DA Disable

The output current of the DAC is programmable by mask option MO_DACISEL:

MO_DACISEL[1:0]	DAC output current
00	0.375 mA
01	0.75 mA
10	1.5 mA
11	3 mA

16. Pulse-Width Modulation

The pulse-width modulator (PWM) converts 7-bit unsigned speech data written to PWMC data register to proportional duty cycle of PWM output. PWM module shares the PWMC data register with Digit-to-Analog Converter. So PWM and DA output can exist at the same time. When PWM circuit is enabled, it generates signal with duty ratio in proportion to the DA value.



The PWM bit of VOC register controls register to enable the circuit and output driver. When PWM bit of VOC is ‘0’, PWME bit and output drivers settings are both cleared. To use PWM for voice output, PWM bit has to be set to ‘1’ first, then set PWME bit and enable output driver by setting the driver number. If PWM bit is disabled and enabled again, the setting for driver and PWME bit will be clear.

The Fast Clock is gated through PWME bit of PWMC command register to provide the clock source of PWM circuit when it is enabled. As PWM needs higher frequency to operate, it cannot generate correct PWM signal in Slow clock only mode.

When the program enters into Sleep mode or Idle mode, it will automatically turn off all voice outputs by clearing VOC[2:1] to ”00”. To activate voice output again when returning to Normal Mode, the VOC register needs to be set again.

The PWM output volume can be adjusted by command register PWMC[6:4]. The bit 6 and 5 control 2 time driver, while bit 4 controls 1 time driver, thus it has 5 levels of driver output. By turning on/off the internal drivers, the sound level of PWM output can be turned up and down. Please note that this adjustment apply only to PWM, but not DA output.

PWM output driver selection

PWMC[6..4]	Number of Driver
000	off
001	1
010	2
011	3
100	2
101	3
110	4
111	5

17. Dual-Tone Multiple Frequency Generator

The Dual-Tone Multiple Frequency (DTMF) generator is used to generate the Tone Dialing signal used in Telecommunication applications. In fact, it can be used to generate any two channel sinusoidal wave signal with frequencies ranging from 1 ~ 4095 Hz with 1 Hz resolution. The DTMF generator derives its clock from 32768 Hz.

The DTMF generator is controlled through DTMFC (DTMF Control) Register. DTMFC can only be written, and it can not be read. The DTMFC register actually maps to Row Register, Column Register and Command Register. So when writing to DTMFC, the actual register being written is determined by Bit 7 and 6.

DTMFC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ROW HIGH	0	0	M11	M10	M9	M8	M7	M6
ROW LOW	0	0	M5	M4	M3	M2	M1	M0
COL HIGH	0	1	M11	M10	M9	M8	M7	M6
COL LOW	0	1	M5	M4	M3	M2	M1	M0
COMMAND	1	1	HOOK	KT	CH1	CH0	DTMF	HB(1)/LB(0)

Bit 5 of command register (HOOK bit) is the main switch of DTMF Generator block. When HOOK Bit is '1', the entire block will be turned off and all internal registers will be not reset. When HOOK Bit is '0', the block will be turned on.

The Row and Column registers determine the frequencies of two channels sine wave generator. As they are 12-bit register, they need to be divided into high parts and low part when writing. The procedure of changing the Row and Column frequency is by selecting High or Low byte to be written in the command register, write to the target register, then toggle the HB/LB bit, and then write to the second part of the register. When both frequencies are set, the DTMF tone can be sent to DTMFO output by turning on bit 1 (DTMF bit) of command register. When DTMF bit is '1', DTMF signal can be output, and the output is disabled when DTMF bit is '0'.

In addition to dual tone generation, the DTMF generation can be used to generate single channel tone determined by either ROW frequency or COL frequency or switching between the two frequencies with

continuous phase. This feature is useful for generating phase coherent FSK (Frequency Shift Keying) tone as often used in Telecommunication.

The frequency range is further expanded to 4095 Hz to cover the more range. For example, the Caller Alerting Tone requires 2130 and 2750 Hz tones to be generated which is beyond the range of the original design.

Bit3	Bit2	Channel select
0	0	Row + Column
0	1	Row frequency
1	0	Column frequency.
1	1	x

In addition to DTMF generation function, this function block also provides others features which are useful for the phone application. For example, Bit 4 (KT bit) of command register controls the generation of 1024 Hz square wave to provide the audio feedback to the user in response to key presses. When KT bit is '1', square wave generation is enabled, and when KT bit '0', the square wave is disabled. The DTMF and Keytone outputs are not dedicated output pins, but are multiplexed with I/O PRT10[0] and PRT10[1]. The functions of these two pins are determined by mask options MO_TONE and MO_KEYTONE.

Mask Option	Value	Function
MO_TONE	0	Normal I/O pin (PRT10[0])
	1	TONEO output through prt10[0]
MO_KEYTONE	0	Normal I/O pin (PRT10[1])
	1	KEYTONE output through prt10[1]

18. Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{DD}	-0.5V ~ 4.0V	
LCD Operating Voltage	V_{LVL5}	< 8.5 V	
Input Voltage	V_{IN}	-0.5V ~ V_{DD}+0.5V	
Output Voltage	V_O	-0.5V ~ V_{DD}+0.5V	
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

19. Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{DD}	2.4V ~ 3.6V	
Input Voltage	V_{IH}	0.9 V_{DD} ~ V_{DD}	
	V_{IL}	0.0V ~ 0.1V_{DD}	
		8 MHz	V_{DD} =3.0V

Operating Frequency	F_{MAX}	8 MHz	V_{DD} =3.0V
		6 MHz	V_{DD} =2.4V
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

20. AC/DC Characteristics

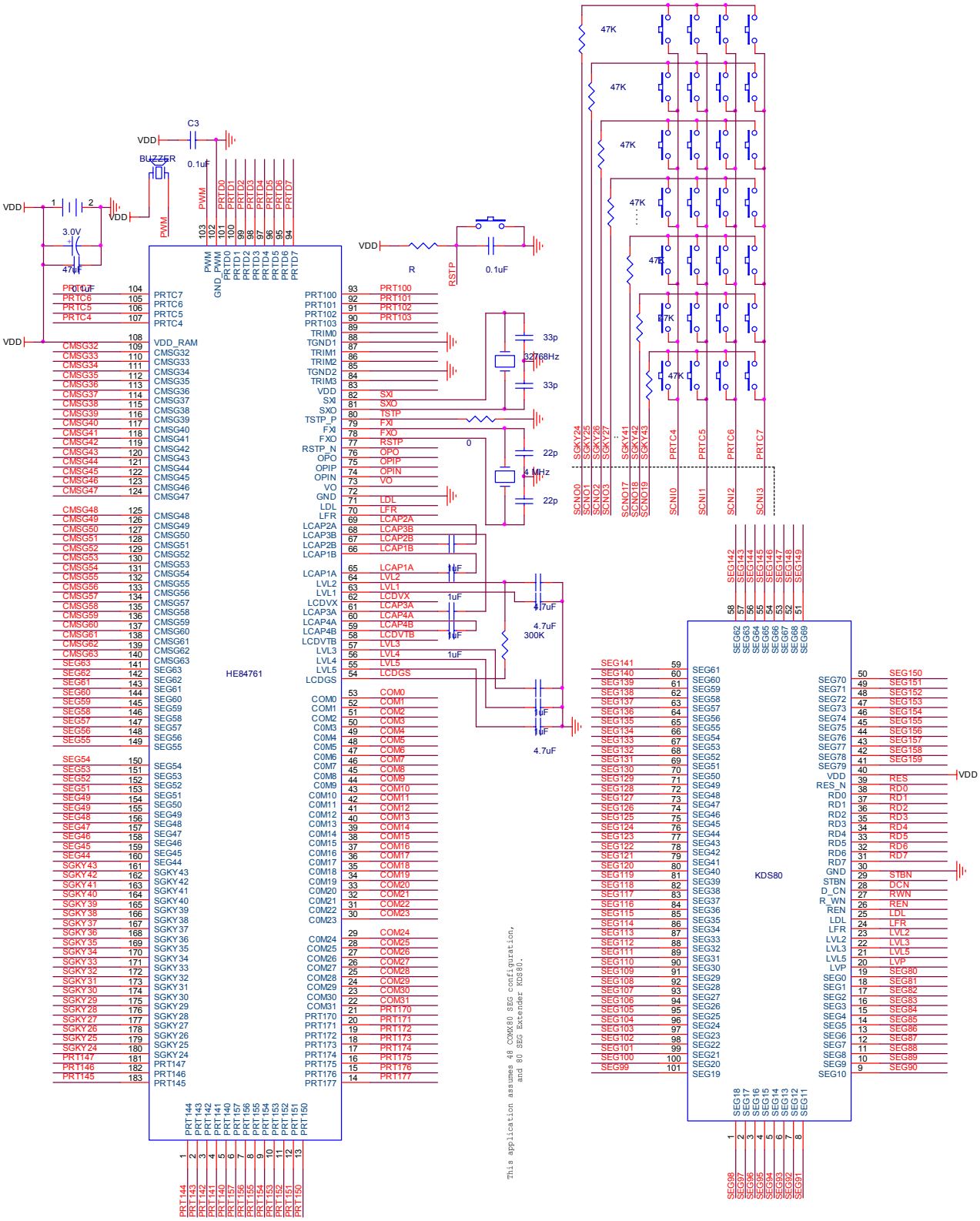
Testing Condition : TEMP=25℃, VDD=3V±10%

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Power consumption						
Normal mode current	I_{FAST}		1	1.5	mA	2M external R/C fast clock
Slow mode Current	I_{SLOW}		15	30	µA	32768 Hz slow clock with LCD disabled
Idle mode Current	I_{IDLE}		10	20	µA	32768 Hz slow clock with LCD disabled
Sleep mode Current	I_{SLEEP}			1	µA	
Additional Current if LCD ON	I_{LCD}		150	220	µA	1/7 bias, no load on SEG and COM pins
I/O specification						
Input High Voltage	V_{IH}	0.8			VDD	Input Pins
Input Low Voltage	V_{IL}			0.2	VDD	Input Pins
Input Hysteresis Width	V_{HYS}		1/3		VDD	I/O, RSTP_N Threshold = 2/3*VDD (Input from low to high), Threshold = 1/3*VDD (Input from high to low)
Output Source Current	I_{OH}	50			µA	Output drive high[*1], V_{OL}=2.0V
Output Sink Current	I_{OL1}	1.0			mA	Output drive low, V_{OL}=0.4V
Input Low Current	I_{IL1}		20		µA	RSTP_N, V_{IL} = GND, Pull high Internally
Input Low Current	I_{IL2}		100		µA	I/O, V_{IL}=GND, if pull high Internally by user
PWM and DAC						
PWM Output Current	I_{PWM}	10	14		mA	PWM[*2] With 32Ω Loading
		6	8		mA	With 64Ω Loading
		4	5		mA	With 100Ω Loading
DAC Output Current	I_{oVO}	2.5	3		mA	VO, DAO@ VDD=3V,VO=0~2V, Data = 7F
Data Retention						
Data Retention Voltage	V_{DR}	1.2			Volts	

Notes:

1. The "Output Source Current" specification is applicable only to the Push-Pull I/O type.
2. This Specification indicates only one PWM driving capability, and there are totally five built-in drivers, user can multiply the actual number of driver to get the total amount of current. (IPWM * N; N=0, 1, 2, 3, 4, 5)

21. Application Circuit



22. Important Note

1. Please note that ICE is different from IC. ICE is the super set of HE80000 series IC, but each IC is a subset of ICE. Never use any hardware resource that real IC doesn't have, especially RAM and register. KBIDS and compiler cannot prevent user to use some hardware resource that didn't exist.
2. Please use ICE5.x (Type-III LCD Driver) to emulate the equivalent effect of Type-IV LCD driver. The same bias and LV5 will get almost the same result of display effect. Adjust your bias and LVL5 on ICE 5.x and make sure the display of LCD is OK. Then the display effect of 84760 (Type-IV LCD driver) will be the same at the same bias and LV5.
3. When accessing any address large than 64KB, users must update TPP first, TPH then TPL. Only by this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate this accessing process on ICE. So 5us delay should be added by firmware.
4. LCD driving circuit must be turned off before IC goes into sleep mode.
5. Please bond the TSTP_P, RSTP_N and PRTD[7:0] with test points on PCB, which can be soldered and probed, and connect TSTP_P pin with zero ohm resistor to GND (or copper wire which can be cut easily on PCB) for good ESD protection. So that IC testing can be done on PCB, if necessary by removing the 0-ohm resistor and driving TSTP_P pin to high.
6. LV5 must be lower than 8.5 Volt. Otherwise IC may breakdown.
7. ***The voltage adjustment mechanism shall be reserved for LV2 voltage fine-tunes; since it's possible there is some variation in LV2 voltage due to IC manufacture process variation. User can use variable-resistor to adjust the LV2 voltage or use some tools to detect the LV2 and then select a proper resistor. Please refer to application note AN025 for the detailed description.***
8. Users must call the library " swap_page" in the file swappage.asm of application note AN029. The real IC register is different from ICE4.x or ICE5.x. This subroutine make sure that users can run on both real IC and ICE for page swapping. The program of swappage.asm as following:

```
.area       swapping_variable(data)
    _mapreg1::          .ds         1  ;store page register(R1Bh)
    mapreg2::           .ds         1   ;store page register(R1Ch)
    .area       swappingpage(code,pag0)


;=====================================================
    ;swap page function
    ;=====================================================
    swappage::
        lda   #10h
        sta   mapreg1
        lda   #00h              ; P1EO[2]   <--0     to enable Port R1Fh
        sta   riceco            ; RICECO is write only
```

```
        lda   mapreg2
        sta   riced
        lda   _mapreg2
        anda  #0fh
        ora   #20h      ;Mapping mapreg2 low nibble to Logical segment2
;       sta   r1Ch
        sta   rps1
        lda   _mapreg2
        rorc
        rorc
        rorc
        rorc
        anda  #0fh      ;Mapping _mapreg2 high nibble to Logical segment3
        ora   #30h
;       sta   r_ps1
        sta   r1Ch
        ret
```

23. Updated Record

Version	Date	Section	Original Content	New Content
1.1	July26,2002	D,G,H		Add TGND1 and TGND2 pins.
1.2	Feb 13, 2003			Added function block descriptions