

**Document Title****512Kx8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Data</u></b>	<b><u>Remark</u></b>
0.0	Initial draft	December 17, 1996	Preliminary
1.0	Finalize - Change datasheet format - Erase low power part from product - Erase 70ns part from KM68U4000B family - Power dissipation Improved 0.7 to 1.0W - $V_{IL}(\text{MAX})$ improved 0.4 to 0.6V. - $I_{CC2}$ decreased 50 to 45mA.	January 14, 1998	Final
2.0	Revise - $I_{CC1}$ decreased 20 to 25mA	February 12, 1998	Final
3.0	Revise - Adopt new code. KM68V4000B → K6T4008V1B KM68U4000B → K6T4008U1B - Improve $V_{OH}$ on DC AND OPERATING CHARACTERISTICS from 2.2 to 2.4V.	February 25, 2000	Final
4.0	Revise - Add 70ns part to K6T4008V1B-F family	August 31, 2000	Final

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## 512K×8 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology: TFT
- Organization: 512K×8
- Power Supply Voltage
  - K6T4008V1B Family: 3.0~3.6V
  - K6T4008U1B Family: 2.7~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three State Outputs
- Package Type: 32-SOP, 32-TSOP2-400F/R

### GENERAL DESCRIPTION

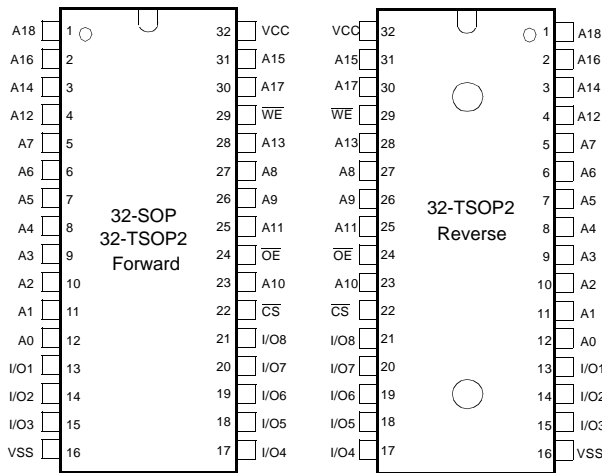
The K6T4008V1B and K6T4008U1B families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature range and have various package type for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Max)	Operating (I <sub>CC2</sub> , Max)	
K6T4008V1B-B	Commercial(0~70°C)	3.0~3.6V	70 <sup>1)</sup> /85 <sup>1)</sup> /100ns	15μA	45mA	32-SOP 32-TSOP2-400F/R
K6T4008U1B-B		2.7~3.3V	85 <sup>1)</sup> /100ns			
K6T4008V1B-F	Industrial(-40~85°C)	3.0~3.6V	70 <sup>1)</sup> /85 <sup>1)</sup> /100ns	20μA		
K6T4008U1B-F		2.7~3.3V	85 <sup>1)</sup> /100ns			

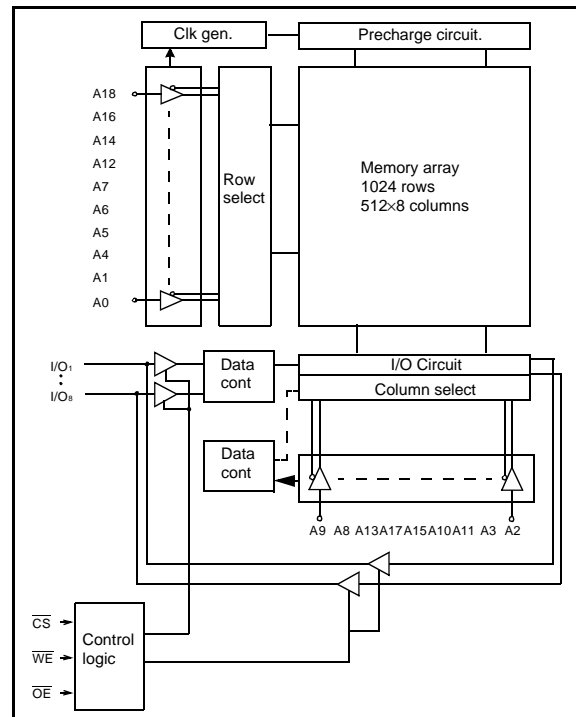
1. The parameter is measured with 30pF test load.

### PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
A0~A18	Address Inputs		

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Commercial Temp Products(0~70°C)		Industrial Temp Products(-40~85°C)	
Part Name	Function	Part Name	Function
K6T4008V1B-GB70	32-SOP, 70ns, 3.3V,LL	K6T4008V1B-GF70	32-SOP, 70ns, 3.3V,LL
K6T4008V1B-GB80	32-SOP, 85ns, 3.3V,LL	K6T4008V1B-GF85	32-SOP, 85ns, 3.3V,LL
K6T4008V1B-GB10	32-SOP, 100ns, 3.3V,LL	K6T4008V1B-GF10	32-SOP, 100ns, 3.3V,LL
K6T4008V1B-VB70	32-TSOP2-F, 70ns, 3.3V,LL	K6T4008V1B-VF70	32-TSOP2-F, 70ns, 3.3V,LL
K6T4008V1B-VB85	32-TSOP2-F, 85ns, 3.3V,LL	K6T4008V1B-VF85	32-TSOP2-F, 85ns, 3.3V,LL
K6T4008V1B-VB10	32-TSOP2-F, 100ns, 3.3V,LL	K6T4008V1B-VF10	32-TSOP2-F, 100ns, 3.3V,LL
K6T4008V1B-MB70	32-TSOP2-R, 70ns, 3.3V,LL	K6T4008V1B-MF70	32-TSOP2-R, 70ns, 3.3V,LL
K6T4008V1B-MB85	32-TSOP2-R, 85ns, 3.3V,LL	K6T4008V1B-MF85	32-TSOP2-R, 85ns, 3.3V,LL
K6T4008V1B-MB10	32-TSOP2-R, 100ns, 3.3V,LL	K6T4008V1B-MF10	32-TSOP2-R, 100ns, 3.3V,LL
K6T4008U1B-GB85	32-SOP, 85ns, 3.0V,LL	K6T4008U1B-GF85	32-SOP, 85ns, 3.0V,LL
K6T4008U1B-GB10	32-SOP, 100ns, 3.0V,LL	K6T4008U1B-GF10	32-SOP, 100ns, 3.0V,LL
K6T4008U1B-VB85	32-TSOP2-F, 85ns, 3.0V,LL	K6T4008U1B-VF85	32-TSOP2-F, 85ns, 3.0V,LL
K6T4008U1B-VB10	32-TSOP2-F, 100ns, 3.0V,LL	K6T4008U1B-VF10	32-TSOP2-F, 100ns, 3.0V,LL
K6T4008U1B-MB85	32-TSOP2-R, 85ns, 3.0V,LL	K6T4008U1B-MF85	32-TSOP2-R, 85ns, 3.0V,LL
K6T4008U1B-MB10	32-TSOP2-R, 100ns, 3.0V,LL	K6T4008U1B-MF10	32-TSOP2-R, 100ns, 3.0V,LL

Note: LL means Low Low standby current

## FUNCTIONAL DESCRIPTION

CS	OE	WE	I/O	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care (Must be in low or high state)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> ,V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.3 to 4.6	V	-
Power Dissipation	P <sub>D</sub>	1	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	K6T4008V1B-B, K6T4008U1B-B
		-40 to 85	°C	K6T4008V1B-F, K6T4008U1B-F
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	K6T4008V1B Family	3.0	3.3	3.6	V
		K6T4008U1B Family	2.7	3.0	3.3	
Ground	V <sub>SS</sub>	All Family	0	0	0	V
Input high voltage	V <sub>IH</sub>	K6T4008V1B, K6T4008U1B Family	2.2	-	V <sub>CC</sub> +0.3 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	K6T4008V1B, K6T4008U1B Family	-0.3 <sup>3)</sup>	-	0.6	V

Note:

- Commercial Product: T<sub>A</sub>=0 to 70°C, otherwise specified.  
Industrial Product: T<sub>A</sub>=-40 to 85°C, otherwise specified.
- Overshoot: V<sub>CC</sub>+3.0V in case of pulse width ≤ 30ns.
- Undershoot: -3.0V in case of pulse width ≤ 30ns.
- Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

- Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Operating power supply	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}=V_{IL}$ , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> , Read	-	-	10	mA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS} \leq 0.2V$ V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	Read	-	-	10	mA
			Write	-	-	25	
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}=V_{IL}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	45	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}=V_{IH}$ , Other inputs = V <sub>IL</sub> or V <sub>IH</sub>	-	-	0.5	mA	
Standby	I <sub>SB1</sub>	$\overline{CS} \geq V_{CC}-0.2V$ , Other inputs=0~V <sub>CC</sub>	-	-	15 <sup>1)</sup>	μA	

- Industrial product = 20μA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V

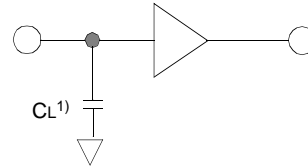
Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load(see right):  $C_L=100\text{pF}+1\text{TTL}$

$C_L^{(1)}=30\text{pF}+1\text{TTL}$

1. K6T4008V1B-70, K6T4008V1B-85 Family and K6T4008U1B-85 Family



1. Including scope and jig capacitance

## AC CHARACTERISTICS

(K6T4008V1B Family:  $V_{CC}=3.0\sim 3.6\text{V}$ , K6T4008U1B Family:  $V_{CC}=2.7\sim 3.3\text{V}$ )

Commercial product:  $T_A=0$  to  $70^\circ\text{C}$ , Industrial product:  $T_A=-40$  to  $85^\circ\text{C}$ )

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	70	-	85	-	100	-	ns
	Address access time	t <sub>AA</sub>	-	70	-	85	-	100	ns
	Chip select to output	t <sub>CO</sub>	-	70	-	85	-	100	ns
	Output enable to valid output	t <sub>OE</sub>	-	35	-	40	-	50	ns
	Chip select to low-Z output	t <sub>LZ</sub>	10	-	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	0	25	0	25	0	30	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	25	0	25	0	30	ns
	Output hold from address change	t <sub>OH</sub>	10	-	10	-	15	-	ns
Write	Write cycle time	t <sub>WC</sub>	70	-	85	-	100	-	ns
	Chip select to end of write	t <sub>CW</sub>	60	-	70	-	80	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	60	-	70	-	80	-	ns
	Write pulse width	t <sub>WP</sub>	55	-	55	-	70	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	25	0	25	0	30	ns
	Data to write time overlap	t <sub>DW</sub>	30	-	35	-	40	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	0	-	ns
	End write to output low-Z	t <sub>OW</sub>	5	-	5	-	5	-	ns

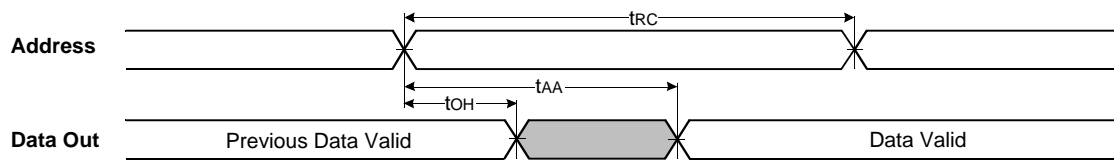
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS} \geq V_{CC}-0.2\text{V}$	2.0	-	3.6	V
Data retention current	I <sub>DR</sub>	$V_{CC}=3.0\text{V}$ , $\overline{CS} \geq V_{CC}-0.2\text{V}$	-	0.5	15 <sup>1)</sup>	$\mu\text{A}$
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms
Recovery time	t <sub>RDR</sub>		5	-	-	

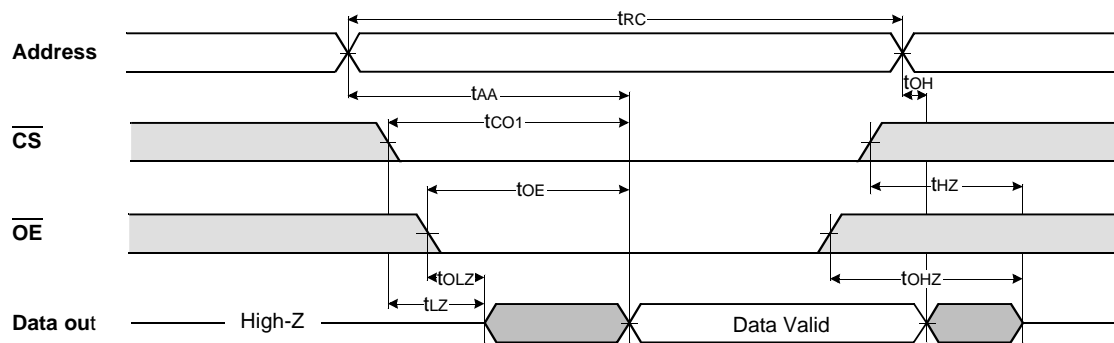
1. Industrial product = 20 $\mu\text{A}$

## TIMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )



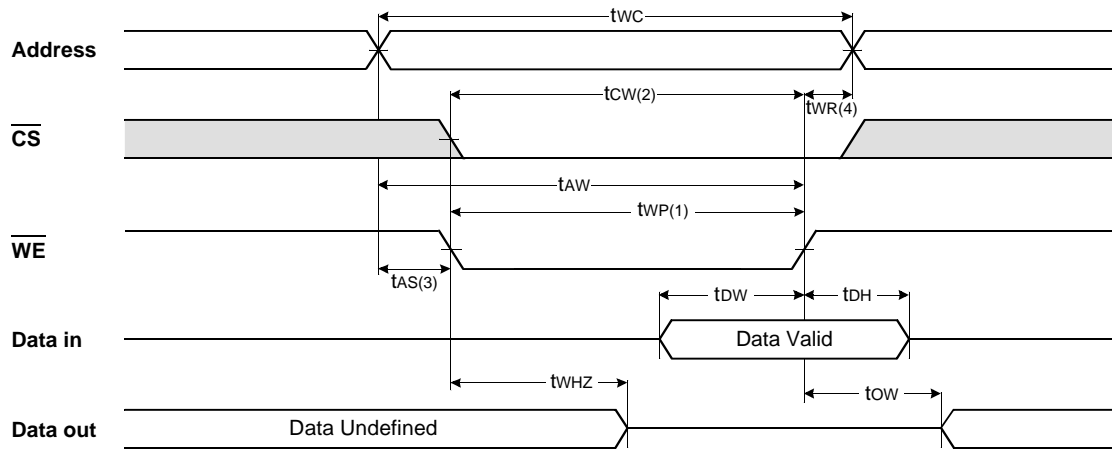
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



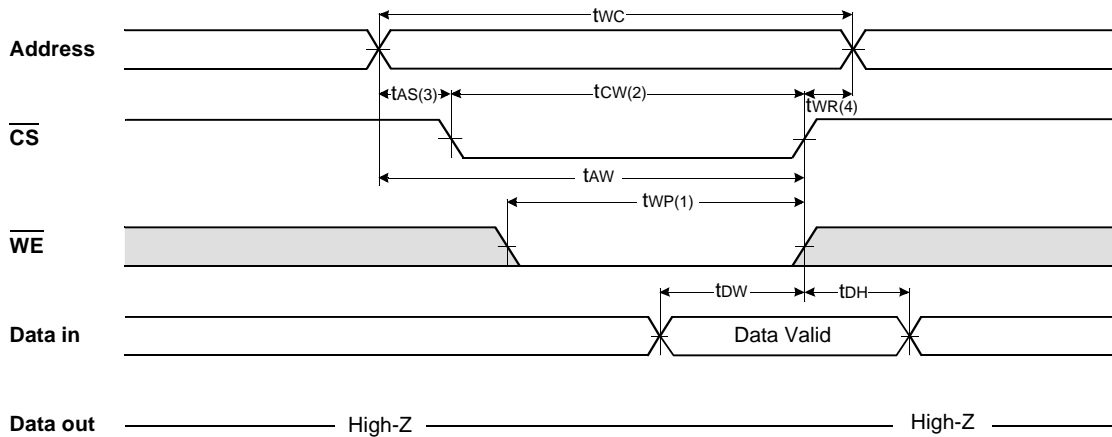
**NOTES (READ CYCLE)**

1.  $t_{HZ}$  and  $t_{OH}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

## TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$ Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS}$ Controlled)

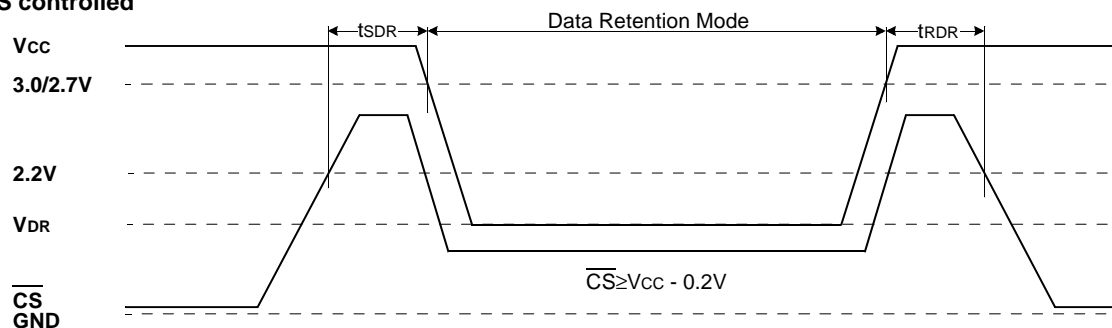


### NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}$  going Low and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS}$  going high and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{WC}$  is measured from the  $\overline{CS}$  going low to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.

## DATA RETENTION WAVE FORM

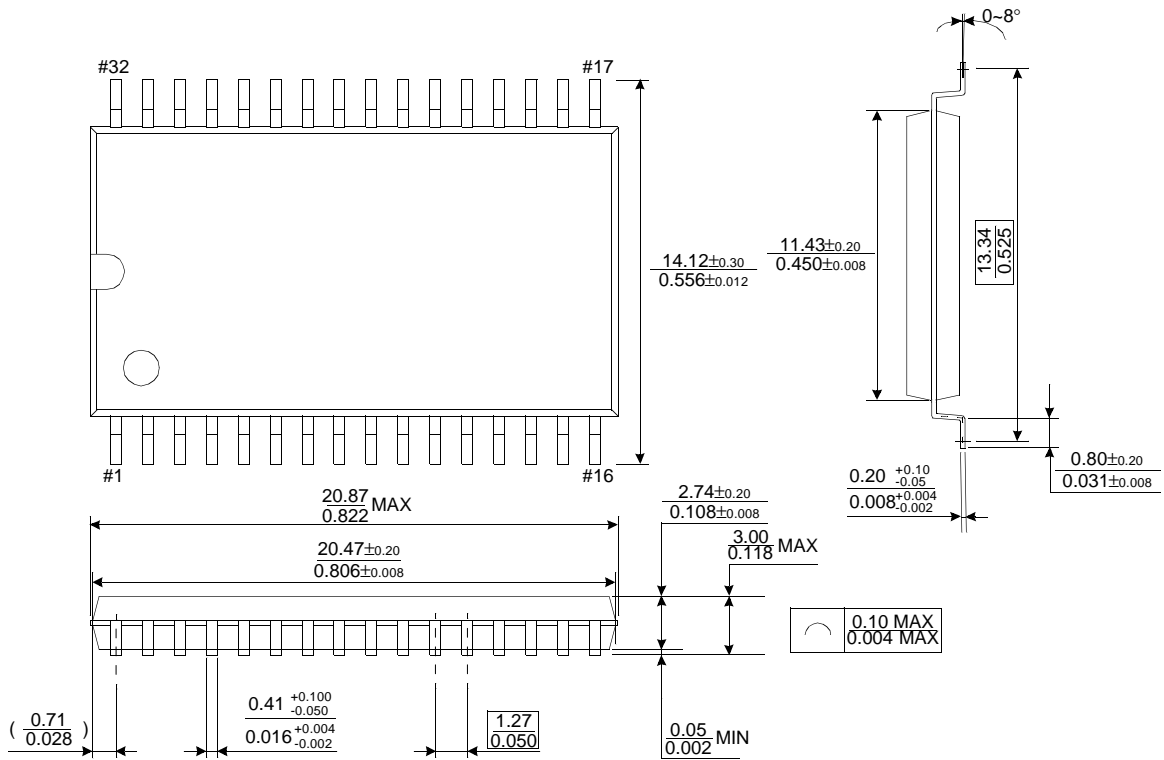
### $\overline{CS}$ controlled



## PACKAGE DIMENSIONS

Units : millimeter(inch)

### 32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)

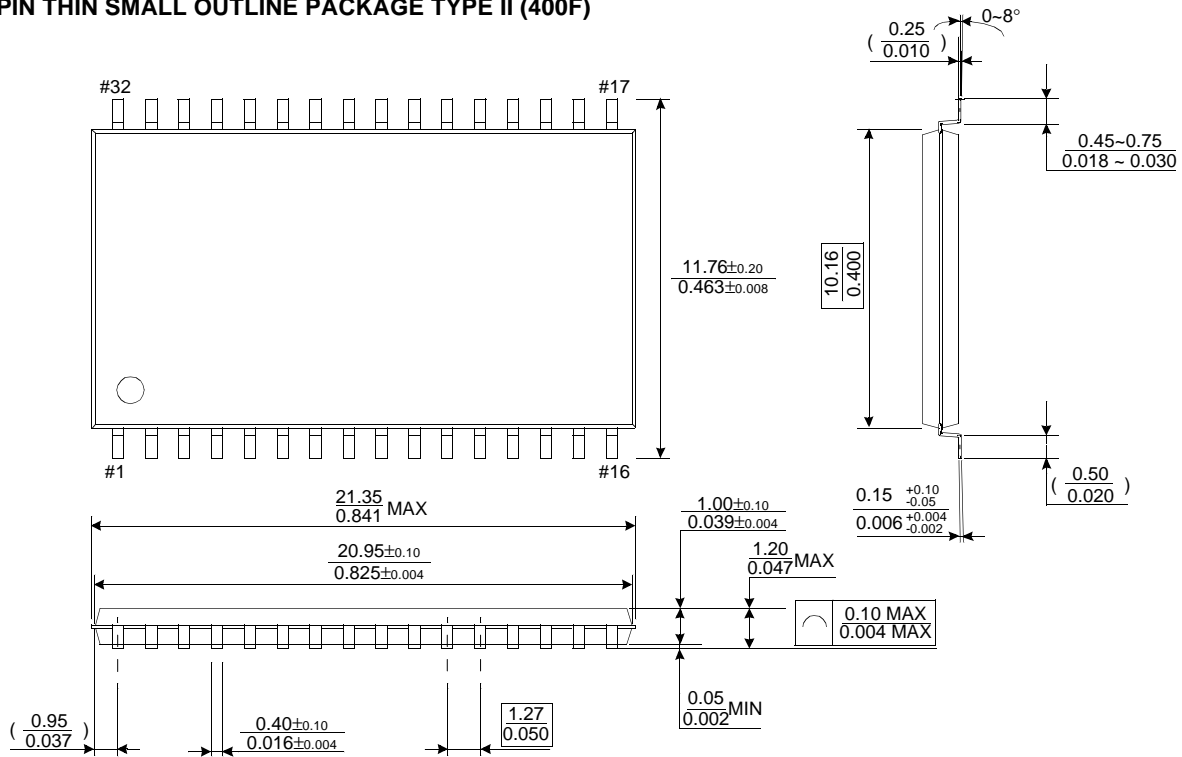




## PACKAGE DIMENSIONS

Units : millimeter(inch)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)

