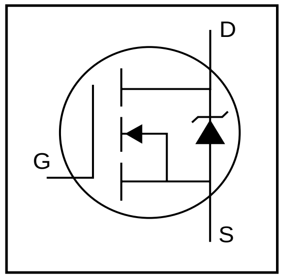
International
IOR Rectifier

PD - 94050A

IRFZ44VS
IRFZ44VL

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Optimized for SMPS Applications



V_{DSS} = 60V

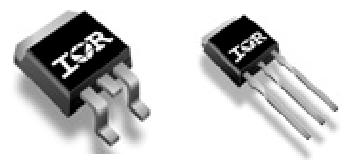
$R_{DS(on)}$ = 16.5mΩ

I_D = 55A

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D^2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D^2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.
The through-hole version (IRFZ44VL) is available for low-profile applications.



D^2Pak IRFZ44VS   TO-262 IRFZ44VL

Absolute Maximum Ratings

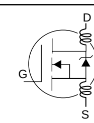
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	55	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	39	
I_{DM}	Pulsed Drain Current ①	220	
P_D @T_C = 25°C	Power Dissipation	115	W
	Linear Derating Factor	0.77	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	115	mJ
I_{AR}	Avalanche Current①	55	A
E_{AR}	Repetitive Avalanche Energy①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

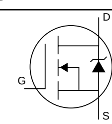
	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case	——	1.3	°C/W
$R_{θJA}$	Junction-to-Ambient	——	40	

01/04/02

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.062	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	16.5	mΩ	V_{GS} = 10V, I_D = 31A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	24	—	—	S	V_{DS} = 25V, I_D = 31A④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS} = 60V, V_{GS} = 0V
		—	—	250		V_{DS} = 48V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	67	nC	I_D = 51A
Q_{gs}	Gate-to-Source Charge	—	—	18		V_{DS} = 48V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	25		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	V_{DD} = 30V
t_r	Rise Time	—	97	—		I_D = 51A
$t_{d(off)}$	Turn-Off Delay Time	—	40	—		R_G = 9.1Ω
t_f	Fall Time	—	57	—		R_D = 0.6Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1812	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	393	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	103	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	55	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	220		
V_{SD}	Diode Forward Voltage	—	—	2.5	V	T_J = 25°C, I_S = 51A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	70	105	ns	T_J = 25°C, I_F = 51A
Q_{rr}	Reverse Recovery Charge	—	146	219	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 89μH R_G = 25Ω, I_{AS} = 51A. (See Figure 12)

③ $I_{SD} \leq$ 51A, di/dt ≤ 227A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

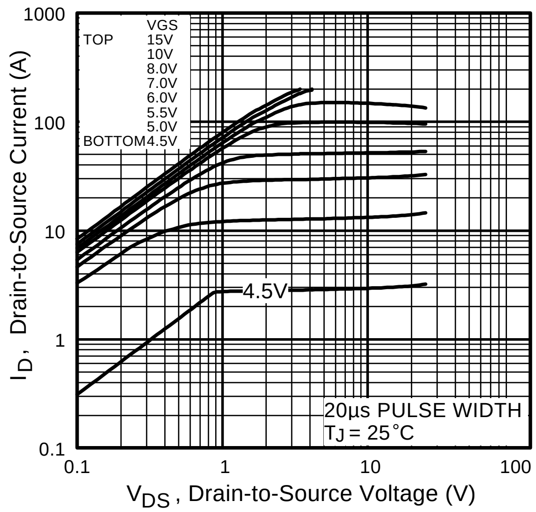


Fig 1. Typical Output Characteristics

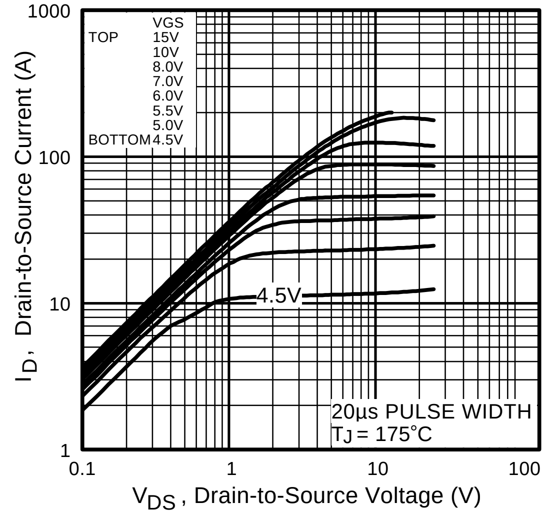


Fig 2. Typical Output Characteristics

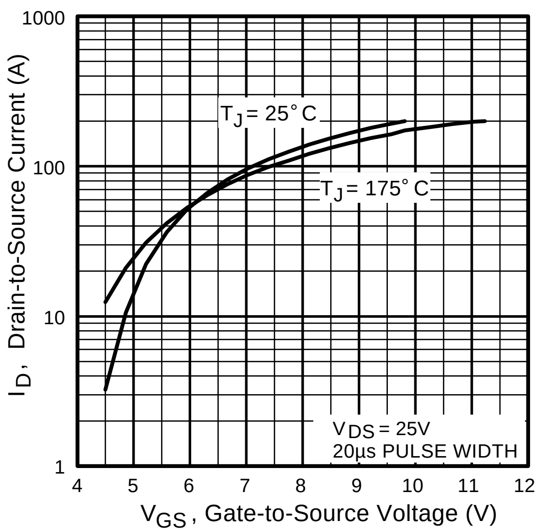


Fig 3. Typical Transfer Characteristics

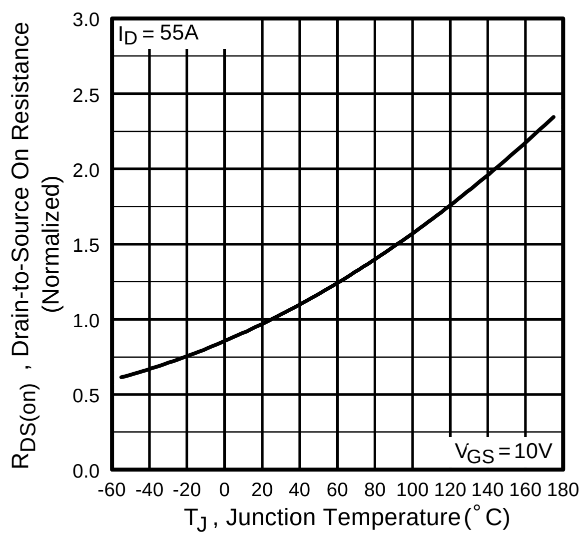


Fig 4. Normalized On-Resistance vs. Temperature

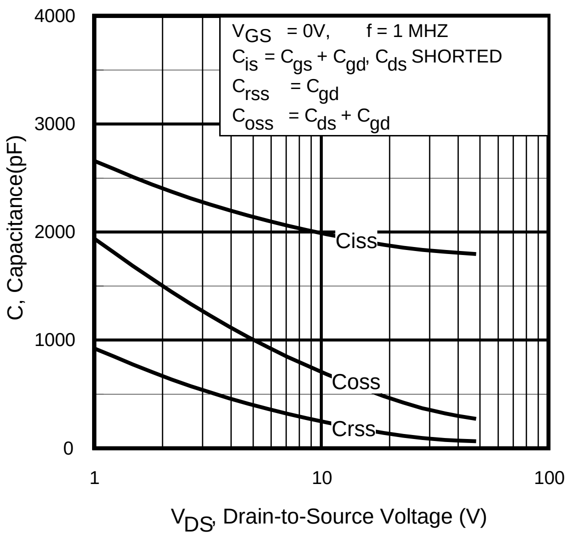


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

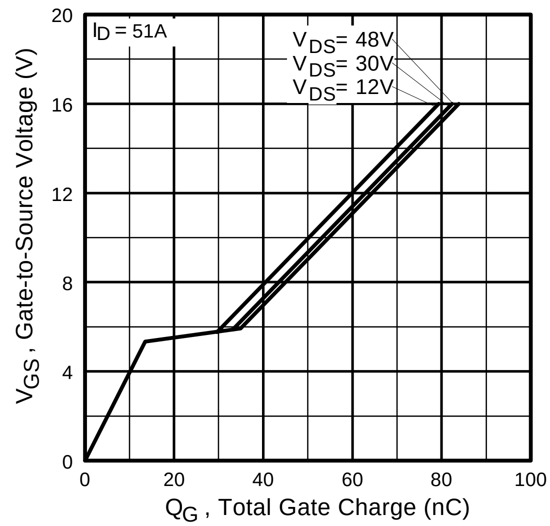


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

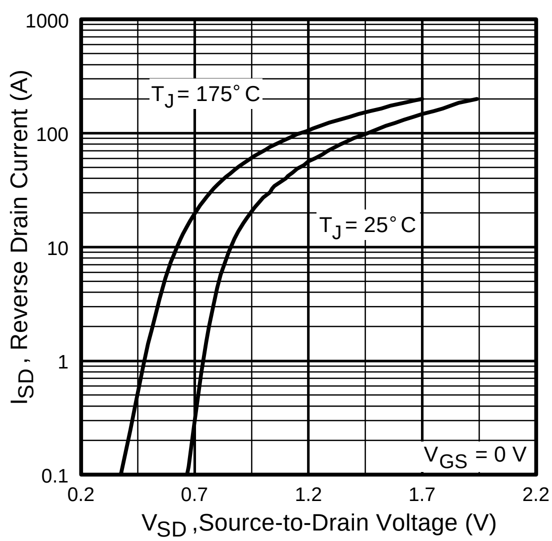


Fig 7. Typical Source-Drain Diode Forward Voltage

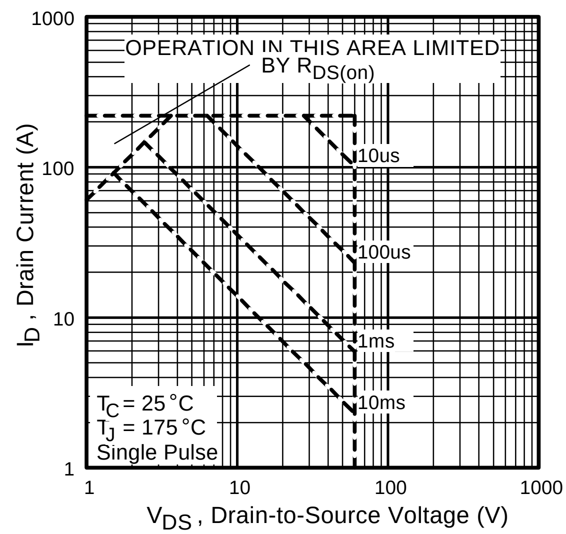


Fig 8. Maximum Safe Operating Area

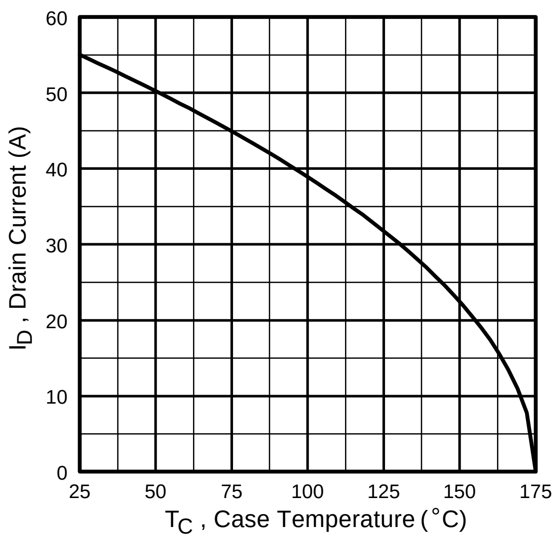


Fig 9. Maximum Drain Current vs. Case Temperature

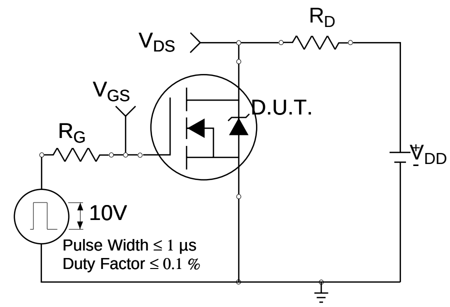


Fig 10a. Switching Time Test Circuit

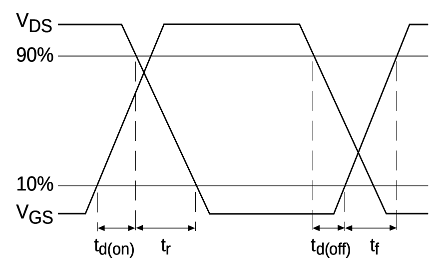


Fig 10b. Switching Time Waveforms

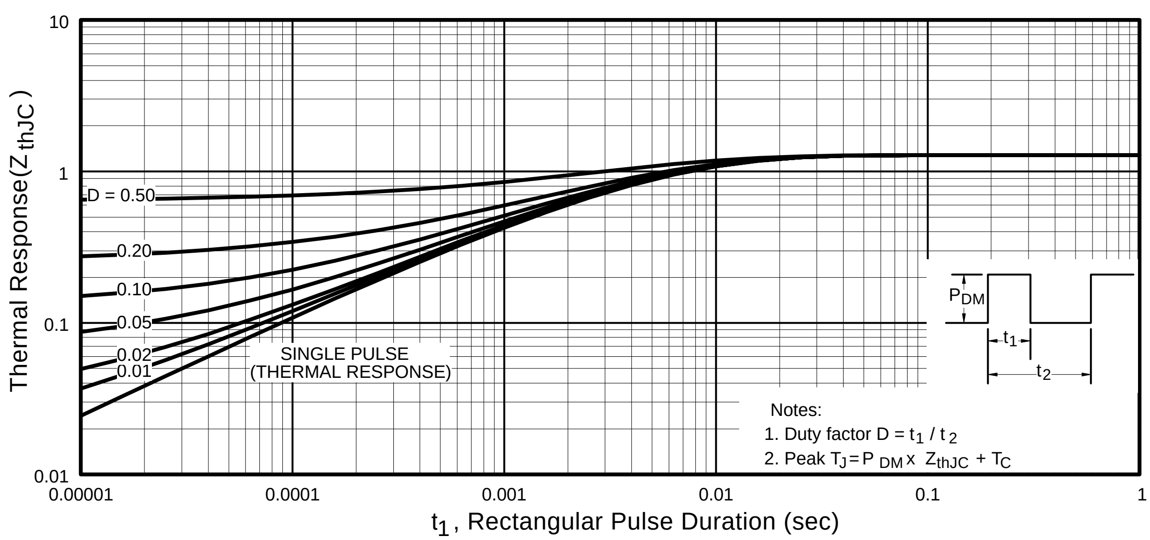


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

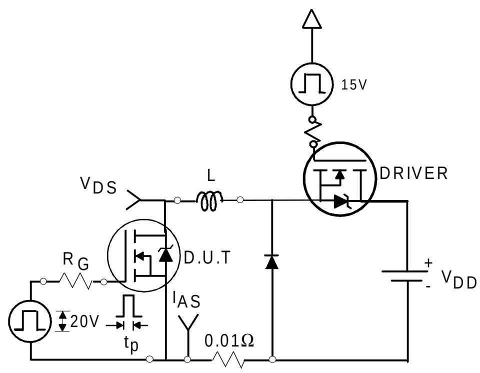


Fig 12a. Unclamped Inductive Test Circuit

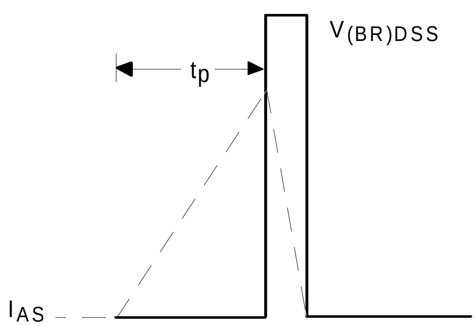


Fig 12b. Unclamped Inductive Waveforms

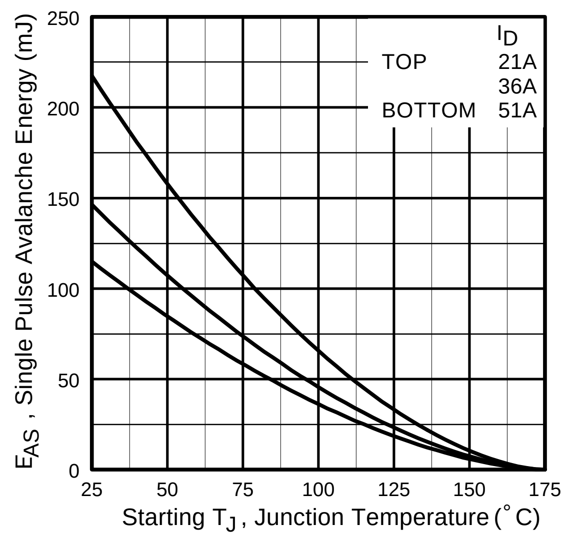


Fig 12c. Maximum Avalanche Energy vs. Drain Current

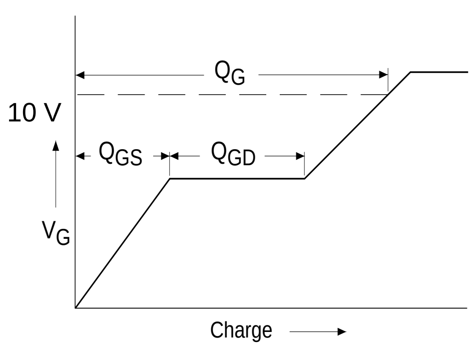


Fig 13a. Basic Gate Charge Waveform

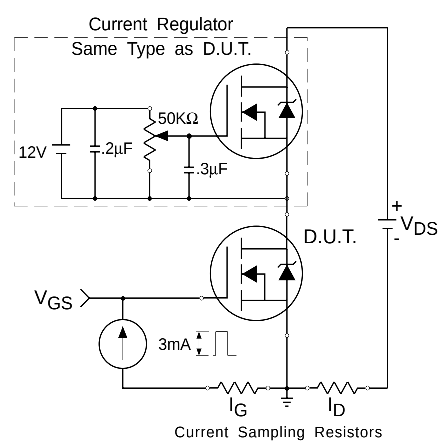
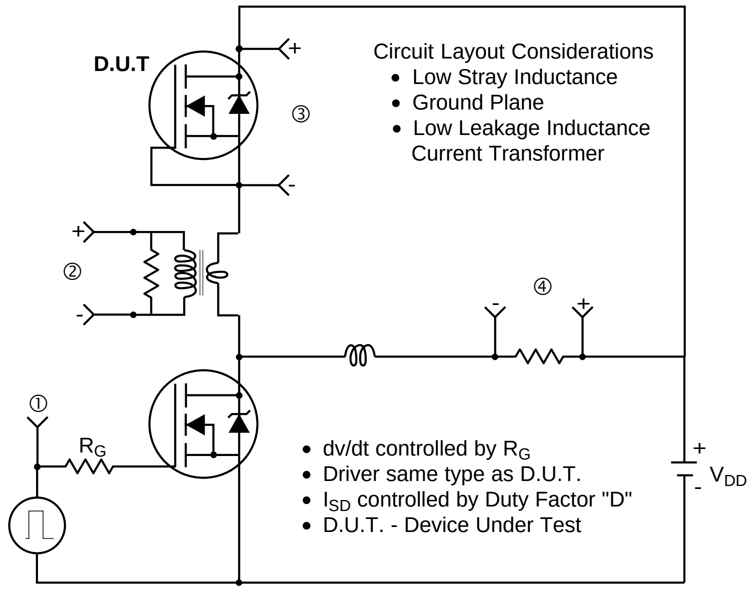
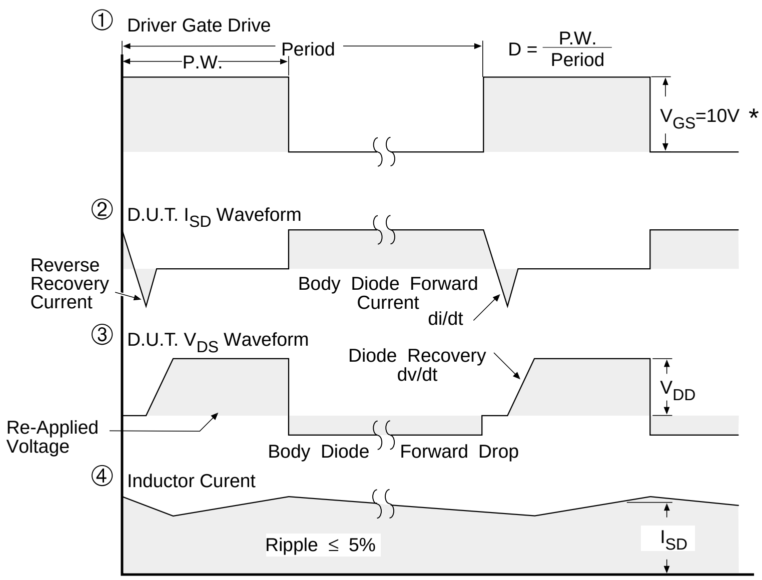


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit





* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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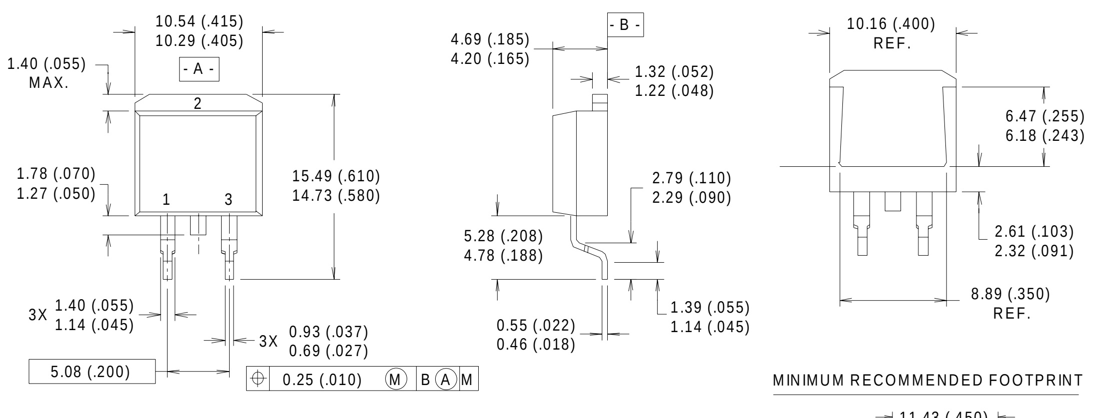
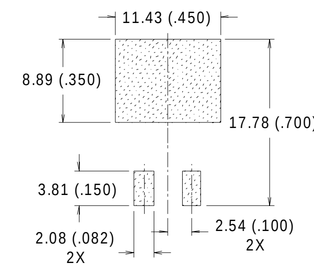
D²Pak Package Outline

Dimensions are shown in millimeters (inches)



MINIMUM RECOMMENDED FOOTPRINT

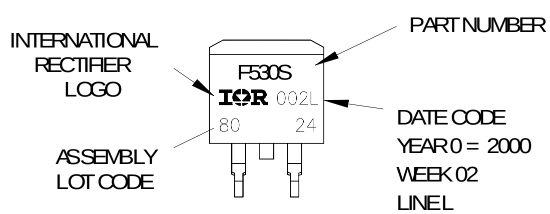


NOTES:
1. DIMENSIONS AFTER SOLDER DIP.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION : INCH.
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

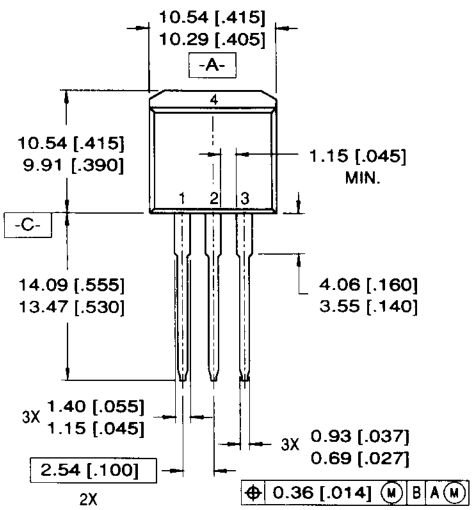
D²Pak Part Marking Information

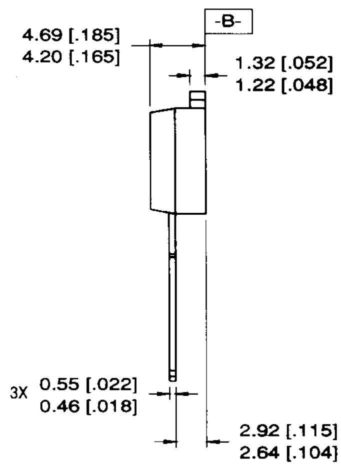
EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"



TO-262 Package Outline

Dimensions are shown in millimeters (inches)





LEAD ASSIGNMENTS

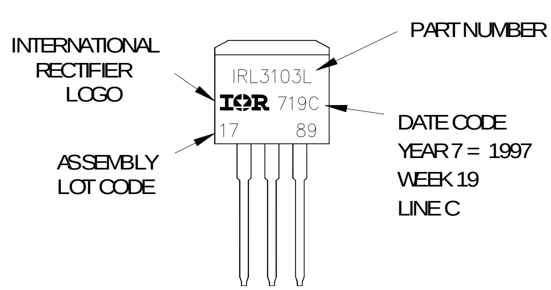
1 = GATE
2 = DRAIN
3 = SOURCE
4 = DRAIN

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

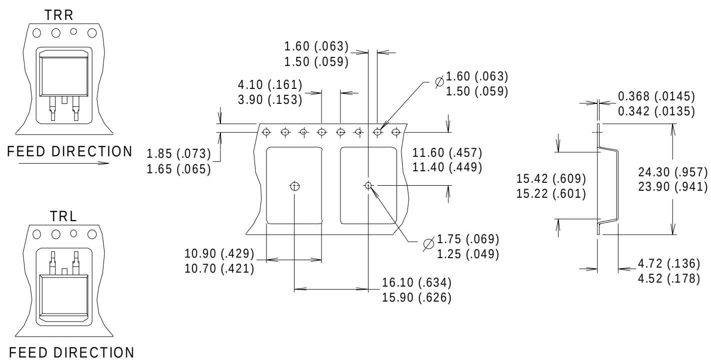
TO-262 Part Marking Information

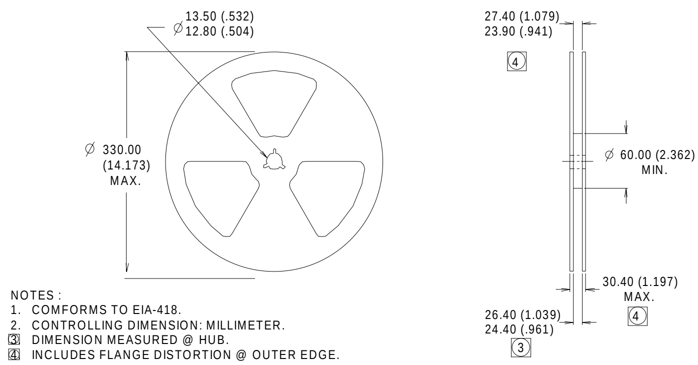
EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)





Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/