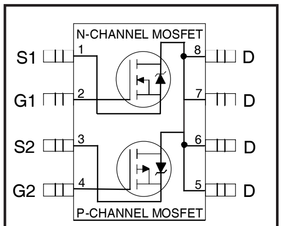
International
IOR Rectifier

PD - 95300

IRF7379PbF

HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Complimentary Half Bridge
- Surface Mount
- Fully Avalanche Rated
- Lead-Free



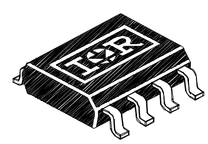
Top View

	N-Ch	P-Ch
V_{DSS}	30V	-30V
$R_{DS(on)}$	0.045Ω	0.090Ω

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques.



SO-8

Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
V_{SD}	Drain-to-Source Voltage	30	-30	A
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	5.8	-4.3	
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	4.6	-3.4	
I_{DM}	Pulsed Drain Current ①	46	-34	
P_D @T_A = 25°C	Power Dissipation	2.5		W
	Linear Derating Factor	0.02		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance Ratings

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient④	50	°C/W

10/7/04

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	V_{GS} = 0V, I_D = 250μA
		P-Ch	-30	—	—		V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.032	—	V/°C	Reference to 25°C, I_D = 1mA
		P-Ch	—	-0.037	—		Reference to 25°C, I_D = -1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	0.038	0.045	Ω	V_{GS} = 10V, I_D = 5.8A ③
			—	0.055	0.075		V_{GS} = 4.5V, I_D = 4.9A ③
		P-Ch	—	0.070	0.090		V_{GS} = -10V, I_D =- 4.3A ③
			—	0.130	0.180		V_{GS} = -4.5V, I_D =- 3.7A ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	—	V	V_{DS} = V_{GS}, I_D = 250μA
		P-Ch	-1.0	—	—		V_{DS} = V_{GS}, I_D = -250μA
g_{fs}	Forward Transconductance	N-Ch	5.2	—	—	S	V_{DS} = 15V, I_D = 2.4A ③
		P-Ch	2.5	—	—		V_{DS} = -24V, I_D = -1.8A ③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	V_{DS} = 24 V, V_{GS} = 0V
		P-Ch	—	—	-1.0		V_{DS} = -24V, V_{GS} = 0V
		N-Ch	—	—	25		V_{DS} = 24 V, V_{GS} = 0V, T_J = 125°C
		P-Ch	—	—	-25		V_{DS} = -24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	±100		V_{GS} = ± 20V
Q_g	Total Gate Charge	N-Ch	—	—	25	nC	N-Channel I_D = 2.4A, V_{DS} = 24V, V_{GS} = 10V ③ P-Channel I_D = -1.8A, V_{DS} = -24V, V_{GS} = -10V
		P-Ch	—	—	25		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	—	2.9		
		P-Ch	—	—	2.9		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	—	7.9		
		P-Ch	—	—	9.0		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	6.8	—	ns	N-Channel V_{DD} = 15V, I_D = 2.4A, R_G = 6.0Ω, R_D = 6.2Ω ③ P-Channel V_{DD} = -15V, I_D = -1.8A, R_G = 6.0Ω, R_D = 8.2Ω
		P-Ch	—	11	—		
t_r	Rise Time	N-Ch	—	21	—		
		P-Ch	—	17	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	22	—		
		P-Ch	—	25	—		
t_f	Fall Time	N-Ch	—	7.7	—		
		P-Ch	—	18	—		
L_D	Internal Drain Inductace	N-P	—	4.0	—	nH	Between lead, 6mm (0.25in.) from
L_S	Internal Source Inductance	N-P	—	6.0	—		package and center of die contact
C_{iss}	Input Capacitance	N-Ch	—	520	—	pF	N-Channel V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz ③ P-Channel V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz
		P-Ch	—	440	—		
C_{oss}	Output Capacitance	N-Ch	—	180	—		
		P-Ch	—	200	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	72	—		
		P-Ch	—	93	—		

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	3.1	A	
		P-Ch	—	—	-3.1		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	46		
		P-Ch	—	—	-34		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.0	V	T_J = 25°C, I_S = 1.8A, V_{GS} = 0V ③
		P-Ch	—	—	-1.0		T_J = 25°C, I_S = -1.8A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	N-Ch	—	47	71	ns	N-Channel T_J = 25°C, I_F = 2.4A, di/dt = 100A/μs P-Channel ③ T_J = 25°C, I_F = -1.8A, di/dt = -100A/μs
		P-Ch	—	53	80		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	56	84	nC	
		P-Ch	—	66	99		

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 10)

② N-Channel $I_{SD} \le$ 2.4A, di/dt $\le$ 73A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 150°C
P-Channel $I_{SD} \le$ -1.8A, di/dt $\le$ 90A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 150°C

③ Pulse width $\le$ 300μs; duty cycle $\le$ 2%.

④ Surface mounted on FR-4 board, t $\le$ 10sec.

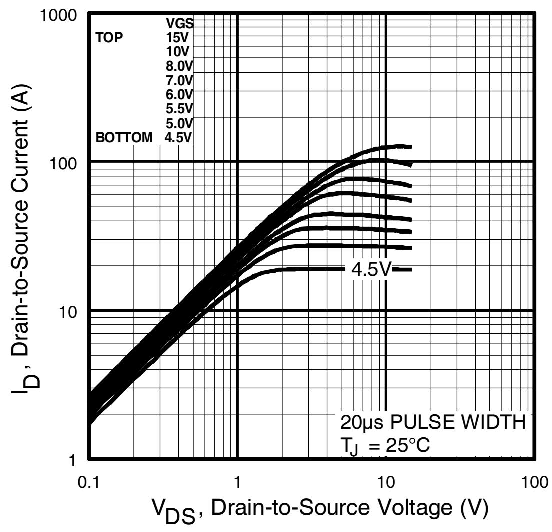


Fig 1. Typical Output Characteristics

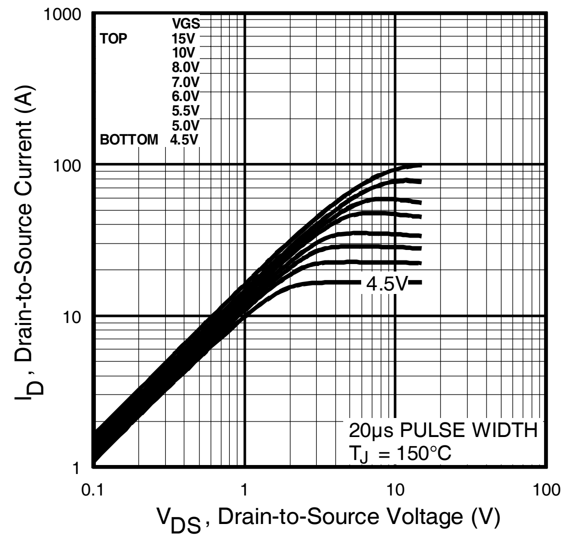


Fig 2. Typical Output Characteristics

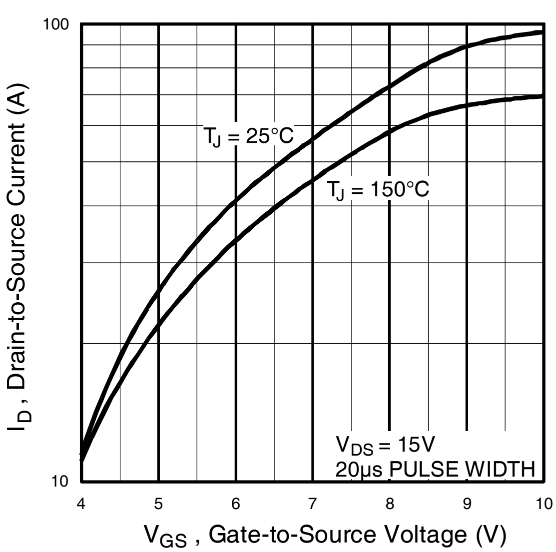


Fig 3. Typical Transfer Characteristics

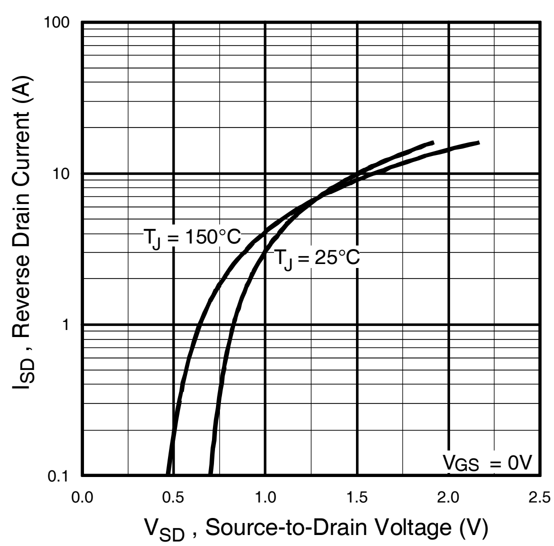


Fig 4. Typical Source-Drain Diode Forward Voltage

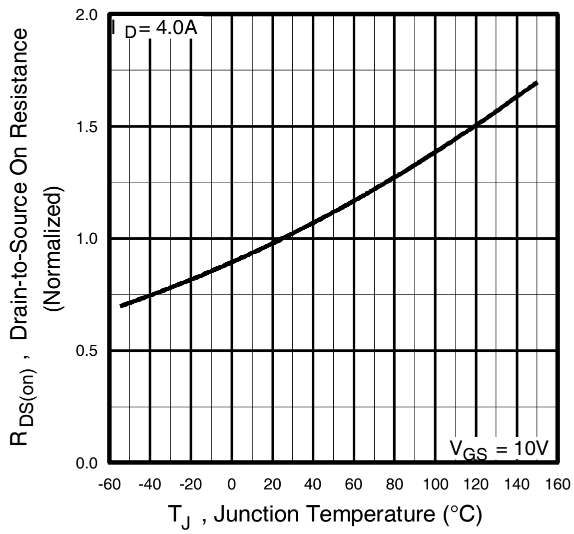


Fig 5. Normalized On-Resistance Vs. Temperature

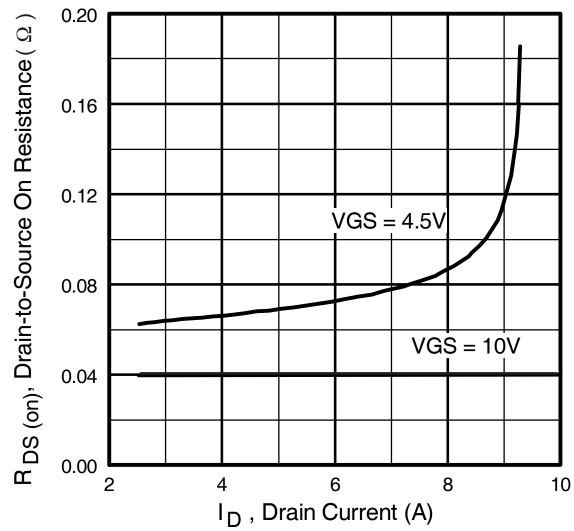


Fig 6. Typical On-Resistance Vs. Drain Current

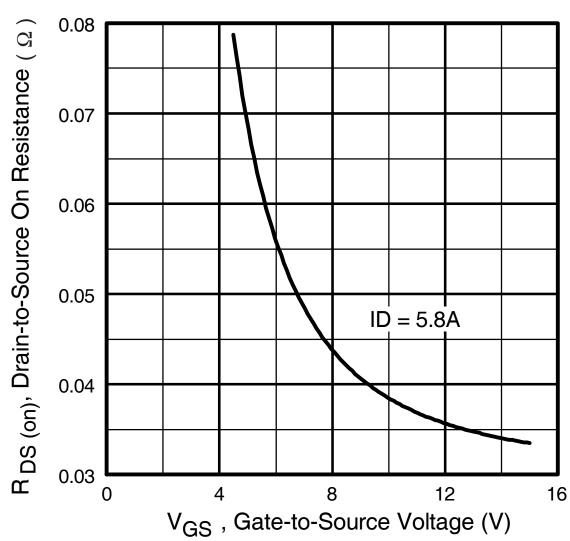


Fig 7. Typical On-Resistance Vs. Gate Voltage

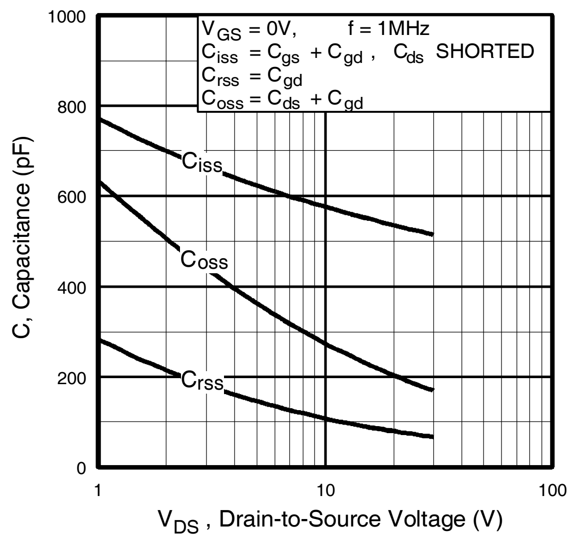


Fig 8. Typical Capacitance Vs. Drain-to-Source Voltage

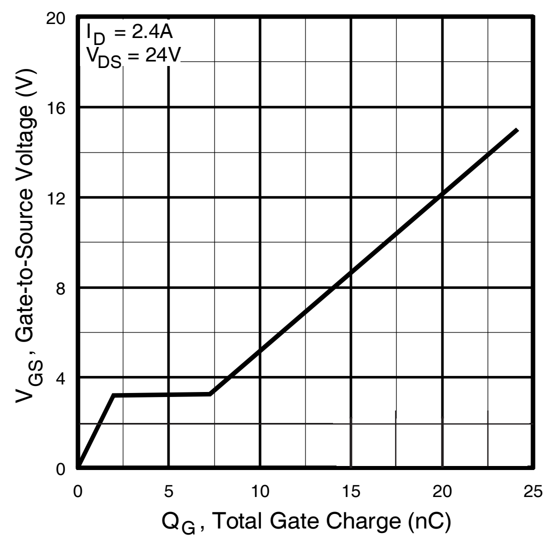


Fig 9. Typical Gate Charge Vs. Gate-to-Source Voltage

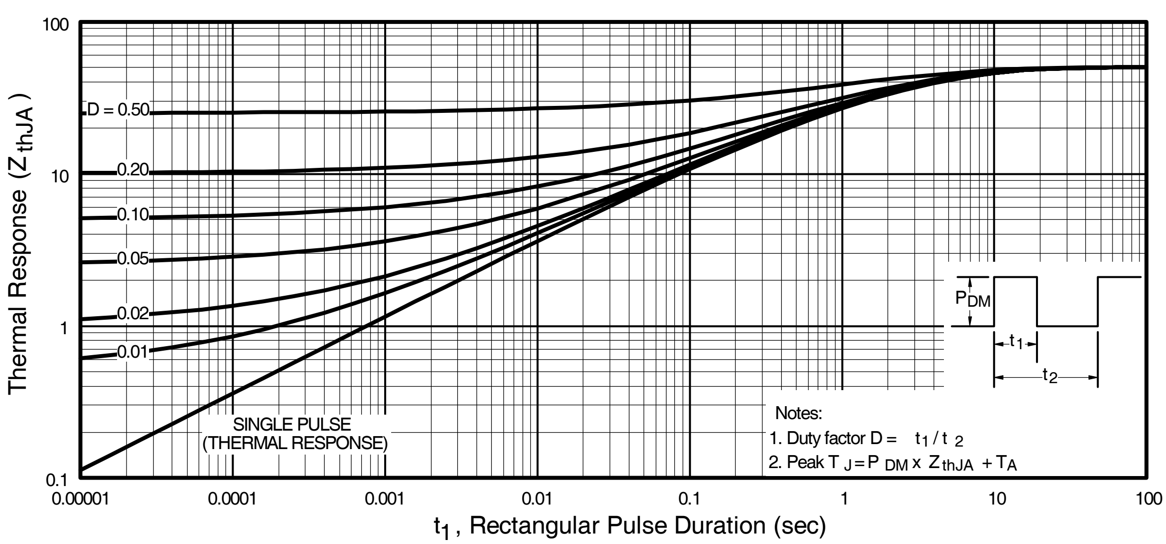


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

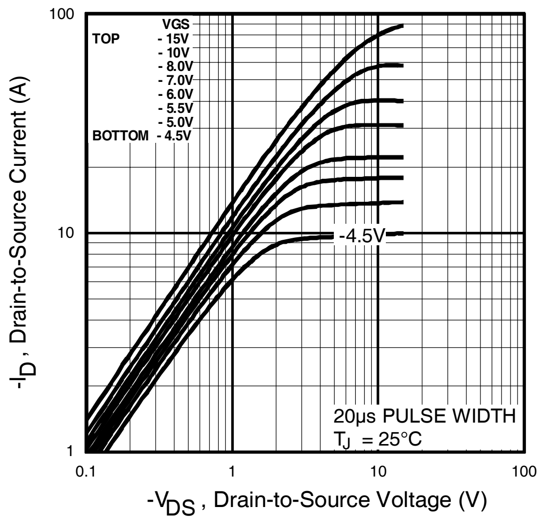


Fig 11. Typical Output Characteristics

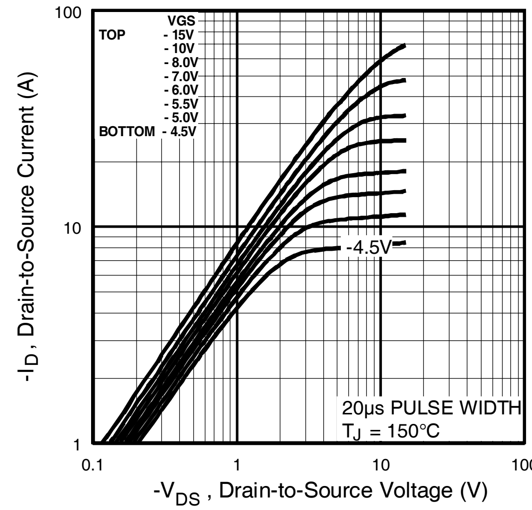


Fig 12. Typical Output Characteristics

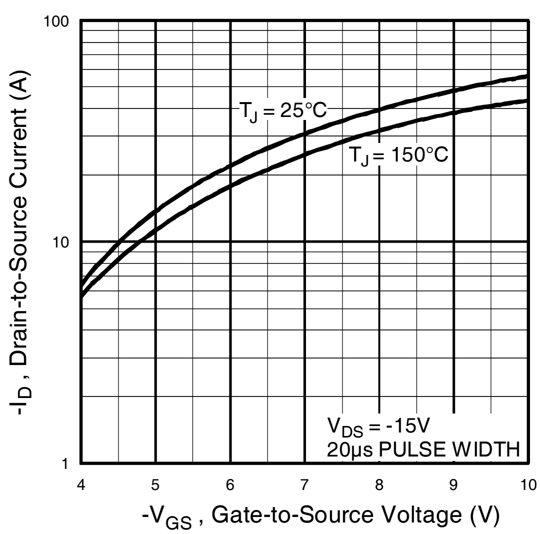


Fig 13. Typical Transfer Characteristics

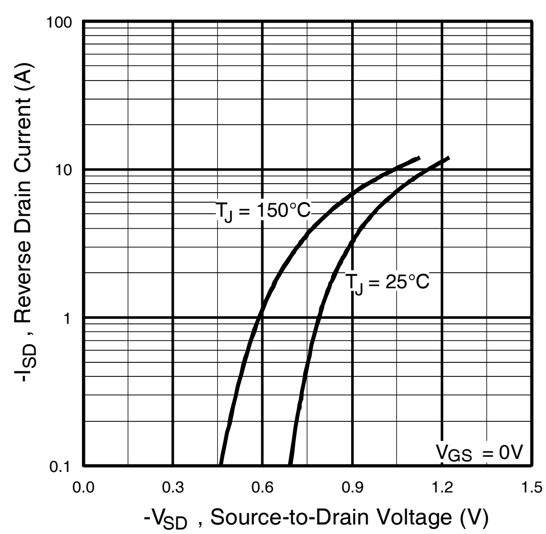


Fig 14. Typical Source-Drain Diode Forward Voltage

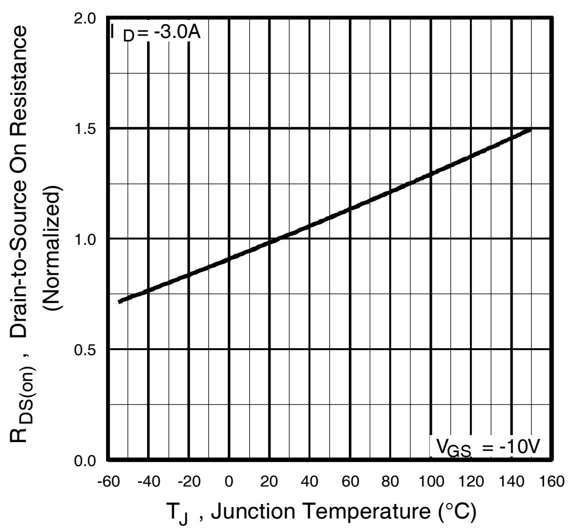


Fig 15. Normalized On-Resistance Vs. Temperature

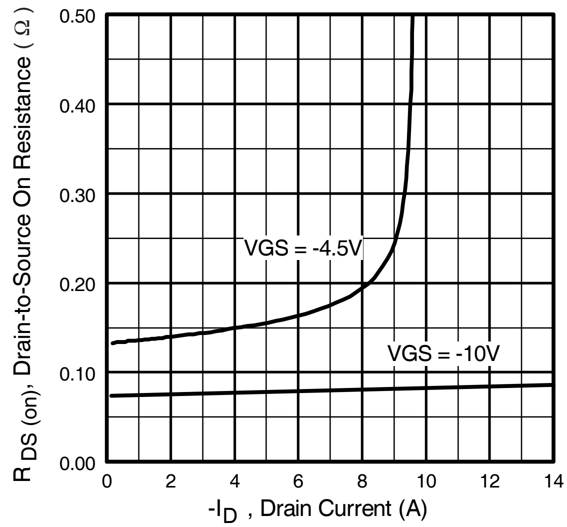


Fig 16. Typical On-Resistance Vs. Drain Current

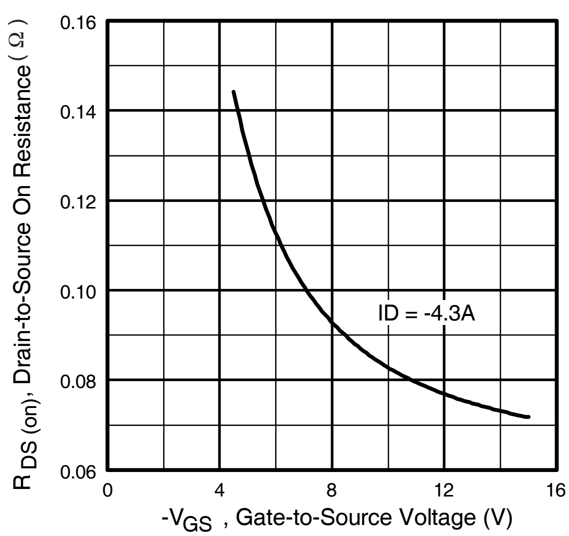


Fig 17. Typical On-Resistance Vs. Gate Voltage

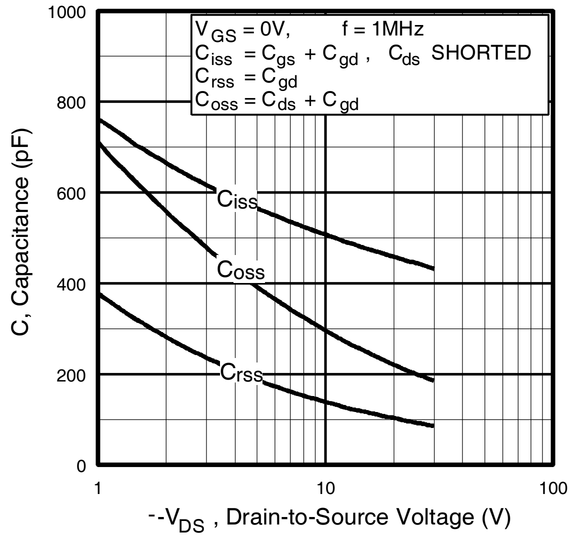


Fig 18. Typical Capacitance Vs. Drain-to-Source Voltage

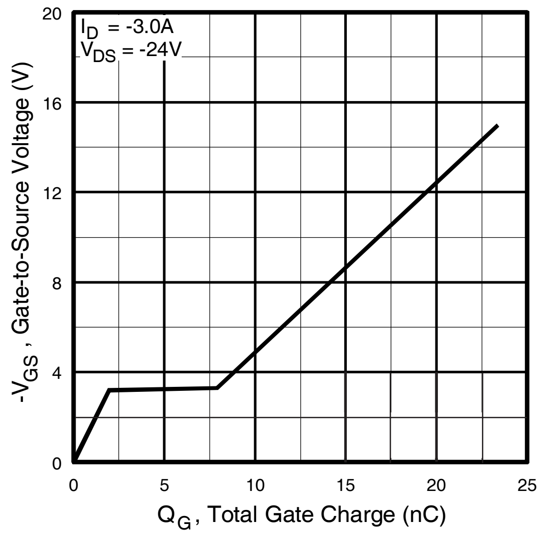


Fig 19. Typical Gate Charge Vs. Gate-to-Source Voltage

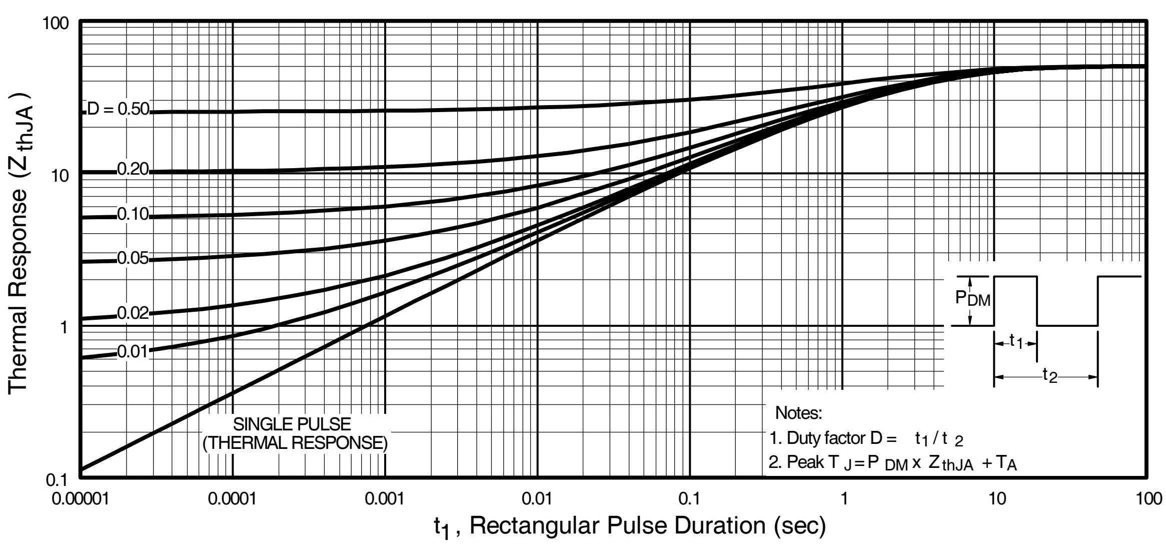
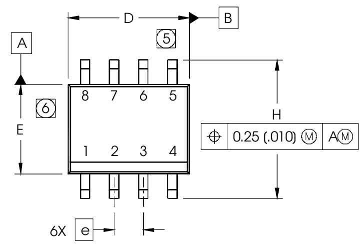


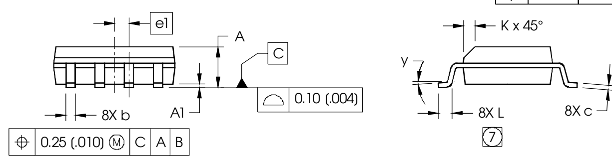
Fig 20. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

SO-8 Package Outline

Dimensions are shown in milimeters (inches)

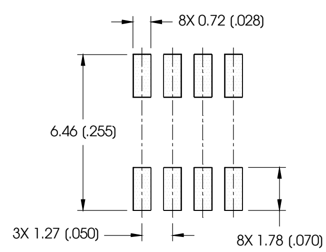


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



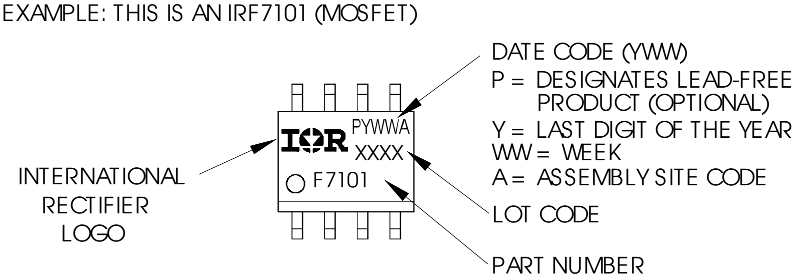
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



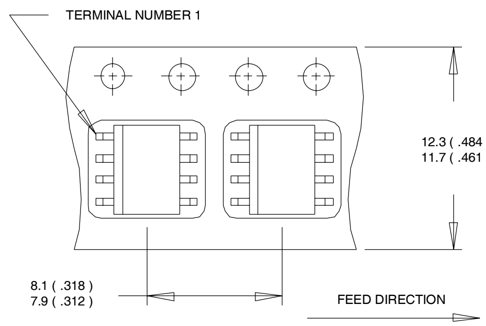
SO-8 Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

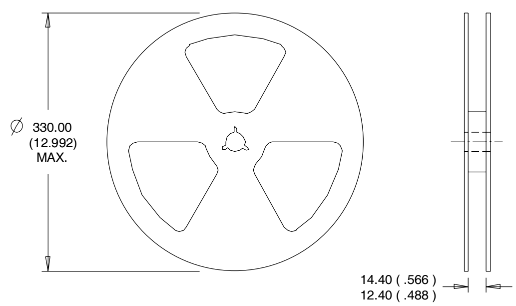


SO-8 Tape and Reel

Dimensions are shown in milimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.

International
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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.10/04