International
IOR Rectifier

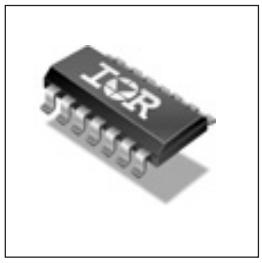
PD- 94546

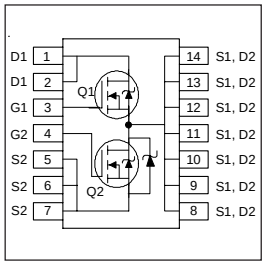
IRF7335D1

- Co-Pack Dual N-channel HEXFET® Power MOSFET and Schottky Diode
- Ideal for Synchronous Buck DC-DC Converters Up to 11A Peak Output
- Low Conduction Losses
- Low Switching Losses
- Low Vf Schottky Rectifier

Dual FETKY™

Co-Packaged Dual MOSFET Plus Schottky Diode





Device Ratings (Typ.Values)

	Q1	Q2 and Schottky
$R_{DS(on)}$	13.4 mΩ	9.6 mΩ
Q_G	13 nC	18 nC
Q_{sw}	5.5 nC	6.4 nC
V_{SD}	1.0V	0.43V

Description

The FETKY™ family of Co-Pack HEXFET®MOSFETs and Schottky diodes offers the designer an innovative, board space saving solution for switching regulator and power management applications. Advanced HEXFET®MOSFETs combined with low forward drop Schottky results in an extremely efficient device suitable for a wide variety of portable electronics applications.

The SO-14 has been modified through a customized leadframe for enhanced thermal characteristics and multiple die capability making it ideal in a variety of power applications. With these improvements multiple devices can be used in an application with dramatically reduced board space. Internal connections enable easier board layout design with reduced stray inductance.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	30	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V④	10	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V④	8.1	
I_{DM}	Pulsed Drain Current ①	81	
P_D @T_A = 25°C	Power Dissipation ③	2.0	W
P_D @T_A = 70°C	Power Dissipation③	1.3	
	Linear Derating Factor	0.02	W/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
E_{AS} (6 sigma)	Single Pulse Avalanche Energy ⑤	50	mJ
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead		20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ③		62.5	

Notes ① through ⑤ are on page 12

Electrical Characteristics

Parameter		Q1-Control FET Min	Q1-Control FET Typ	Q1-Control FET Max	Q2-Synch FET & Schottky Min	Q2-Synch FET & Schottky Typ	Q2-Synch FET & Schottky Max	Units	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	30			30			V	V_{GS} = 0V, I_D = 250µA
Breakdown Voltage Tem. Coefficient	$\Delta BV_{DSS}/\Delta T_J$	0.025			0.033			V	Reference to 25°C, I_D = 1.0mA
Static Drain-Source on Resistance	$R_{DS(on)}$		13.4	17.5		9.6	12.8	mΩ	V_{GS} = 4.5V, I_D = 10A②
Gate Threshold Voltage	$V_{GS(th)}$	1.0			1.1			V	V_{DS} = V_{GS},I_D = 250µA
Drain-Source Leakage Current	I_{DSS}			30			30	µA	V_{DS} = 24V, V_{GS} = 0
				0.3			10	mA	V_{DS} = 24V, V_{GS} = 0, Tj = 125°C
Gate-Source Leakage Current	I_{GSS}			±100			±100	nA	V_{GS} = ±12V
Forward Transconductance	g_{FS}	21			28			S	V_{GS}=5V, I_D=8.0A, V_{DS}=15V
Total Gate Charge	Q_G		13	20		18	27	nC	V_{GS}=4.5V, I_D=8.0A, V_{DS}=15V
Pre-Vth Gate-Source Charge	Q_{GS1}		3.2			5.8			
Post-Vth Gate-Source Charge	Q_{GS2}		1.4			1.5			
Gate to Drain Charge	Q_{GD}		4.1			4.9			
Switch Chg(Q_{gs2} + Q_{gd})	Q_{sw}		5.5			6.4			
Output Charge	Q_{oss}		7.7			11		nC	V_{DS} = 16V, V_{GS} = 0
Gate Resistance	R_G		4.3	10		2.6	5.0	Ω	
Turn-on Delay Time	$t_{d(on)}$		6.8			8.8		ns	V_{DD} = 16V, I_D = 8.0A
Rise Time	t_r		5.9			3.3			V_{GS} = 4.5V
Turn-off Delay Time	$t_{d(off)}$		19			17			Clamped Inductive Load
Fall Time	t_f		9.1			7.0			
Input Capacitance	C_{iss}		1500			2300			
Output Capacitance	C_{oss}		310			450		pF	V_{DS} = 15V, V_{GS} = 0
Reverse Transfer Capacitance	C_{rss}		140			180			

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Min	Typ	Max	Units	Conditions
Continuous Source Current (Body Diode)	I_S			10			10	A	MOSFET symbol showing the
Pulse Source Current (Body Diode)	I_{SM}			81			81		intergral reverse p-n junction diode
Diode Forward Voltage	V_{SD}		1	1.25		0.43	0.50	V	T_J = 25°C, I_S = 1.0A,V_{GS}= 0V
Reverse Recovery Time	t_{rr}		28			31		ns	T_J = 125°C, I_F = 8.0A, V_R= 15V
Reverse Recovery Charge	Q_{rr}		24			26		nC	di/dt = 100A/µs
Reverse Recovery Time	t_{rr}		29			31		ns	T_J = 125°C, I_F =8.0A, V_R= 15V
Reverse Recovery Charge	Q_{rr}		26			26		nC	di/dt =100A/µs

Typical Characteristics

Q1 - Control FET

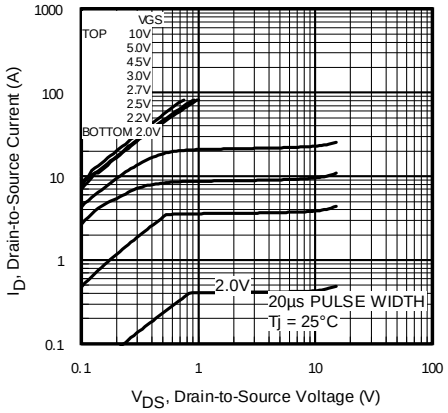


Fig 1. Typical Output Characteristics

Q2 - Synchronous FET & Schottky

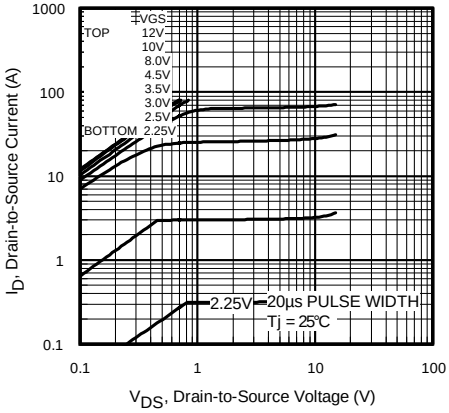


Fig 2. Typical Output Characteristics

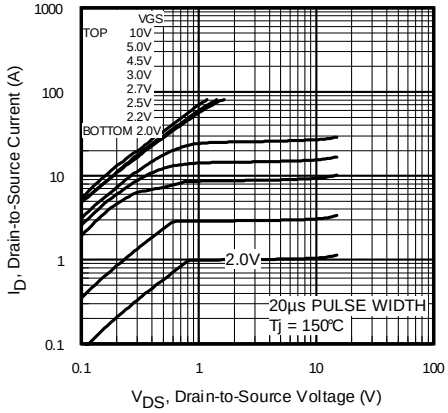


Fig 3. Typical Output Characteristics

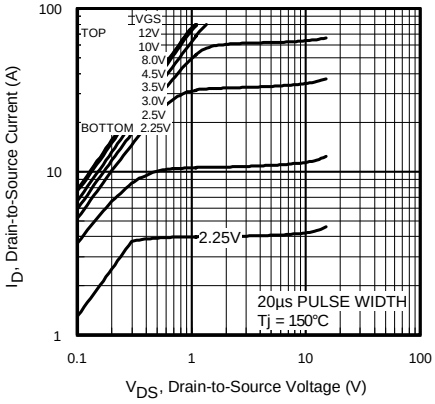


Fig 4. Typical Output Characteristics

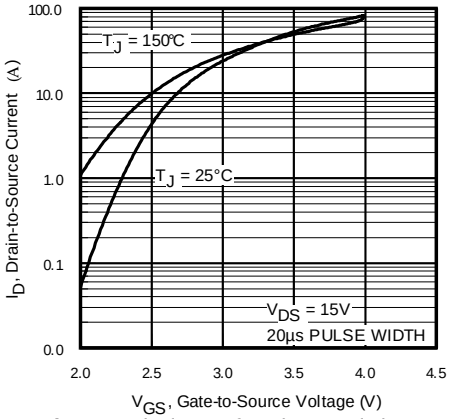


Fig 5. Typical Transfer Characteristics

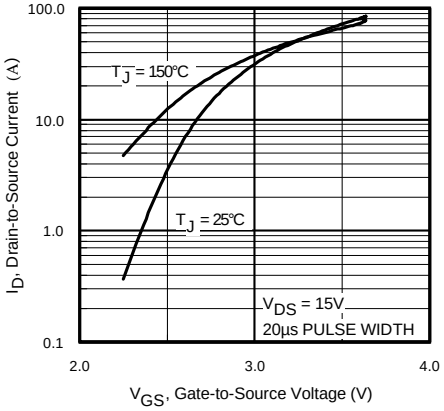


Fig 6. Typical Transfer Characteristics

Typical Characteristics

Q1 - Control FET

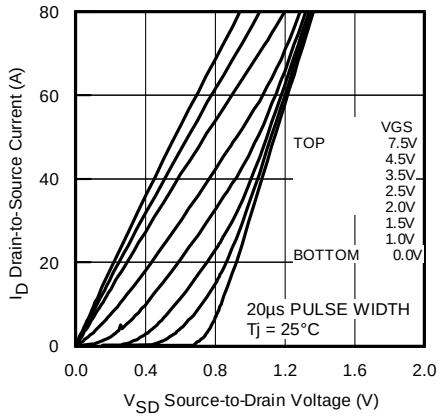


Fig. 7. Typical Reverse Output Characteristics

Q2 - Synchronous FET & Schottky

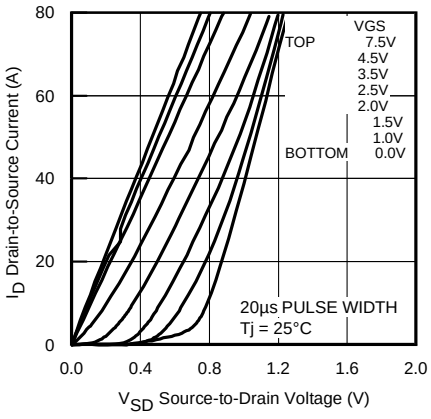


Fig. 8. Typical Reverse Output Characteristics

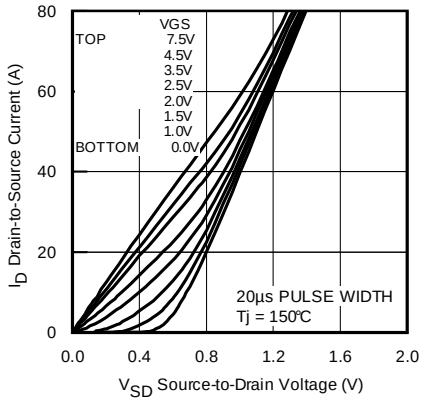


Fig. 9. Typical Reverse Output Characteristics

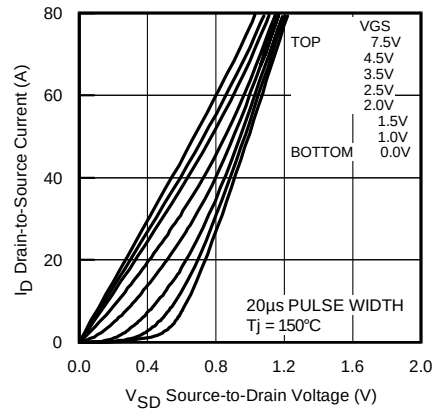


Fig. 10. Typical Reverse Output Characteristics

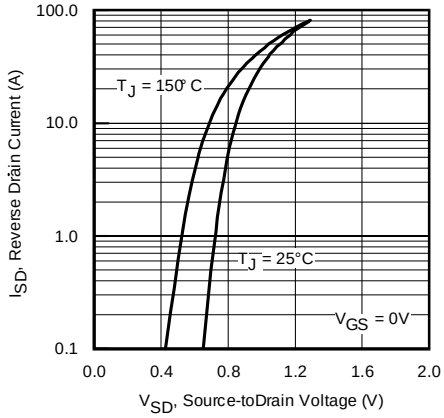


Fig 11. Typical Source-Drain Diode Forward Voltage

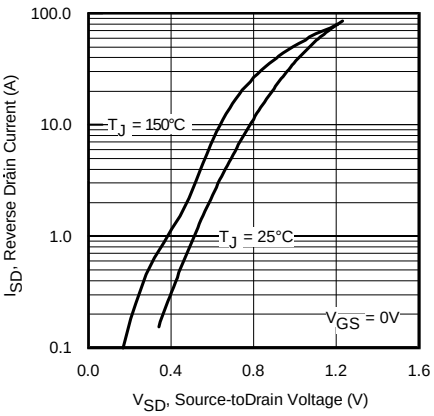


Fig 12. Typical Source-Drain Diode Forward Voltage

Typical Characteristics

Q1 - Control FET

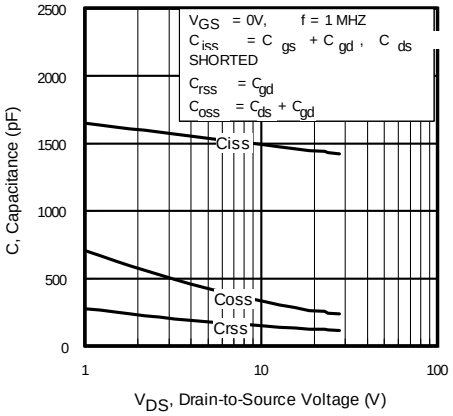


Fig 13. Typical Capacitance Vs.Drain-to-Source Voltage

Q2 - Synchronous FET & Schottky

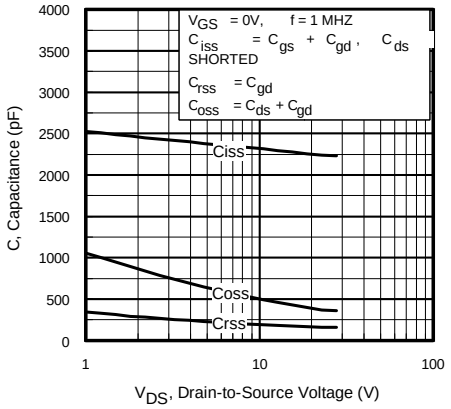


Fig 14. Typical Capacitance Vs.Drain-to-Source Voltage

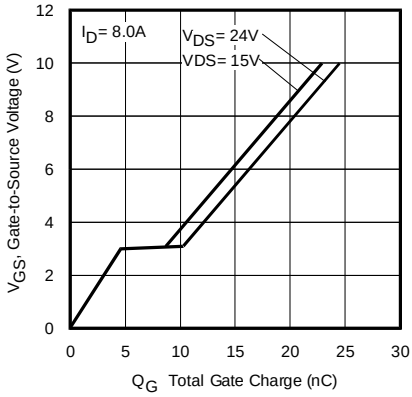


Fig. 15. Gate-to-Source Voltage vs Typical Gate Charge

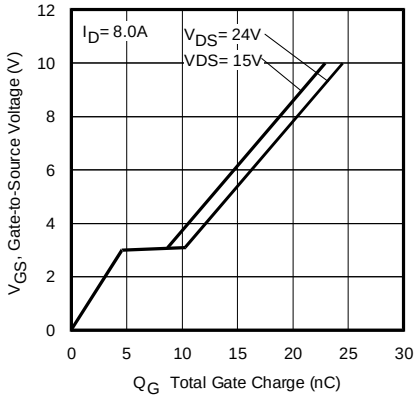


Fig. 16. Gate-to-Source Voltage vs Typical Gate Charge

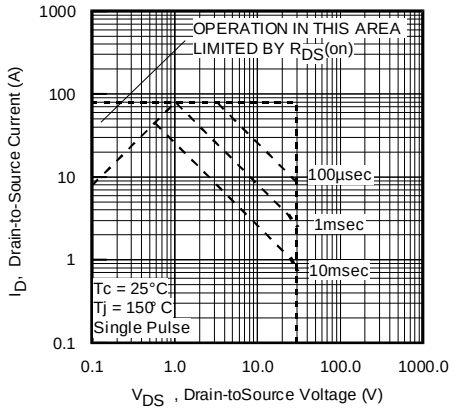


Fig 17. Maximum Safe Operating Area

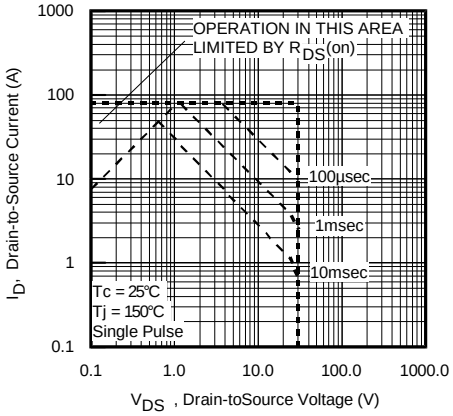


Fig 18. Maximum Safe Operating Area

Q1 - Control FET

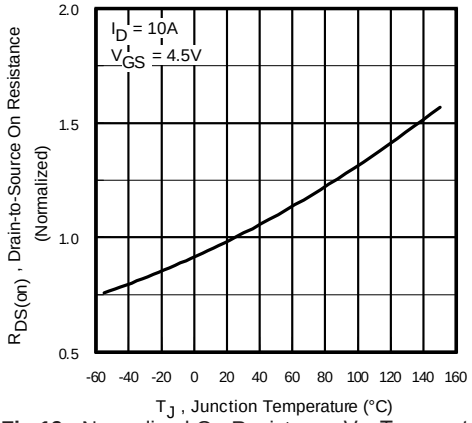


Fig 19. Normalized On-Resistance Vs. Temperature

Q2 - Synchronous FET & Schottky

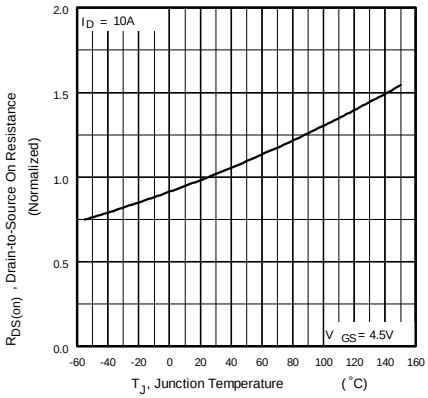


Fig 20. Normalized On-Resistance Vs. Temperature

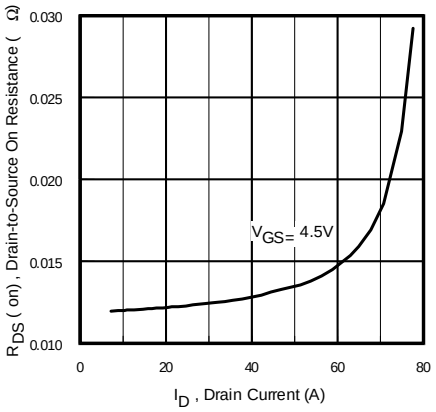


Fig 21. Typical On-Resistance Vs. Drain Current

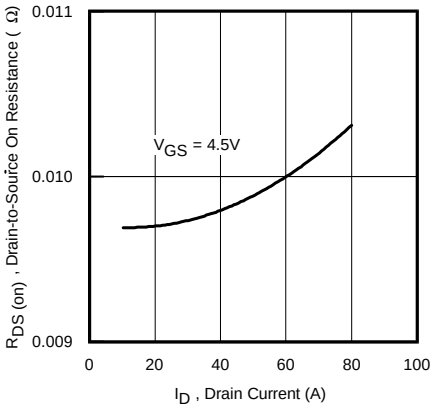


Fig 22. Typical On-Resistance Vs. Drain Current

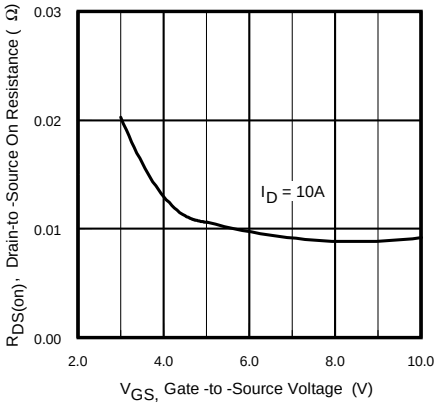


Fig 23. Typical On-Resistance Vs. Gate Voltage

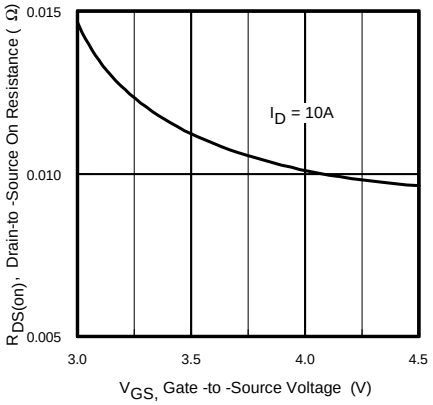


Fig 24. Typical On-Resistance Vs. Gate Voltage

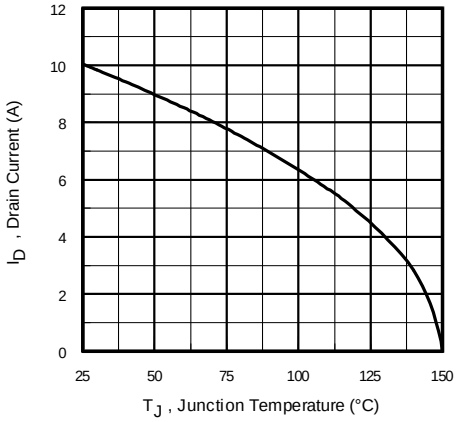


Fig 25. Maximum Drain Current Vs.CaseTemperature

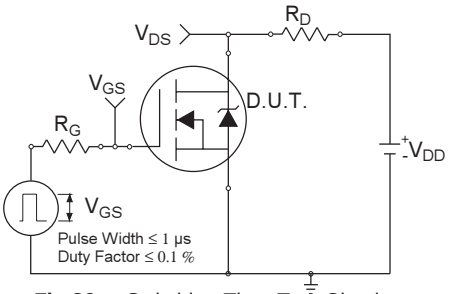


Fig 26a. Switching Time Test Circuit

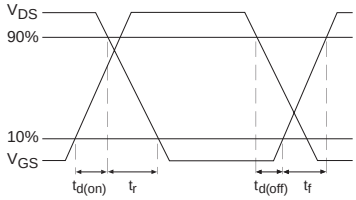


Fig 26b. Switching Time Waveforms

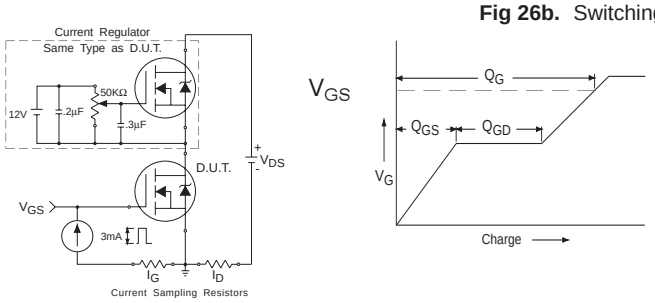


Fig 27a&b. Basic Gate Charge Test Circuit and Waveform

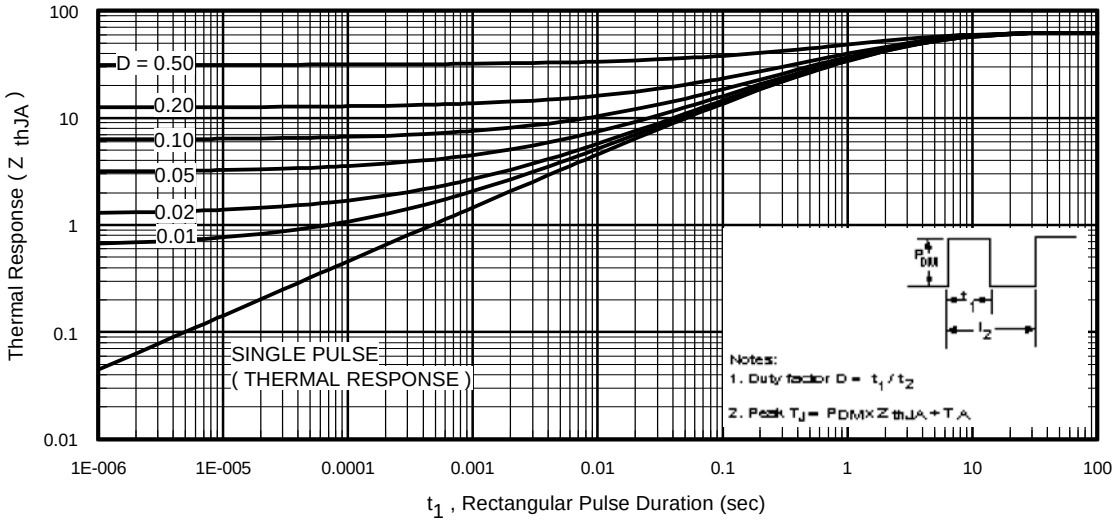


Fig. 28. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Schottky Diode Characteristics

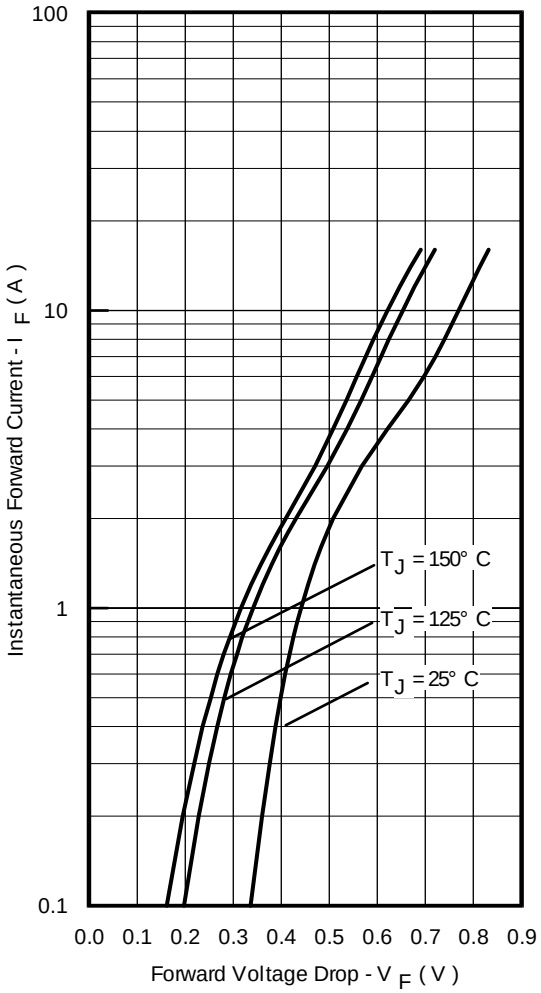


Fig. 29 - Maximum Forward Voltage Drop Characteristics

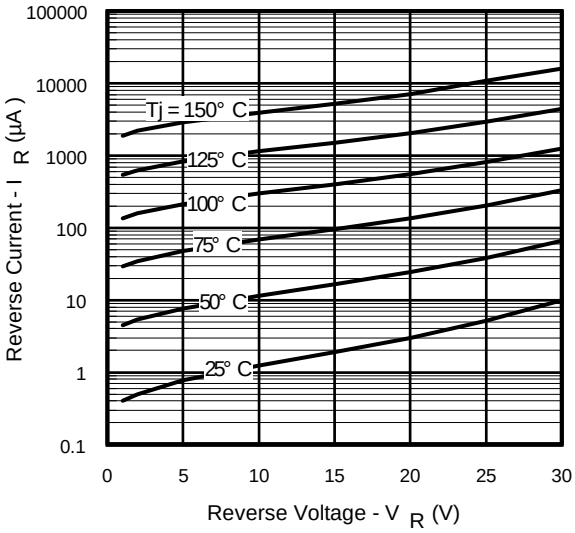


Fig. 30 - Typical Values of Reverse Current Vs. Reverse Voltage

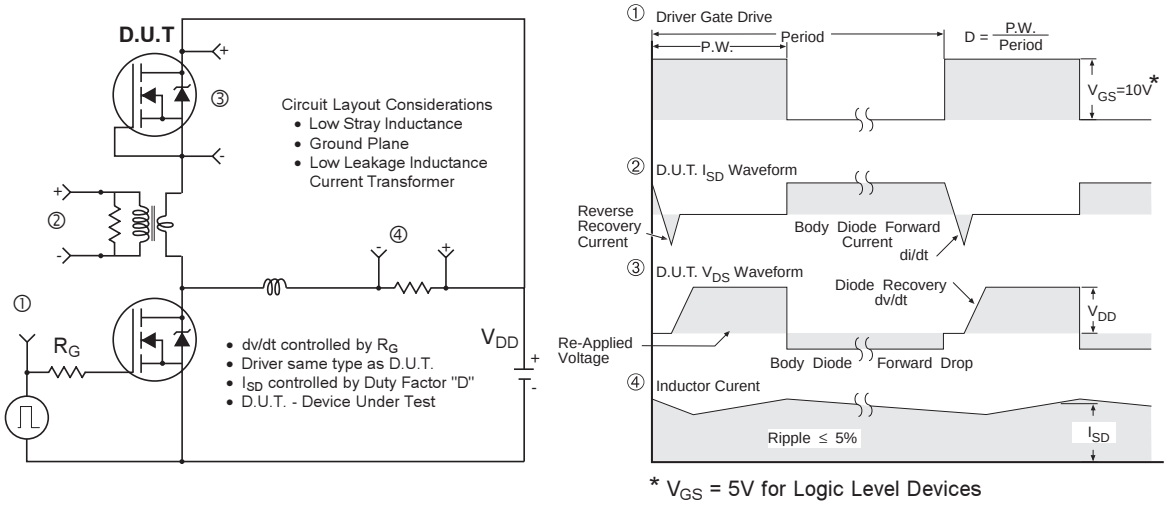


Fig. 31 Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

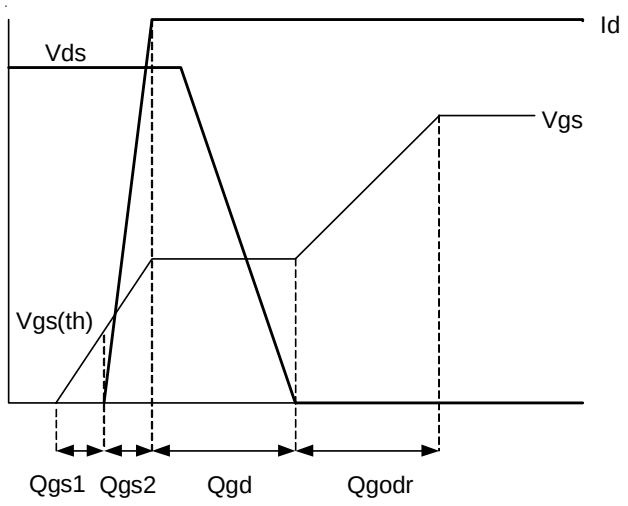


Fig. 32 Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}^{\ 2} \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P^{*}_{output}$$

$$P_{loss} = \left(I_{rms}^{\ 2} \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

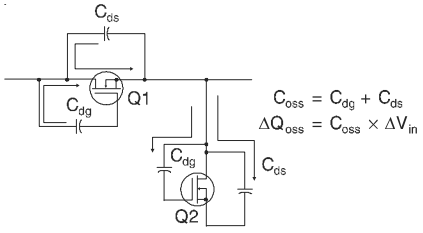
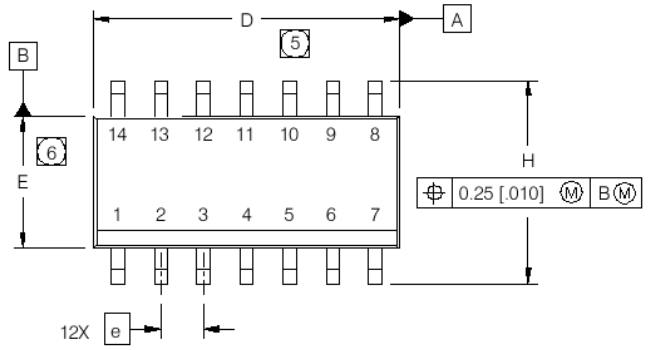
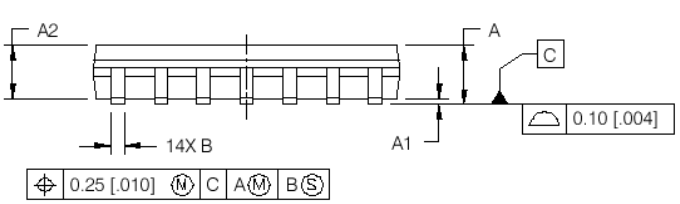


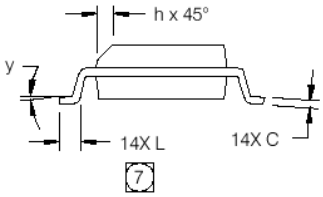
Figure A: Q_{oss} Characteristic

SO-14 Package Details



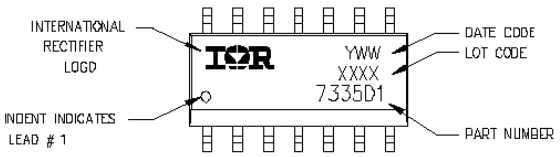
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.127	0.25
A2	.055	.061	1.40	1.55
B	.0138	.0192	0.35	0.49
C	.0075	.0098	0.19	0.25
D	.337	.344	8.58	8.74
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
y	0°	8°	0°	8°





SO-14 Part Marking

2. DEVICE MARKING SHALL NOT EXHIBIT MISSING OR INCOMPLETE CHARACTERS WHICH IMPEDE LEGIBILITY.
3. ALL MARKING SHALL BE ALIGNED TO THE CENTER OF THE DEVICE. OTHERWISE, THE MARKING SHALL, AS A MINIMUM, RETAIN ITS COMPLETE LEGIBILITY.
4. DEVICES SHALL BE CAPABLE OF PASSING A MARKING PERMANENCY TEST (ACETONE FOR 5 MINUTES OR EQUIVALENT TEST). FAILURE CRITERIA: AFTER SUBJECTION TO THE TEST, SPECIFIED MARKING WHICH ARE MISSING IN WHOLE OR IN PART, FADED, SMEARED, BLURRED, OR DISLODGED TO THE EXTENT THAT THEY CANNOT READILY BE IDENTIFIED FROM A MINIMUM DISTANCE OF 15 cm (6") WITH NORMAL ROOM LIGHTING AND WITHOUT THE AID OF MAGNIFICATION OR WITH A VIEWER HAVING 0–3X MAGNIFICATION, SHALL CONSTITUTE FAILURE.
5. TOP MARKING SHALL INCLUDE THE FOLLOWING:
   5.1) IR LOGO
   5.2) DATE CODE (YWW)
   Y = LAST DIGIT OF CALENDAR YEAR
   WW = WEEK OF MOLDING
   5.3) XXXX = LOT CODE
   5.4) PART NUMBER: 7335D1



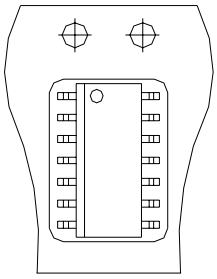
TOP MARKING

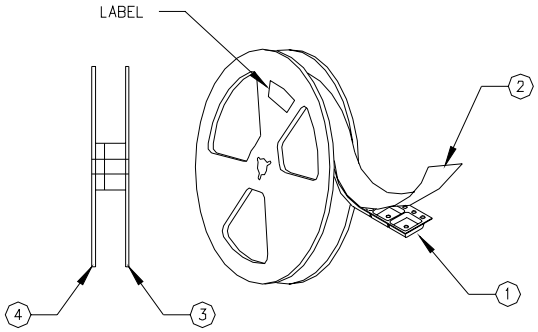
SO-14 Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
   - 1.1 REEL SIZE 13 INCH DIAMETER.
   - 1.2 EACH REEL CONTAINING 4,000 DEVICES.
   - 1.3 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
   - 1.4 PART ORIENTATION SHALL BE AS SHOWN BELOW.

2. LABELLING (REEL AND SHIPPING BAG).
   - 2.1 CUST. PART NUMBER: IRF7335D1TR
   - 2.2 I.R. PART NUMBER: IRF7335D1TR
   - 2.3 QUANTITY:
   - 2.4 VENDOR CODE: IR
   - 2.5 LOT CODE:
   - 2.6 DATE CODE:





4		38-0027	REEL, Ø 13", HALF, 4mm	1
3		38-0026	REEL, Ø 13", HALF, 8mm	1
2		38-0023	TAPE, COVER, 8mm CARRIER	A/R
1		38-0017	TAPE, CARRIER, 8mm, SO-14	A/R
ITEM		IR No.	DESCRIPTION	QTY

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Pulse width ≤ 300 µs; duty cycle ≤ 2%.
③ When mounted on 1 inch square copper board.
④ Combined Q1,Q2 I_{RMS} @ Pwr V_{out} pins. Calculated continuous current based on max allowable junction temperature; switching or other losses will decrease RMS current capability
⑤ Q1 and Q2 is tested 100% in production to 50mJ to stress and eliminate potentially defective parts. This is not a design for use value.

Data and specifications subject to change without notice.
This product has been designed and qualified for the consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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