FEMTOCLOCKS™ CRYSTAL-TO-LVDS FREQUENCY SYNTHESIZER

ICS844003I-04

General Description

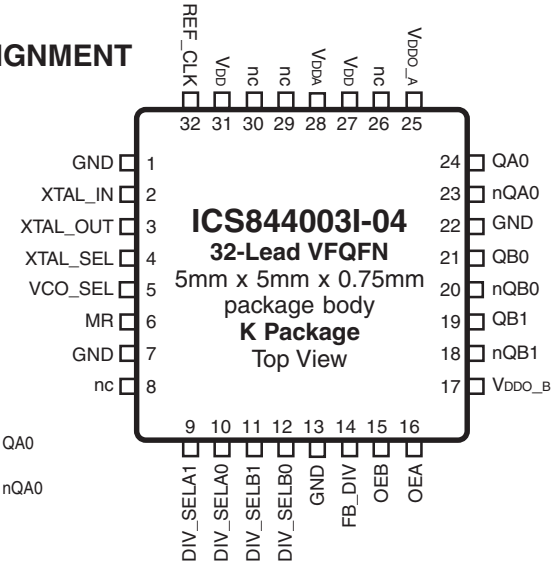
The ICS844003I-04 is a 3 differential output LVDS Synthesizer designed to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. Using a 19.53125MHz, 20MHz or 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of 4 frequency select pins (DIV_SELA[1:0], DIV_SELB[1:0]): 625MHz, 500MHz, 312.5MHz, 250MHz, 156.25MHz, 125MHz and 100MHz. The ICS844003I-04 has 2 output banks, Bank A with one differential LVDS output pair and Bank B with two differential LVDS output pairs.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The ICS844003I-04 uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS844003I-04 is packaged in a 32-pin VFQFN package.

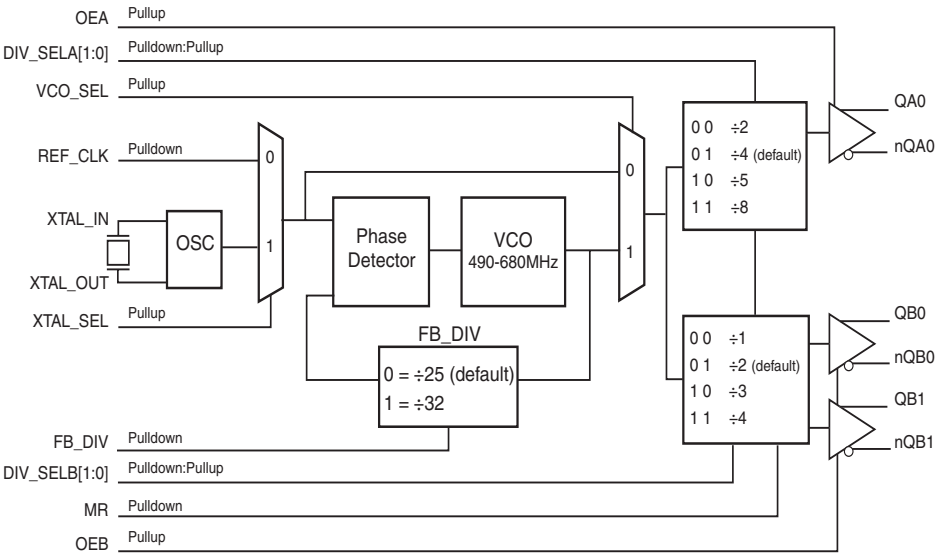
Features

- Three LVDS outputs on two banks, Bank A with one LVDS pair and Bank B with 2 LVDS output pairs
- Using a 19.53125MHz, 20MHz or 25MHz crystal, the two output banks can be independently set for 625MHz, 500MHz, 312.5MHz, 250MHz, 156.25MHz, 125MHz or 100MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 490MHz to 680MHz
- RMS phase jitter @ 125MHz (1.875MHz - 20MHz): 0.50ps (typical)
- 3.3V output supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Pin Assignment



Block Diagram



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 7, 13, 22	GND	Power		Power supply ground.
2, 3	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. XTAL_IN is also the overdrive pin if you want to overdrive the crystal circuit with a single-ended reference clock.
4	XTAL_SEL	Input	Pullup	Crystal select pin. Selects between the single-ended REF_CLK or crystal interface. Has an internal pullup resistor so the crystal interface is selected by default. LVCMOS/LVTTL interface levels.
5	VCO_SEL	Input	Pullup	VCO select pin. When Low, the PLL is bypassed and the crystal reference or REF_CLK (depending on XTAL_SEL setting) are passed directly to the output dividers. Has an internal pullup resistor so the PLL is not bypassed by default. LVCMOS/LVTTL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset, (except for ÷1 state, when the device is configured as a buffer), causing the true outputs QXx to go low and the inverted outputs nQXx to go high. When logic LOW, the internal dividers and the outputs are enabled. MR has an internal pulldown resistor so the power-up default state of outputs and dividers are enabled. LVCMOS/LVTTL interface levels.
8, 26, 29, 30	nc	Unused		No connect.
9	DIV_SELA1	Input	Pulldown	Division select pin for Bank A. Default = LOW. LVCMOS/LVTTL interface levels.
10	DIV_SELA0	Input	Pullup	Division select pin for Bank A. Default = HIGH. LVCMOS/LVTTL interface levels.
11	DIV_SELB1	Input	Pulldown	Division select pin for Bank B. Default = LOW. LVCMOS/LVTTL interface levels.
12	DIV_SELB0	Input	Pullup	Division select pin for Bank B. Default = HIGH. LVCMOS/LVTTL interface levels.
14	FB_DIV	Input	Pulldown	Feedback divide select. When Low (default), the feedback divider is set for ÷20. When HIGH, the feedback divider is set for ÷24. LVCMOS/LVTTL interface levels.
15	OEB	Input	Pullup	Output enable Bank B. Active High output enable. When logic HIGH, the output pair on Bank B is enabled. When logic LOW, the output pair drives differential Low (QBx=Low, nQBx=High). Has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels.
16	OEA	Input	Pullup	Output enable Bank A. Active High output enable. When logic HIGH, the 2 output pairs on Bank A are enabled. When logic LOW, the output pair drives differential Low (QA0=Low, nQA0=High). Has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels.
17	V_{DDO_B}	Power		Output supply pin for Bank B outputs.
18, 19	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
20, 21	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
23, 24	nQA0, QA0	Ouput		Differential output pair. LVDS interface levels.
25	V_{DDO_A}	Power		Output supply pin for Bank A outputs.
27, 31	V_{DD}	Power		Core supply pins.
28	V_{DDA}	Power		Analog supply pin.
32	REF_CLK	Input	Pulldown	Single-ended reference clock input. Has an internal pulldown resistor to pull to low state by default. Can leave floating if using the crystal interface. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

TABLE 3A. OUTPUT BANK A CONFIGURATION SELECT FUNCTION TABLE

Inputs		Outputs
DIV_SELA1	DIV_SELA0	QA0, nQA0
0	0	÷2
0	1	÷4 (default)
1	0	÷5
1	1	÷8

TABLE 3B. OUTPUT BANK B CONFIGURATION SELECT FUNCTION TABLE

Inputs		Outputs
DIV_SELB1	DIV_SELB0	QBx, nQBx
0	0	÷1
0	1	÷2 (default)
1	0	÷3
1	1	÷4

TABLE 3C. OEA SELECT FUNCTION TABLE

Inputs	Outputs
OEA	QA0/nQA0
0	Hi-Z
1	Active (default)

TABLE 3D. OEB SELECT FUNCTION TABLE

Inputs	Outputs
OEB	QB0/nQB0, QB1/nQB1
0	Hi-Z
1	Active (default)

TABLE 3E. FEEDBACK DIVIDER CONFIGURATION SELECT FUNCTION TABLE

Inputs	
FB_DIV	Feedback Divide
0	÷25 (default)
1	÷32

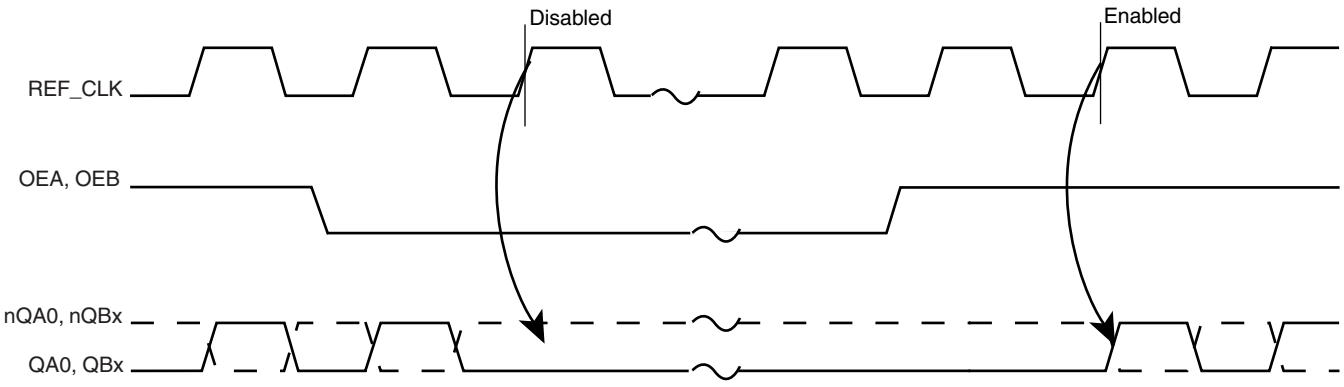


FIGURE 1. OE TIMING DIAGRAM

TABLE 3F. BANK A FREQUENCY TABLE

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA0/nQA0 Output Frequency (MHz)
Crystal Frequency (MHz)	FB_DIV	DIV_SELA1	DIV_SELA0				
25	0	0	0	25	2	12.5	312.5
20	0	0	0	25	2	12.5	250
25	0	0	1	25	4	6.25	156.25
24	0	0	1	25	4	6.25	150
20	0	0	1	25	4	6.25	125
25	0	1	0	25	5	5	125
25	0	1	1	25	8	3.125	78.125
24	0	1	1	25	8	3.125	75
20	0	1	1	25	8	3.125	62.5
19.44	1	0	0	32	2	16	311.04
15.625	1	0	0	32	2	16	250
19.44	1	0	1	32	4	8	155.52
18.75	1	0	1	32	4	8	150
15.625	1	0	1	32	4	8	125
15.625	1	1	0	32	5	6.4	100
19.44	1	1	1	32	8	4	77.76
18.75	1	1	1	32	8	4	75
15.625	1	1	1	32	8	4	62.5

TABLE 3G. BANK B FREQUENCY TABLE

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QBx/nQBx Output Frequency (MHz)
Crystal Frequency (MHz)	FB_DIV	DIV_SELB1	DIV_SELB0				
25	0	0	0	25	1	25	625
25	0	0	1	25	2	12.5	312.5
20	0	0	1	25	2	12.500	250
22.5	0	1	0	25	3	8.333	187.5
25	0	1	1	25	4	6.25	156.25
24	0	1	1	25	4	6.25	150
20	0	1	1	25	4	6.25	125
19.44	1	0	0	32	1	32	622.08
19.44	1	0	1	32	2	16	311.04
15.625	1	0	1	32	2	16	250
18.75	1	1	0	32	3	10.667	200
19.44	1	1	1	32	4	8	155.52
18.75	1	1	1	32	4	8	150
15.625	1	1	1	32	4	8	125

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.97	3.3	3.63	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.15	3.3	V_{DD}	V
$V_{DDO\_A, B}$	Output Supply Voltage		2.97	3.3	3.63	V
I_{DD}	Power Supply Current			115		mA
I_{DDA}	Analog Supply Current			15		mA
I_{DDO}	Output Supply Current			45		mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±10%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, MR, FB_DIV DIV_SELA1, DIV_SELB1	$V_{DD} = V_{IN}$ = 3.63V			150	µA
		DIV_SELB0, DIV_SELA0, VCO_SEL, XTAL_SEL, OEA, OEB	$V_{DD} = V_{IN}$ = 3.63V			5	µA
I_{IL}	Input Low Current	REF_CLK, MR, FB_DIV DIV_SELA1, DIV_SELB1	V_{DD} = 3.63V, V_{IN} = 0V	-5			µA
		DIV_SELB0, DIV_SELA0, VCO_SEL, XTAL_SEL, OEA, OEB	V_{DD} = 3.63V, V_{IN} = 0V	-150			µA

TABLE 4D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±10%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			400		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.35		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental			
Frequency	FB_DIV = ÷25		19.6		27.2	MHz
	FB_DIV = ÷32		15.313		21.25	MHz
Equivalent Series Resistance (ESR)					50	Ω
Shunt Capacitance					7	pF
Drive Level					100	µW

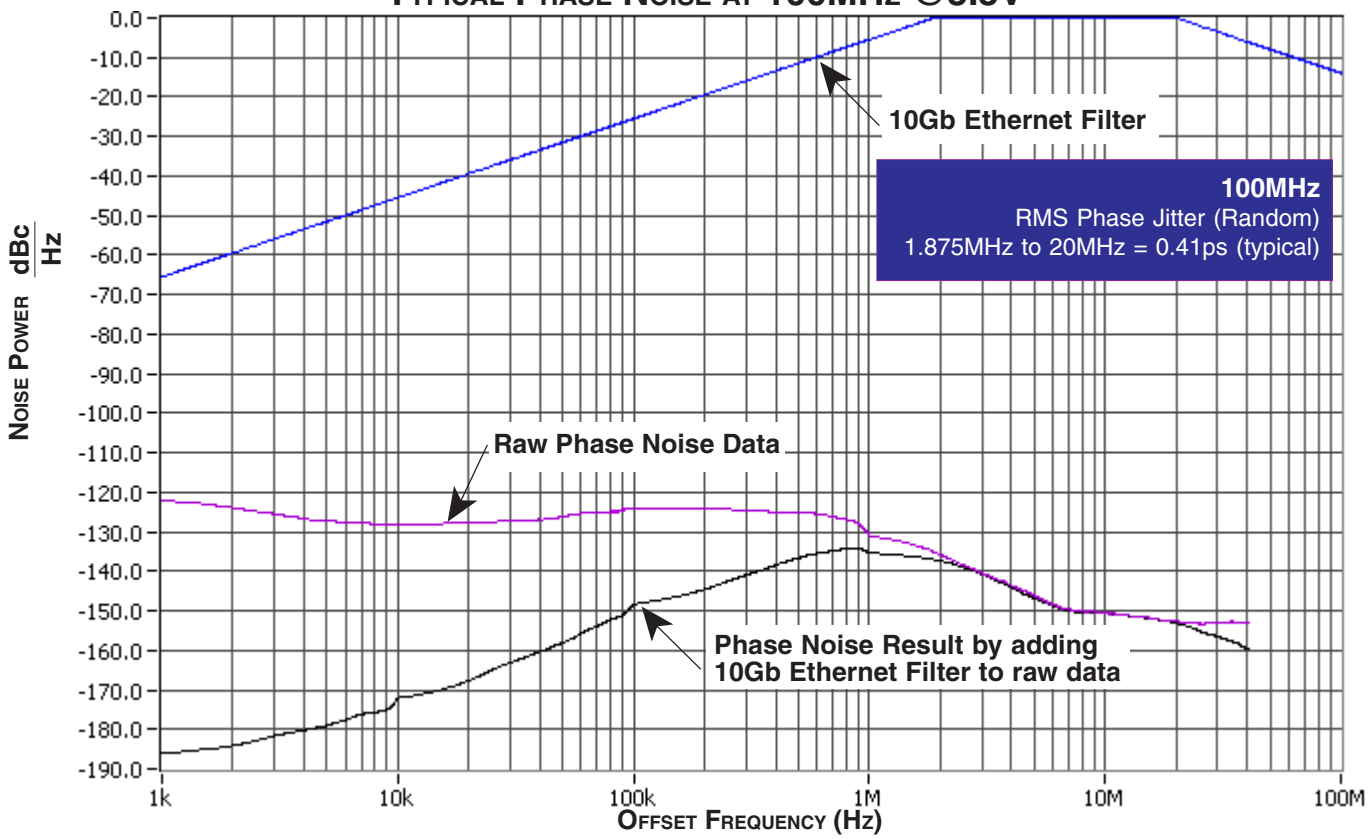
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±10%, T_A = -40°C TO 85°C

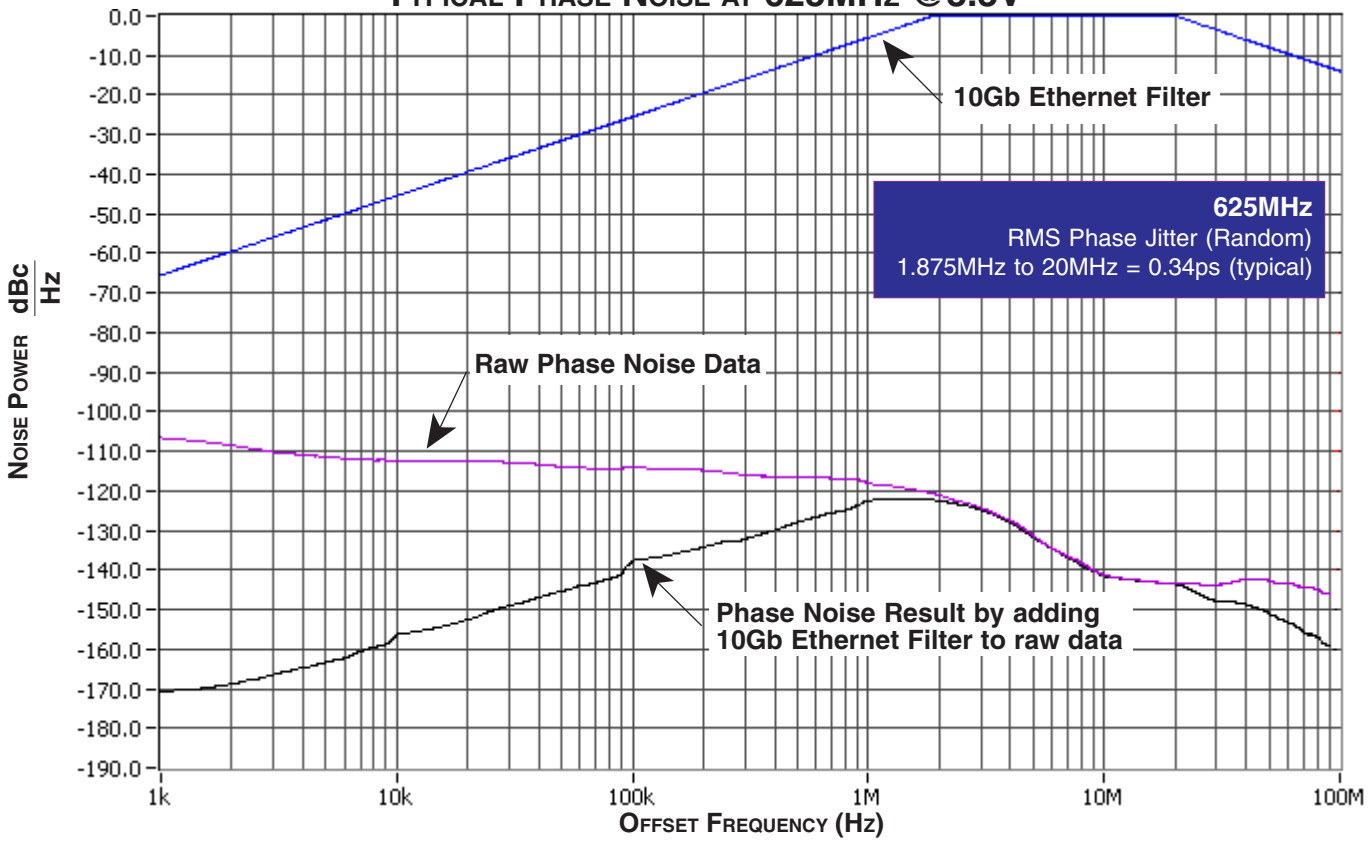
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range		Output Divider = ÷1	490		680	MHz
			Output Divider = ÷2	245		340	MHz
			Output Divider = ÷3	163.33		226.67	MHz
			Output Divider = ÷4	122.5		170	MHz
			Output Divider = ÷5	98		136	MHz
			Output Divider = ÷8	61.25		85	MHz
*t*sk(b)	Bank Skew, NOTE 1				TBD		ps
*t*sk(o)	Output Skew;	NOTE 2, 3	Outputs @ Same Frequency		TBD		ps
		NOTE 2, 3, 4	Outputs @ Different Frequencies		TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 5		625MHz (1.875MHz - 20MHz)		0.34		ps
			500MHz (1.875MHz - 20MHz)		0.38		ps
			312.5MHz (1.875MHz - 20MHz)		0.34		ps
			250MHz (1.875MHz - 20MHz)		0.42		ps
			125MHz (1.875MHz - 20MHz)		0.50		ps
			100MHz (1.875MHz - 20MHz)		0.41		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		325		ps
odc	Output Duty Cycle		Output Divider ≠ ÷1		50		%
			Output Divider = ÷1		50		%

NOTE 1: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Characterized using output dividers 1, 2, 4, 8.
NOTE 5: Please refer to the Phase Noise Plots.

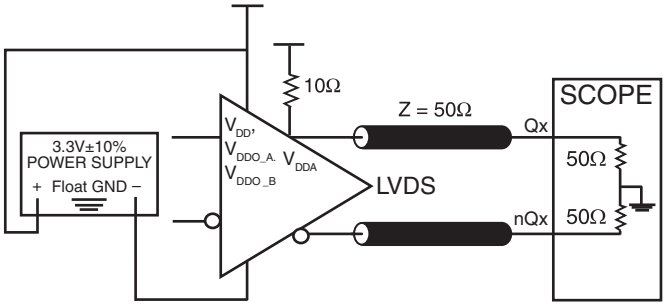
TYPICAL PHASE NOISE AT 100MHZ @3.3V



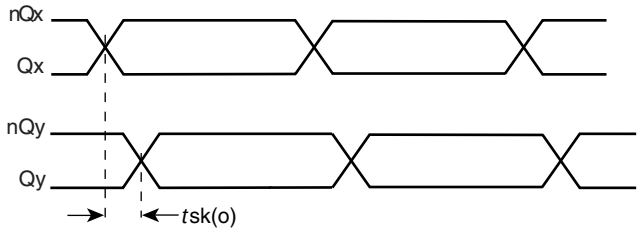
TYPICAL PHASE NOISE AT 625MHZ @3.3V



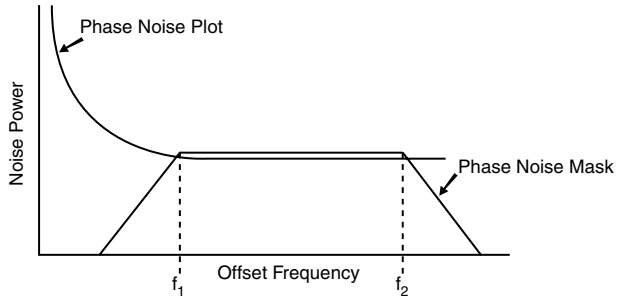
PARAMETER MEASUREMENT INFORMATION



3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT

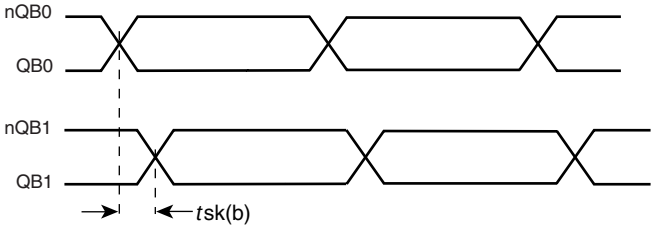


OUTPUT SKEW

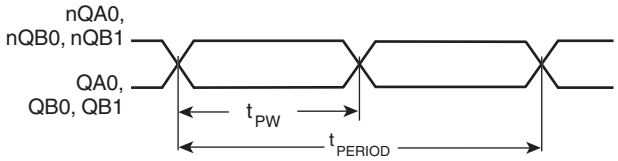


RMS Jitter = $\sqrt{\text{Area Under the Masked Phase Noise Plot}}$

RMS PHASE JITTER

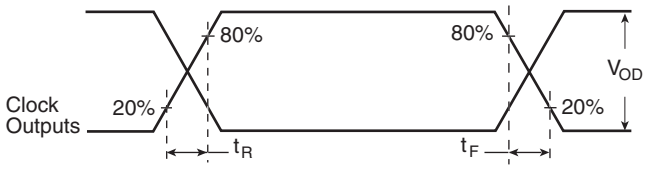


BANK SKEW

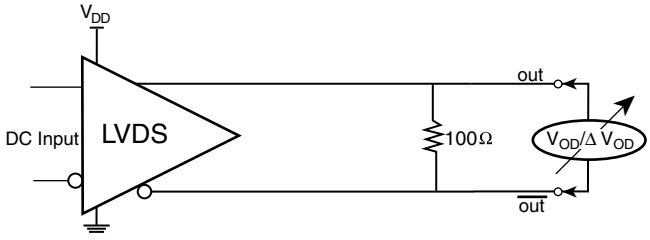


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

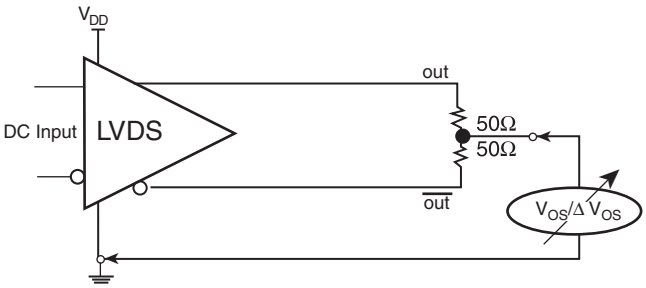
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844003I-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDOx} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

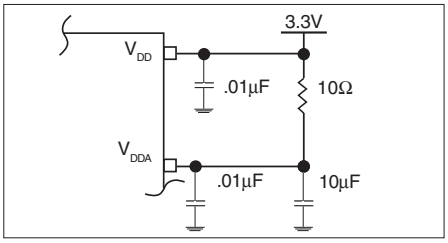


FIGURE 2. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS844003I-04 has been characterized with an 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

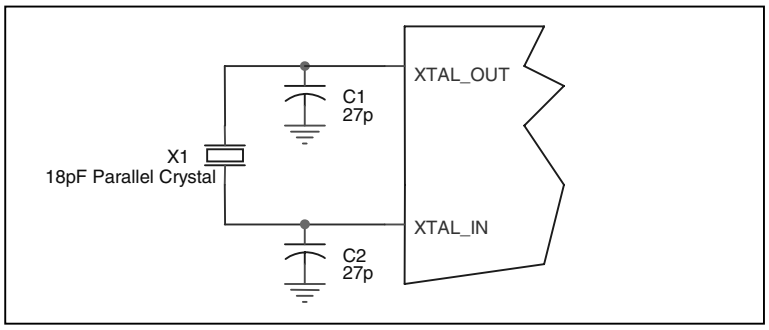


FIGURE 3. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

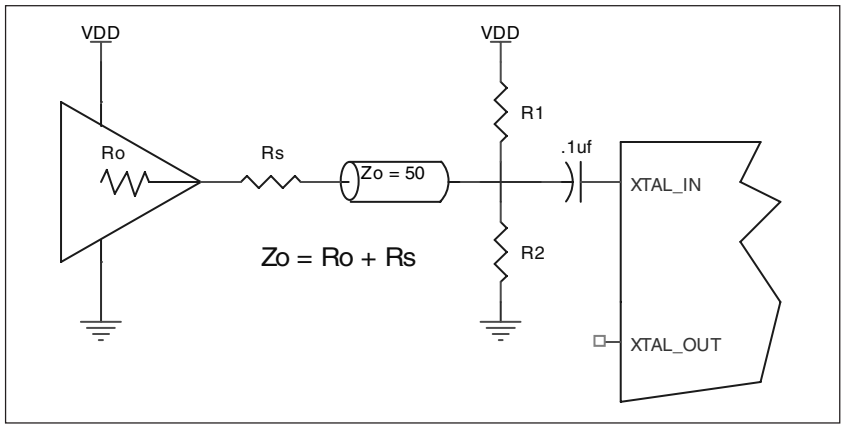


FIGURE 4. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT:
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVDS OUTPUT
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 5.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

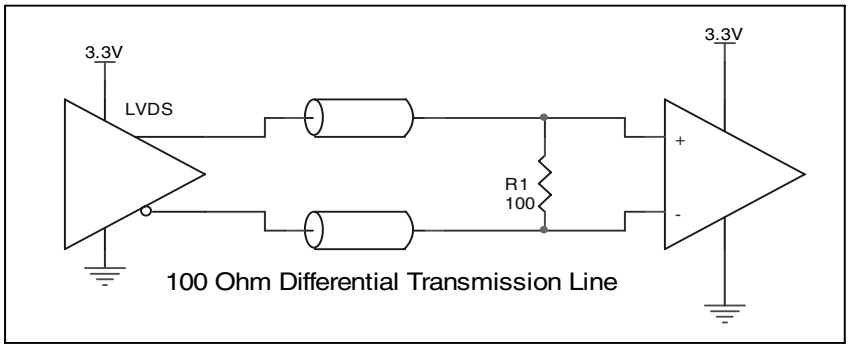


Figure 5. Typical LVDS Driver Termination

Thermal Release Path

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder as shown in *Figure 6.* For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

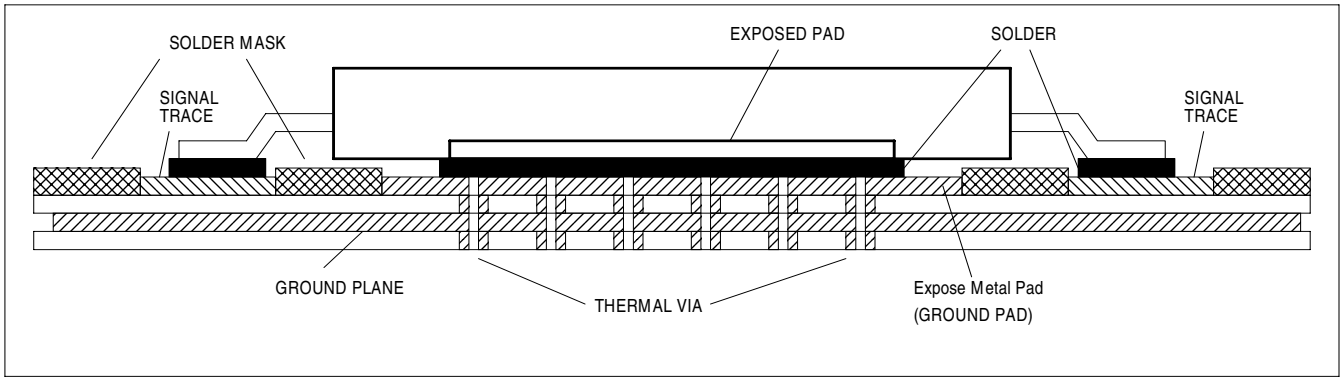


Figure 6. P.C. Board for Exposed Pad Thermal Release Path Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS844003I-04.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS844003I-04 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 10% = 3.63V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX} + I_{DDO_MAX}) = 3.63V * (115mA + 15mA + 45mA) = **635.25mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming air flow of 1 meter per second and a multi-layer board, the appropriate value is 32.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.635W * 32.4°C/W = 105.6°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 32-LEAD VFQFN, FORCED CONVECTION

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

TRANSISTOR COUNT

The transistor count for ICS844003I-04 is: 4058

PACKAGE OUTLINE - K SUFFIX FOR 32 LEAD VFQFN

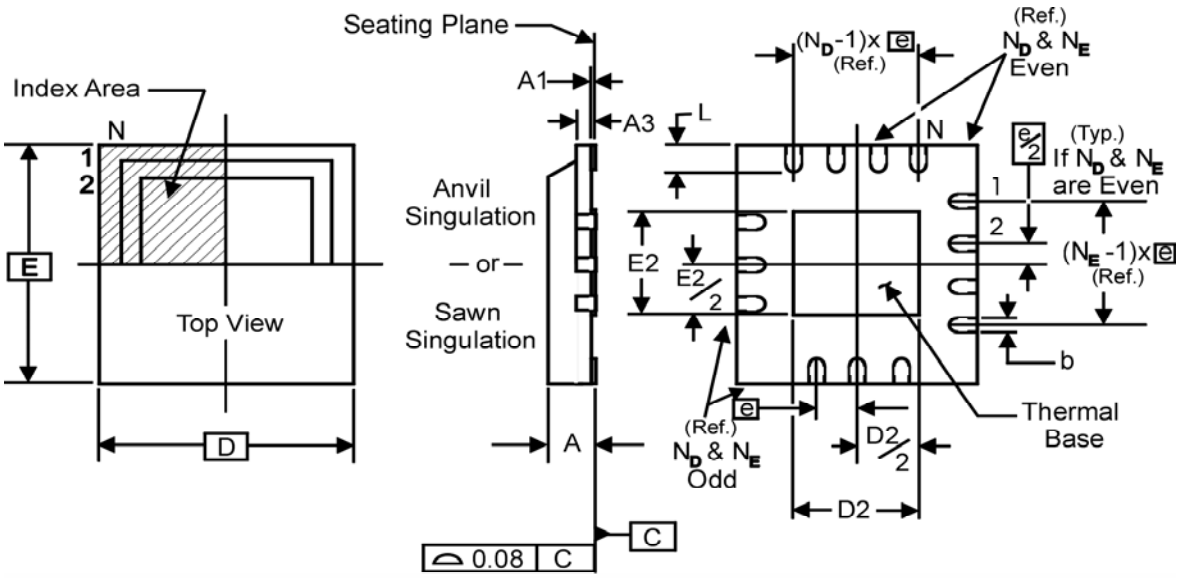


TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	0.80	--	1.00
A1	0	--	0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D			8
N_E			8
D		5.00 BASIC	
D2	1.25	2.25	3.25
E		5.00 BASIC	
E2	1.25	2.25	3.25
e		0.50 BASIC	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844003AKI-04	TBD	32 Lead VFQFN	tray	-40°C to 85°C
844003AKI-04T	TBD	32 Lead VFQFN	2500 tape & reel	-40°C to 85°C
844003AKI-04LF	ICS403AI04L	32 Lead "Lead-Free" VFQFN	tray	-40°C to 85°C
844003AKI-04LFT	ICS403AI04L	32 Lead "Lead-Free" VFQFN	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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