Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (4K x 4-BIT)

IDT6168SA
IDT6168LA

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 12/15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 10/12/15/20/25/35ns (max.)
- Low power consumption
  - — IDT6168SA
    Active: 225mW (typ.)
    Standby: 100µW (typ.)
  - — IDT6168LA
    Active: 225mW (typ.)
    Standby: 10µW (typ.)
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin ceramic or plastic DIP, 20-pin SOIC, 20-pin SOJ, 20-pin CERPACK and 20-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS™ process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86705 is listed on this function. Refer to Section 2/page 2-4

DESCRIPTION:

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for high-speed memory applications.

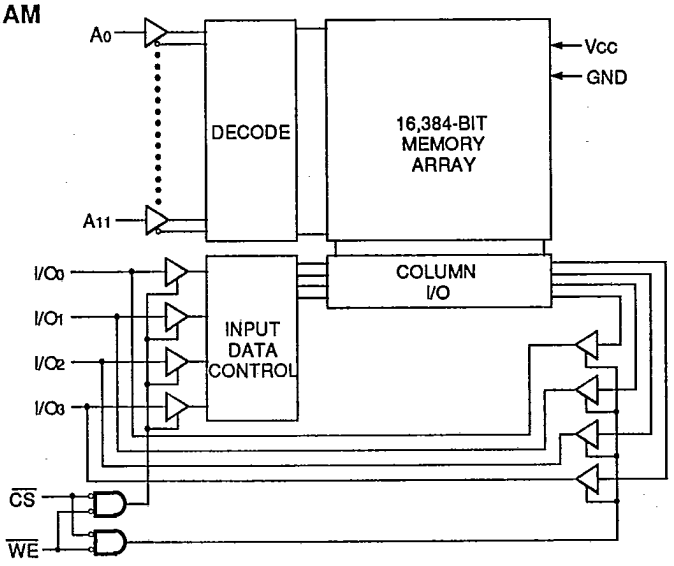
Access times as fast 10ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery. All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply.

The IDT6168 is packaged in either a space saving 20-pin, 300 mil ceramic or plastic DIP, 20-pin CERPACK, 20-pin SOIC, 20-pin SOJ, or 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

5

FUNCTIONAL BLOCK DIAGRAM



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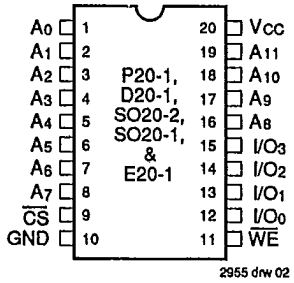
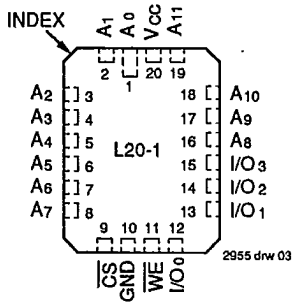
PIN CONFIGURATIONS



DIP/SOIC/SOJ/CERPACK
TOP VIEW



LCC
TOP VIEW

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DOUT	Active
Write	L	L	DIN	Active

NOTE: 2955 tbl 02
1. H = VIH, L = VIL, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2955 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTIONS

Name	Description
A0–A11	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O0-3	Data Input/Output
VCC	Power
GND	Ground

2955 tbl 01

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2955 tbl 05
1. VIL (min.) = -3.0V for pulse width less than 20ns.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	7	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

NOTE: 2955 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2955 tbl 06

T-46-23-08

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA10 Com'l.	6168SA10 Mil.	6168SA12[4] Com'l.	6168SA12[4] Mil.	6168SA15[4] Com'l.	6168SA15[4] Mil.	6168SA20 6168LA20 Com'l.	6168SA20 6168LA20 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[3]	SA	120	—	110	120	110	120	90	100	mA
		LA	—	—	—	—	—	—	70	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	175	—	165	175	145	165	120	120	mA
		LA	—	—	—	—	—	—	100	110	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	SA	65	—	65	65	55	60	45	45	mA
		LA	—	—	—	—	—	—	30	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[3]	SA	20	—	20	20	20	20	20	20	mA
		LA	—	—	—	—	—	—	0.5	5	

DC ELECTRICAL CHARACTERISTICS (Continued)[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA25 6168LA25 Com'l.	6168SA25 6168LA25 Mil.	6168SA35 6168LA35 Com'l.	6168SA35 6168LA35 Mil.	6168SA45/55 6168LA45/55 Com'l.	6168SA45/55 6168LA45/55 Mil.	6168SA70[2] 6168LA70[2] Com'l.	6168SA70[2] 6168LA70[2] Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[3]	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	110	120	100	110	—	110	—	110	mA
		LA	90	100	80	90	—	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	SA	35	45	30	35	—	35	—	35	mA
		LA	25	30	20	25	—	25/20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[3]	SA	2	10	2	10	—	10	—	10	mA
		LA	0.05	0.3	0.05	0.3	—	0.3	—	0.3	

2955 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f = f_{MAX} (all inputs except Chip Select cycling at f = 1/t_{RC}). f = 0 means no address or control lines change.
4. Military values are preliminary only.

T-46-23-08

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6168SA Min.	IDT6168SA Max.	IDT6168LA Min.	IDT6168LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL COM'L	— —	10 2	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL COM'L	— —	10 2	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2955 tbl 08

DATA RETENTION CHARACTERISTICS

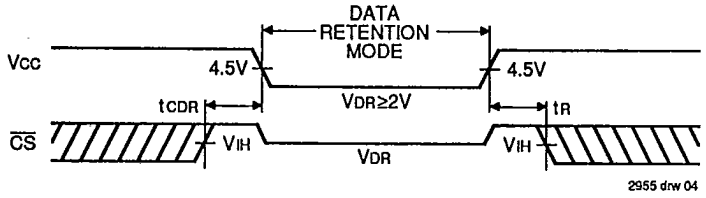
(LA Version Only)

Symbol	Parameter	Test Condition		IDT6168LA Min.	IDT6168LA Typ.(1)	IDT6168LA Max.	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or ≤ 0.2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	— —	0.5(2) 1.0(3)	100(2) 150(3)	µA
			COM'L.	— —	0.5(2) 1.0(3)	20(2) 30(3)	µA
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(5)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2955 tbl 09

NOTES:
1. T_A = +25°C,
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed, but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2955 tbl 10

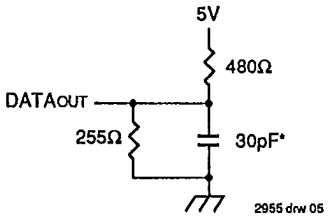


Figure 1. Output Load

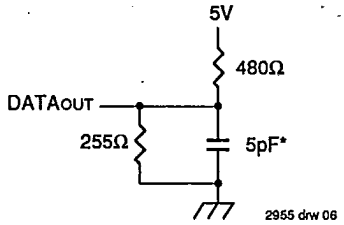


Figure 2. Output Load
(for tHZ, tLZ, tWZ and tOW)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA10[3] Min.	6168SA10[3] Max.	6168SA12 Min.	6168SA12 Max.	6168SA15 Min.	6168SA15 Max.	6168SA20/25 6168LA20/25 Min.	6168SA20/25 6168LA20/25 Max.	Unit
Read Cycle										
tRC	Read Cycle Time	10	—	12	—	15	—	20/25	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	20/25	ns
tACS	Chip Select Access Time	—	10	—	12	—	15	—	20/25	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tLZ	Chip Select to Output in Low Z[2]	3	—	3	—	3	—	5	—	ns
tHZ	Chip Deselect to Output in High Z[2]	—	6	—	7	—	8	—	10	ns
tPU	Chip Select to Power Up Time[2]	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time[2]	—	10	—	12	—	15	—	20/25	ns

AC ELECTRICAL CHARACTERISTICS (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

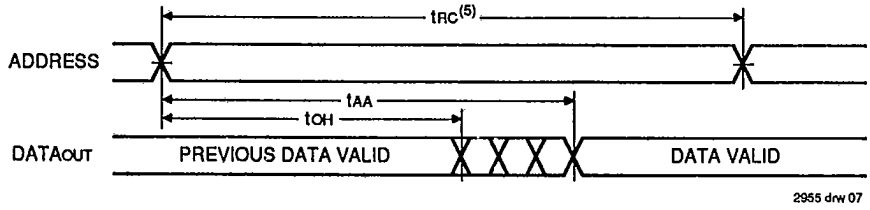
Symbol	Parameter	6168SA35 6168LA35 Min.	6168SA35 6168LA35 Max.	6168SA45/55[1] 6168LA45/55[1] Min.	6168SA45/55[1] 6168LA45/55[1] Max.	6168SA70[1] 6168LA70[1] Min.	6168SA70[1] 6168LA70[1] Max.	Unit
Read Cycle								
tRC	Read Cycle Time	35	—	45/55	—	70	—	ns
tAA	Address Access Time	—	35	—	45/55	—	70	ns
tACS	Chip Select Access Time	—	35	—	45/55	—	70	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Chip Select to Output in Low Z[2]	5	—	5	—	5	—	ns
tHZ	Chip Deselect to Output in High Z[2]	—	15	—	25	—	30	ns
tPU	Chip Select to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time[2]	—	35	—	40/50	—	60	ns

2955 tbl 11

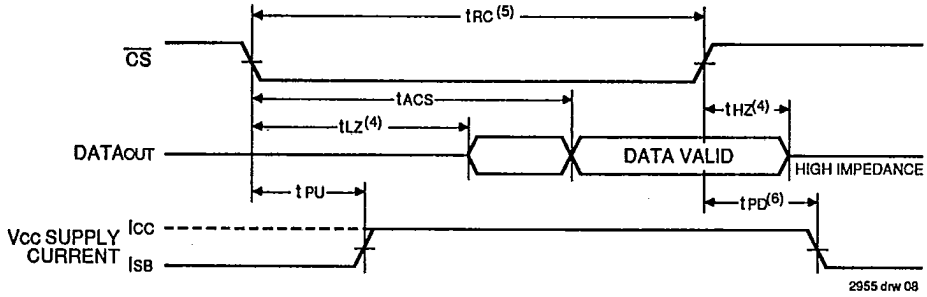
NOTES:
1. -55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
2. This parameter is guaranteed, but not tested.
3. 0° to +70°C temperature range only.

T-46-23-08

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. This parameter is guaranteed and not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA10[4] Min.	6168SA10[4] Max.	6168SA12 Min.	6168SA12 Max.	6168SA15 Min.	6168SA15 Max.	6168SA20/25 6168LA20/25 Min.	6168SA20/25 6168LA20/25 Max.	Unit
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	ns
tCW	Chip Select to End of Write	10	—	12	—	15	—	20	—	ns
tAW	Address Valid to End of Write	10	—	12	—	15	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	7	—	8	—	9	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z[2]	—	4	—	5	—	6	—	7	ns
tOW	Output Active from End of Write[2]	0	—	0	—	0	—	0	—	ns

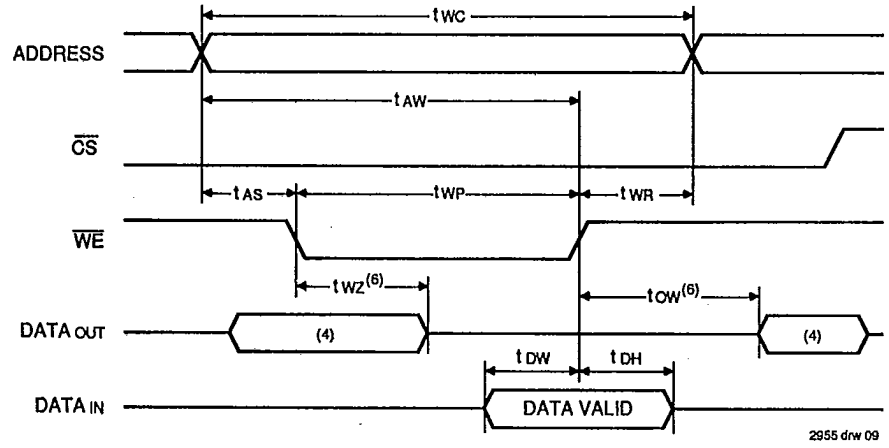
AC ELECTRICAL CHARACTERISTICS (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35 Min.	6168SA35 6168LA35 Max.	6168SA45/55[1] 6168LA45/55[1] Min.	6168SA45/55[1] 6168LA45/55[1] Max.	6168SA70[1] 6168LA70[1] Min.	6168SA70[1] 6168LA70[1] Max.	Unit
Write Cycle								
tWC	Write Cycle Time	30	—	40/50	—	60	—	ns
tCW	Chip Select to End of Write	30	—	40/50	—	60	—	ns
tAW	Address Valid to End of Write	30	—	40/50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	30	—	40/50	—	60	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	DataValid to End of Write	15	—	20	—	25	—	ns
tDH	Data Hold Time	0	—	3	—	3	—	ns
tWZ	Write Enable to Output in High Z[2]	—	13	—	20/25	—	30	ns
tOW	Output Active from End of Write[2]	0	—	0	—	0	—	ns

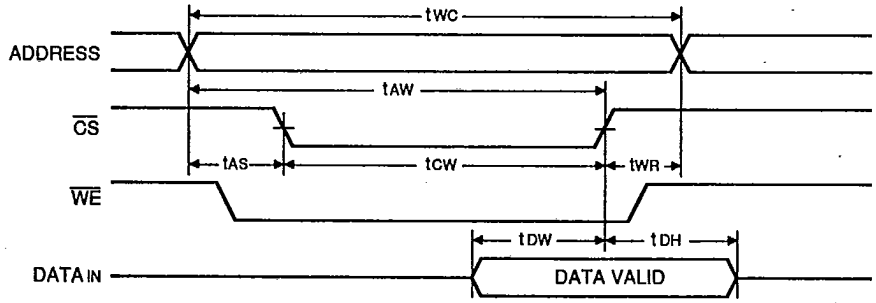
2955 tbl 12

NOTES:
1. -55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
2. This parameter is guaranteed, but not tested.
3. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
4. 0° to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3)



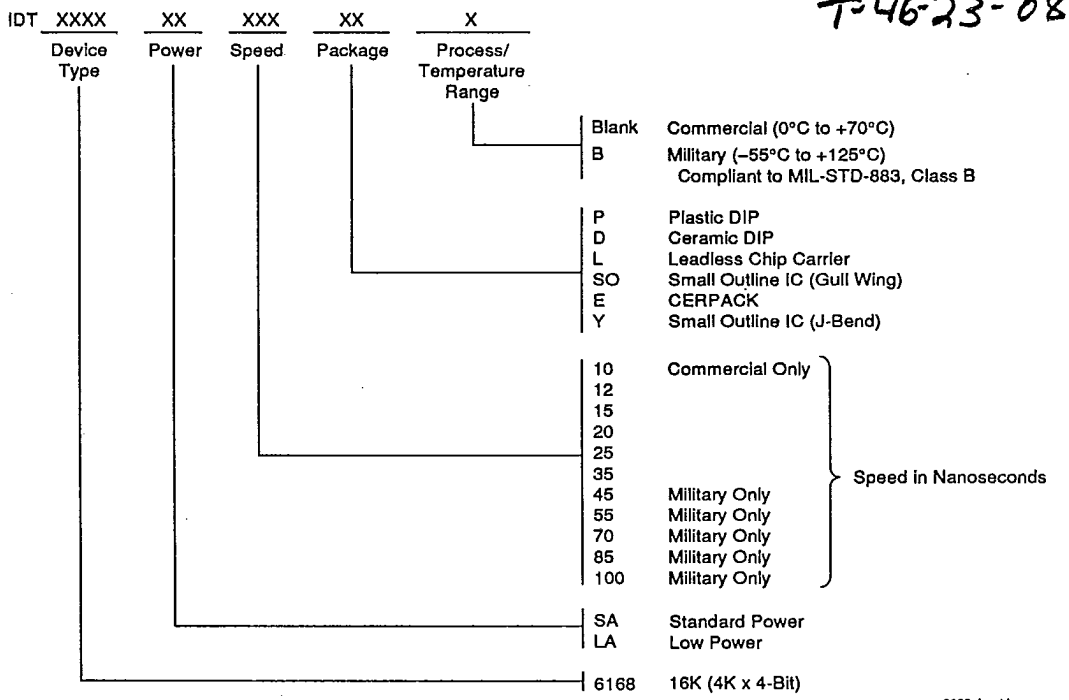
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP} or t_{CW}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

ORDERING INFORMATION

T-46-23-08



2955 drw 11

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