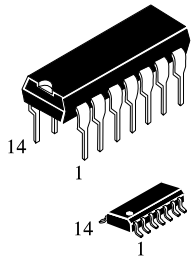
IW4001B

Quad 2-Input NOR Gate
High-Voltage Silicon-Gate CMOS

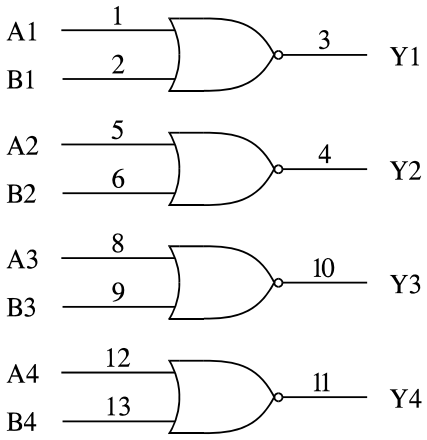
The IW4001B NOR gates provide the system designer with direct emplementation of the NOR function.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  0.5 V min @ 5.0 V supply
  1.0 V min @ 10.0 V supply
  1.5 V min @ 15.0 V supply



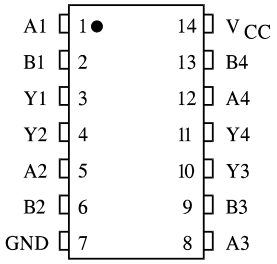
ORDERING INFORMATION
IW4001BN Plastic
IW4001BD SOIC
IZ4001B CHIP
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

L – LOW voltage level

H – HIGH voltage level

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	500 500	mW
Ptot	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 12 mW/°C from 100° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125 °C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.5V V_{OUT}=1.0 V V_{OUT}=1.5V	5.0 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V V_{OUT}=1.0 V or V_{CC} - 1.0 V V_{OUT}=1.5 V or V_{CC} - 1.5 V	5.0 10 15	1.5 3 4	1.5 3 4	1.5 3 4	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0 10 15 20	0.25 0.5 1.0 5.0	0.25 0.5 1.0 5.0	7.5 15 30 150	µA
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC} U_{OL}=0.4 V U_{OL}=0.5 V U_{OL}=1.5 V	 5.0 10 15	 0.64 1.6 4.2	 0.51 1.3 3.4	 0.36 0.9 2.4	mA
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC} U_{OH}=2.5 V U_{OH}=4.6 V U_{OH}=9.5 V U_{OH}=13.5 V	 5.0 5.0 10 15	 -2.0 -0.64 -1.6 -4.2	 -1.6 -0.51 -1.3 -3.4	 -1.15 -0.36 -0.9 -2.4	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=200kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figure 1)	5.0 10 15	250 120 90	250 120 90	250 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	200 100 80	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF

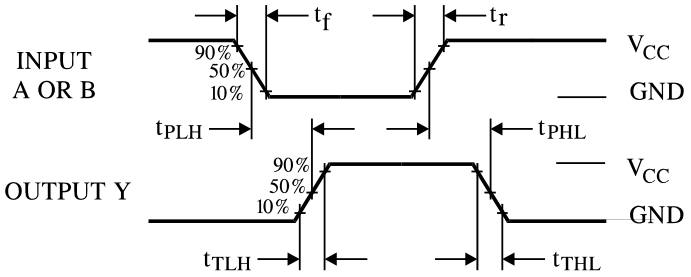
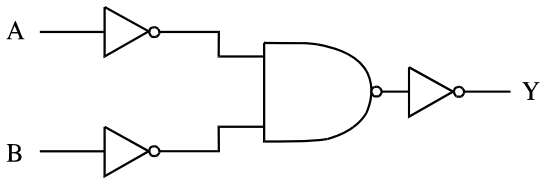
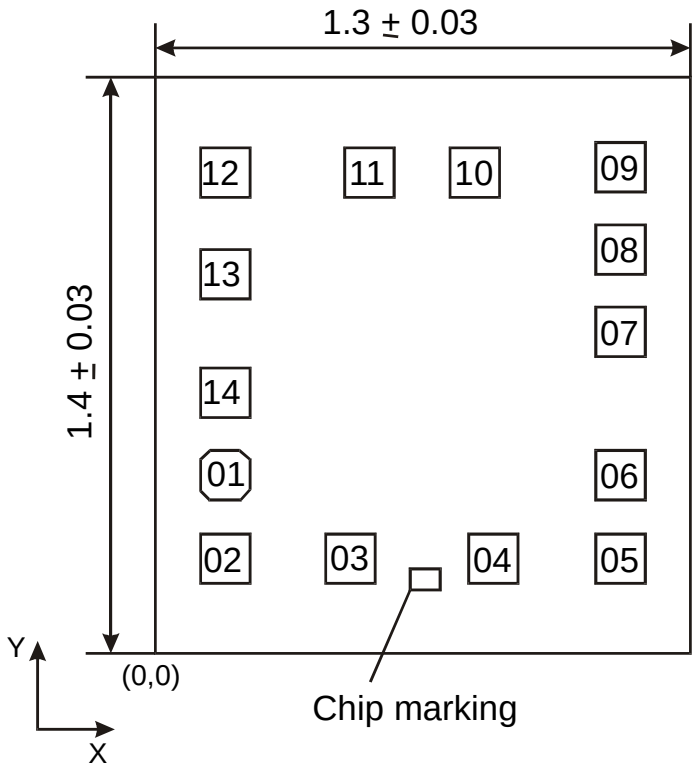


Figure 1. Switching Waveforms

EXPANDED LOGIC DIAGRAM
(1/4 of the Device)



CHIP PAD DIAGRAM



Chip marking: 400115
Location of marking (mm): left lower corner **x = 0.619, y = 0.154**
Chip thickness: 0.46 ± 0.02 мм

PAD LOCATION

Chip thickness	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	A1	0.110	0.373	0.120×0.120
02	B1	0.110	0.170	0.120×0.120
03	Y1	0.414	0.170	0.120×0.120
04	Y2	0.761	0.170	0.120×0.120
05	A2	1.070	0.170	0.120×0.120
06	B2	1.070	0.373	0.120×0.120
07	GND	1.070	0.721	0.120×0.120
08	A3	1.070	0.921	0.120×0.120
09	B3	1.070	1.121	0.120×0.120
10	Y3	0.716	1.108	0.120×0.120
11	Y4	0.460	1.108	0.120×0.120
12	A4	0.110	1.108	0.120×0.120
13	B4	0.110	0.861	0.120×0.120
14	Vcc	0.110	0.573	0.120×0.120

Note: Location is given as per passivation layer