FemtoClock™ Crystal-to-LVDS Clock Generator

ICS844011

PRELIMINARY DATA SHEET

General Description

ICS HiPerClockS™

The ICS844011 is a Fibre Channel Clock Generator and a member of the HiPerClocks™ family of high performance devices from IDT. The ICS844011 uses an 18pF parallel resonant crystal over the range of 20.4MHz - 28.3MHz. For Fibre Channel applications, a 26.5625MHz crystal is used. The ICS844011 has excellent <1ps phase jitter performance, over the 637kHz - 10MHz integration range. The ICS844011 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

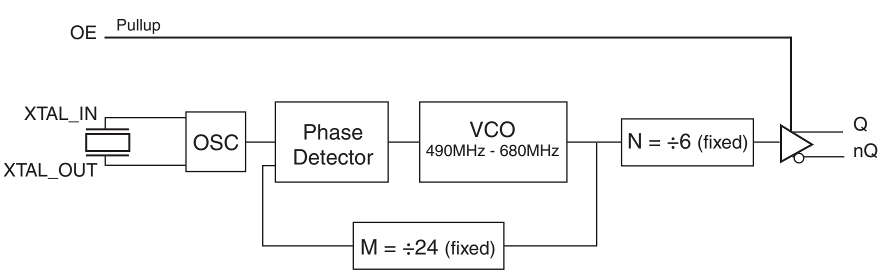
Features

- One differential LVDS clock output pair
- Crystal interface designed for 18pF parallel resonant crystals (20.4MHz – 28.3MHz)
- Output frequency range: 81.66MHz – 113.33MHz
- VCO range: 490MHz – 680MHz
- RMS phase jitter @ 106.25MHz, using a 26.5625MHz crystal (637kHz - 10MHz): 0.75ps (typical)
- RMS phase jitter @ 156.25MHz, (1.875MHz - 20MHz): 0.45ps (typical)
- Full 3.3V or 2.5V operating supply
- Available in both standard (RoHs 5) and lead-free (RoHS 6) packages
- 0°C to 70°C ambient operating temperature

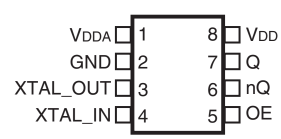
Common Configuration Table – Fibre Channel

Inputs				
Crystal Frequency (MHz)	M	N	Multiplication Value M/N	Output Frequency (MHz)
26.5625	24	6	4	106.25
25	24	6	4	100

Block Diagram



Pin Assignment



ICS844011
8-lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDA}	Power		Analog power supply.
2	GND	Power		Power supply ground.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	OE	Input	Pullup	Output enable pin. When HIGH, Q/nQ output is active. When LOW, the Q/nQ output is in a high impedance state. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential clock output. LVDS interface levels.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to an internal input resistor. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	129.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.07	3.3	V_{DD}	V
I_{DD}	Power Supply Current			90		mA
I_{DDA}	Analog Supply Current			7		mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.07	2.5	V_{DD}	V
I_{DD}	Power Supply Current			85		mA
I_{DDA}	Analog Supply Current			7		mA

Table 3C. LVCMOS/LVTTL Input DC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	OE	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

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Table 3D. LVDS DC Characteristics, V_{DD} **= 3.3V±5%,** T_A **= 0°C to 70°C**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.25		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 3E. LVDS DC Characteristics, V_{DD} **= 2.5V±5%,** T_A **= 0°C to 70°C**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.2		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		20.4		28.3	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

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AC Characteristics

Table 5A. AC Characteristics, V_{DD} = 3.3V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		81.66		113.33	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	106.25MHz, Integration Range: 637kHz – 10MHz				ps
		100MHz, Integration Range: 637kHz – 10MHz		0.75		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		275		ps
odc	Output Duty Cycle			50		%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to the phase noise plot.

Table 5B. AC Characteristics, V_{DD} = 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		81.66		113.33	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	106.25MHz, Integration Range: 637kHz – 10MHz		0.45		ps
		100MHz, Integration Range: 637kHz – 10MHz		0.93		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		295		ps
odc	Output Duty Cycle			50		%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to the phase noise plot.

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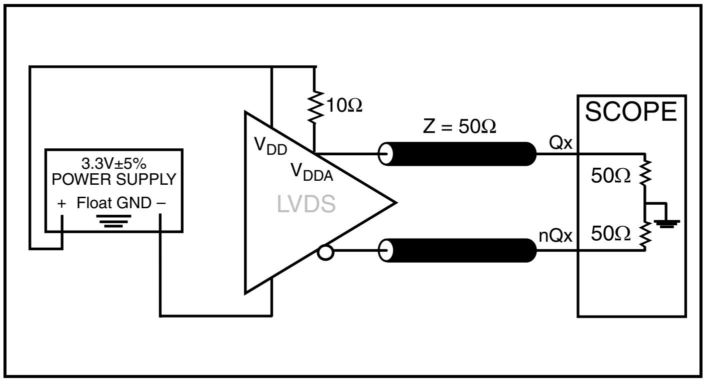
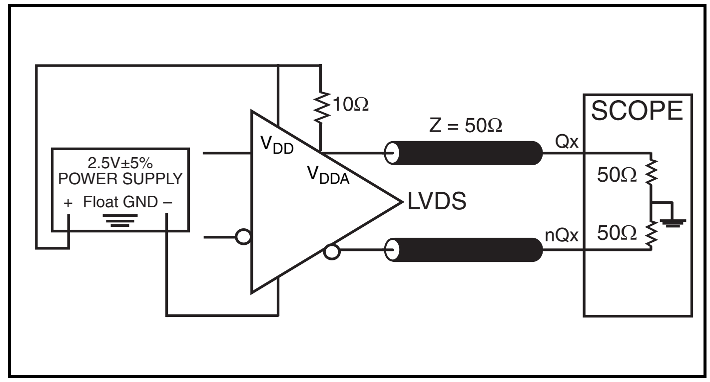
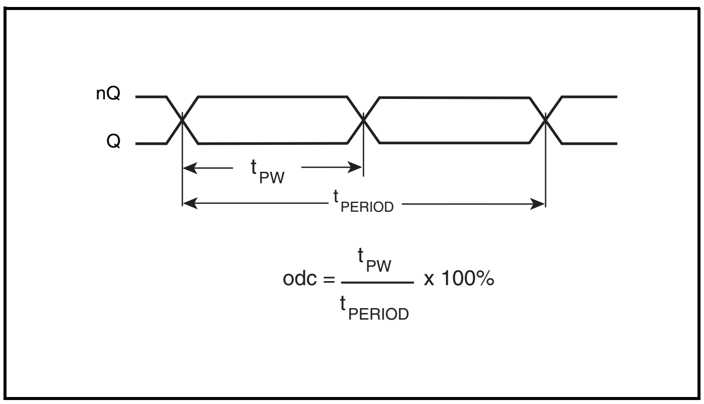
Parameter Measurement Information



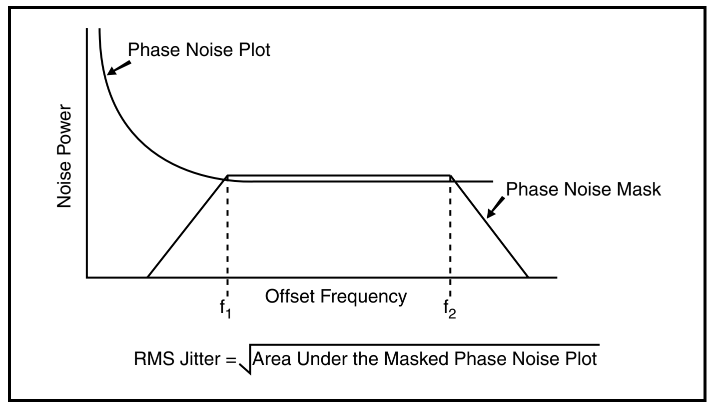
3.3V LVDS Output Load AC Test Circuit



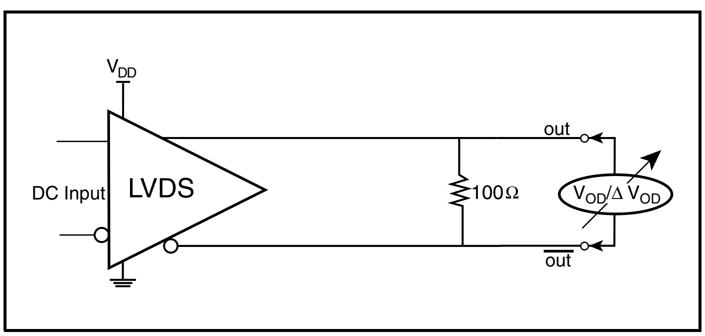
2.5V LVDS Output Load AC Test Circuit



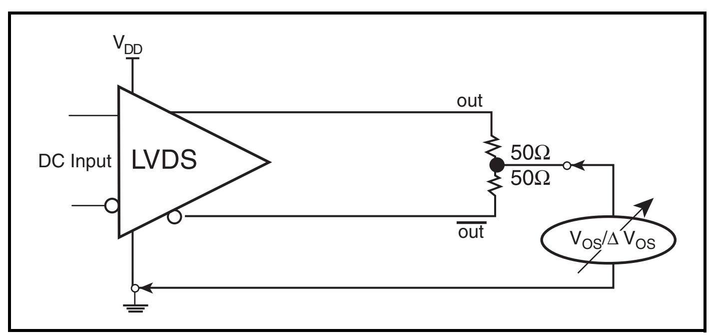
Output Duty Cycle/Pulse Width/Period



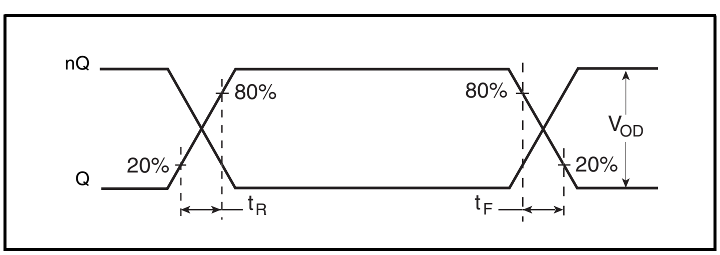
RMS Phase Jitter



Differential Output Voltage Setup



Offset Voltage Setup



Output Rise/Fall Time

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Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844011 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

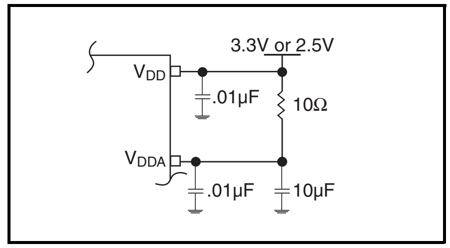

Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS844011 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

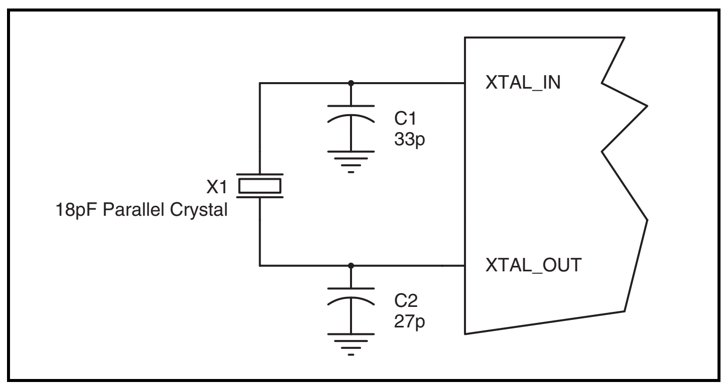

Figure 2. Crystal Input Interface

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LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

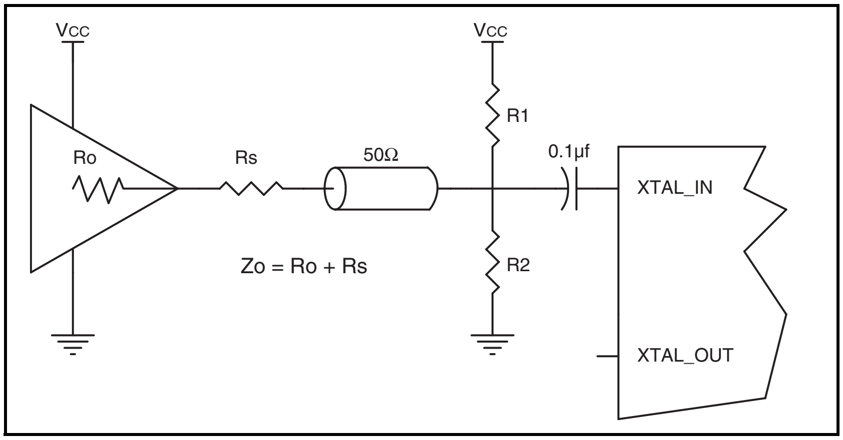

Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

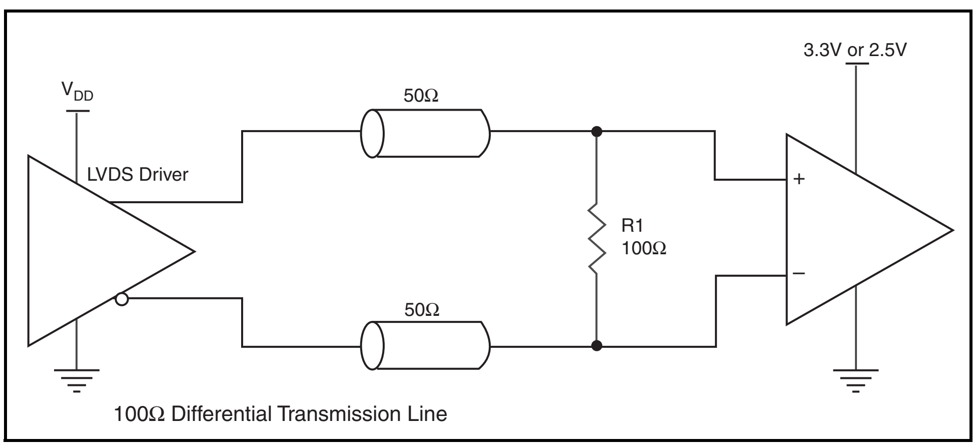

Figure 4. Tyical LVDS Driver Termination

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Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844011.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844011 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (90mA + 7mA) = **336.1mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.336W * 129.5°C/W = 113.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 8-lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

Transistor Count

The transistor count for ICS844011 is: 2533

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

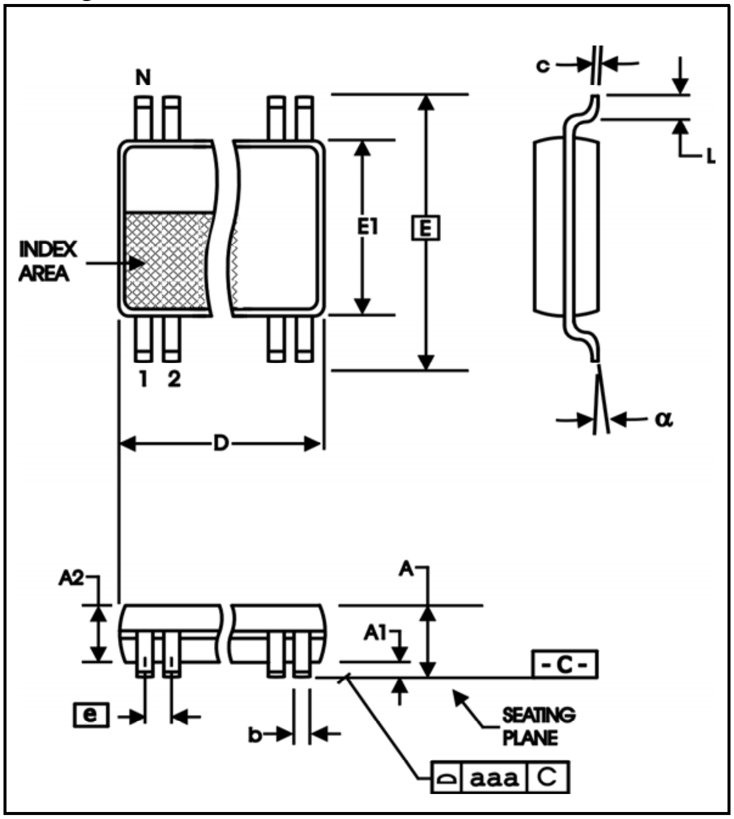

Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

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Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844011AG	4011A	8-lead TSSOP	Tube	0°C to 70°C
844011AG	4011A	8-lead TSSOP	2500 Tape & Reel	0°C to 70°C
844011AGLF	011AL	Lead-Free, 8-lead TSSOP	Tube	0°C to 70°C
844011AGLFT	011AL	Lead-Free, 8-lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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