## Dual 8-input Multiplexers

The HD100163 is a dual 8 -input Multiplexer. The Data Select(Sn) inputs determine which bit ( An and Bn ) will be presented at the Outputs $\left(Z_{A}\right.$ and $Z_{B}$ respectively). The same bit $(0-7)$ will be selected for both the $Z_{A}$ and $Z_{B}$ output.

PIN ARRANGEMENT

- HD100163

- HD100163F

! Top View
- LOGIC DIAGRAM

- TRUTH TABLE

| Input |  |  |  |  |  |  |  |  |  |  | Output |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Address |  |  | Data |  |  |  |  |  |  |  |  |
| S : | S | So | $\begin{aligned} & \mathrm{A} ; \\ & \mathrm{B} ; \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathbf{A}_{6} \\ & \mathbf{B}_{6} \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathbf{A}_{5} \\ & B_{5} \\ & \hline \end{aligned}$ | $\begin{aligned} & A_{1} \\ & B_{1} \end{aligned}$ | $\begin{aligned} & \hline \mathrm{A}_{3} \\ & \mathrm{~B}_{3} \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathbf{A}_{2} \\ & \mathbf{B}_{2} \end{aligned}$ | $\begin{aligned} & \mathbf{A}_{1} \\ & \mathbf{B}_{1} \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathbf{A}_{0} \\ & B_{0} \end{aligned}$ |  |
|  | $\begin{aligned} & \mathrm{L} \\ & \mathrm{~L} \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{~L} \end{aligned}$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | ${ }_{\mathrm{H}}^{\mathrm{L}}$ | L |
| $\mathrm{L}$ | $\stackrel{L}{\mathrm{~L}}$ | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | $\begin{gathered} - \\ \underset{H}{\mathrm{H}} \\ \hline \end{gathered}$ | $\times$ | ${ }_{\mathrm{H}}^{\mathrm{L}}$ |
| $\begin{aligned} & \mathrm{L} \\ & \mathrm{~L} \end{aligned}$ | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \mathrm{L} \\ & \mathrm{~L} \\ & \hline \end{aligned}$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | $\times$ | $\times$ | L |
| $\mathrm{I}$ | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \\ & \hline \end{aligned}$ | $\times$ | $\times$ | $\times$ | $\times$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | $\times$ | $\times$ | $\times$ | ${ }_{\mathrm{L}}^{\mathrm{L}}$ |
| $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{~L} \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{~L} \end{aligned}$ | $\times$ | $\times$ | $\times$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | $\times$ | $\times$ | $\times$ | $\times$ | L H |
| $\begin{array}{\|l\|} \hline \mathrm{H} \\ \mathrm{H} \\ \hline \end{array}$ | $\begin{aligned} & \hline \mathrm{L} \\ & \mathrm{~L} \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \\ & \hline \end{aligned}$ | $\times$ | $\times$ | $\begin{aligned} & \mathrm{L} \\ & \mathbf{H} \end{aligned}$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | $\stackrel{\mathrm{L}}{\mathrm{L}}$ |
| $\begin{array}{r} \mathrm{H} \\ \mathrm{H} \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & \hline \mathrm{L} \\ & \mathrm{~L} \\ & \hline \end{aligned}$ | $\times$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \\ & \hline \end{aligned}$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | $\stackrel{\mathrm{L}}{\mathrm{L}}$ |
| $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \\ & \hline \end{aligned}$ | $\begin{array}{r} \mathrm{H} \\ \mathrm{H} \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | $\times$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \\ & \hline \end{aligned}$ |

IDC CHARACTERISTICS ( $V_{\text {EF: }}=-4.2 \mathrm{to}-4.8 \mathrm{~V}, V_{C C}=V_{C C A}=\mathrm{GND}, T a=0$ to $\left.+85^{\circ} \mathrm{C}\right)$

| Item | Symbol | Fest Condition |  | min | typ | max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Current | 1\% | All input open |  | 76 | 109 | 153 | mA |
|  |  |  | $S_{n}$ input |  |  | 265 | $\mu \mathrm{A}$ |
| Input Current | I'17 | lis lillma | $\mathrm{A}_{n}, \mathrm{~B}_{3}$ input |  |  | 340 | $\mu \mathrm{A}$ |

Sote' As for wher them, refer to the "Comman $1 \times$ Characteristics"

AC CHARACTERISTICS $\left(V_{E E}=-2.2\right.$ to $\left.-2.8 \mathrm{~V}, V_{C C}=V_{C C A}=2.0 \mathrm{~V}\right)$ - HD100163

| Item | Symbol | Test Condition |  | 0 |  | $25^{\circ}{ }^{\circ}$ |  |  | $85^{\circ} \mathrm{C}$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | min | max | min | typ | max | min | max |  |
| Propagation | trin. trint | See test circuit and waveform | $\mathrm{A}_{11}, \mathrm{~B}_{n}$ input to out put | 0.60 | 1.30 | 0.60 | 0.95 | 1.40 | 0.60 | 1.40 | ns |
| Delay Time |  |  | $S_{\text {n }}$ input to output | 1.25 | 2.45 | 1.30 | 1.75 | 2.50 | 1.30 | 2.50 |  |
| Transition Time | trim. 1 mm |  |  | 0.55 | 1.70 | 0.55 | 1.20 | 1.70 | 0.55 | 1.70 | ns |

- HD100163F

| Item | Symbol | Test Condition |  | $0^{\circ}{ }^{\circ}$ |  | $25^{\circ} \mathrm{C}$ |  |  | $85^{\circ} \mathrm{C}$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | min | max | min | typ | max | min | max |  |
| Propagation Delay Time | IV.A. thent | See test circuit and waveform | $\mathrm{A}_{n}, \mathrm{~B}_{\mathrm{n}}$ input to output | 0.70 | 1.40 | 0.80 | 0.95 | 1.50 | 0.80 | 1.50 | ns |
|  |  |  | $\mathrm{S}_{\mathrm{n}}$ input to output | 1.30 | 2.40 | 1.40 | 1.75 | 2.50 | 1.40 | 2.50 |  |
| Transition Time | trih, tTH. |  |  | 0.55 | 1.60 | 0.55 | 1.10 | 1.60 | 0.55 | 1.60 | ns |

Note) The circuits in a test socket or mounted on a printed circuit board and (ransverse air flow greater than 2.5 m s ( 500 linear fpm) is maintained.

