January 2006

FMS6690
Six Channel, 6th Order SD/PS/HD Video Filter Driver

Features

- Three selectable sixth-order 15/32MHz (PS/HD) filters
- Three fixed sixth-order 8MHz (SD) filters with muxed input
- Transparent input clamping
- Single video load drive (2Vpp, 150Ω, A_V = 6dB)
- AC or DC-coupled inputs
- AC or DC-coupled outputs
- DC-coupled outputs eliminate AC-coupling capacitors
- Low power
- 5V only
- Lead (Pb) free packages - TSSOP-20

Applications

- Cable and satellite set-top boxes
- DVD players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

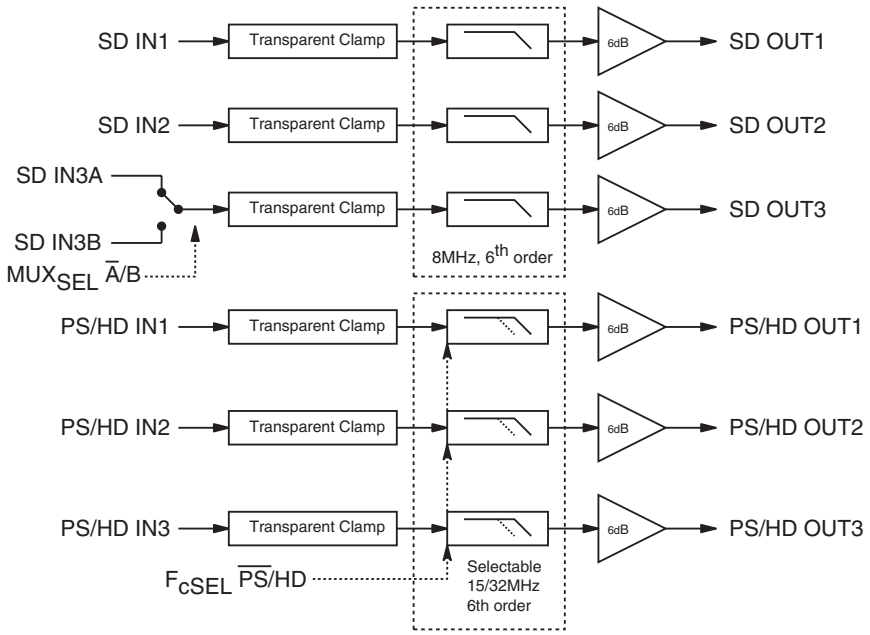
Description

The FMS6690 Low Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Six 6th order Butterworth filters provide improved image quality compared to typical passive solutions. The combination of low power Standard Definition (SD), Progressive Scan (PS), and High Definition (HD) filters greatly simplify DVD video output circuitry. Three channels offer fixed SD filters and feature an additional muxed input, while the other three channels are selectable between PS and HD filters. The FMS6690 offers a fixed gain of 6dB.

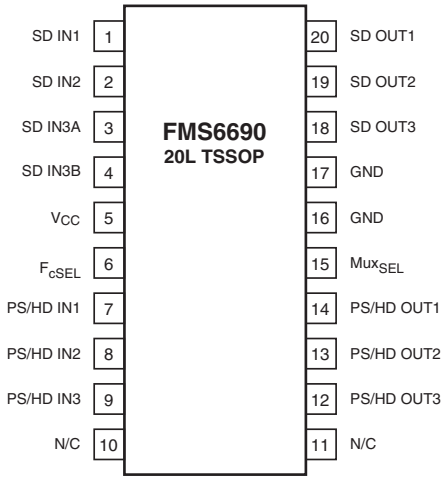
The FMS6690 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required (see applications section for details).

The outputs can drive AC or DC-coupled single (150Ω) video loads. DC-coupling the outputs removes the need for output coupling capacitors. The input DC levels will be offset approximately +280mV at the output.

Block Diagram



Pin Configuration



Pin Assignments

Pin #	Pin	Type	Description
1	SD IN1	Input	SD video input, channel 1
2	SD IN2	Input	SD video input, channel 2
3	SD IN3A	Input	SD video input, channel 3A
4	SD IN3B	Input	SD video input, channel 3B
5	VCC	Input	+5V supply
6	FcSEL	Input	Selects filter corner frequency for pins 7, 8, and 9. “0” = PS, “1” = HD
7	PS/HD IN1	Input	Selectable PS or HD video input, channel 1
8	PS/HD IN2	Input	Selectable PS or HD video input, channel 2
9	PS/HD IN3	Input	Selectable PS or HD video input, channel 3
10	N/C	Input	No Connect
11	N/C	Input	No Connect
12	PS/HD OUT3	Output	Filtered PS or HD video output, channel 3
13	PS/HD OUT2	Output	Filtered PS or HD video output, channel 2
14	PS/HD OUT1	Output	Filtered PS or HD video output, channel 1
15	MUX_{SEL}	Input	Mux selects between channel 3A and 3B inputs. “0” = A, “1” = B
16	GND	Input	Must be tied to Ground
17	GND	Input	Must be tied to Ground
18	SD OUT3	Output	Filtered SD video output, channel 3
19	SD OUT2	Output	Filtered SD video output, channel 2
20	SD OUT1	Output	Filtered SD video output, channel 1

Absolute Maximum Ratings

Parameter	Min	Max	Unit
DC Supply Voltage	-0.3	6	V
Analog and Digital I/O	-0.3	V_{cc} + 0.3	V
Output Current, Any One Channel (Do Not Exceed)		50	mA

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	˚C
Storage Temperature Range	-65		150	˚C
Lead Temperature (Soldering, 10s)			300	˚C
Thermal Resistance ($Theta_{JA}$), JEDEC Standard Multi-Layer Test Boards, Still Air		74		˚C/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	0		70	˚C
Supply Voltage Range	4.75	5.0	5.25	V

DC Electrical Characteristics

T_c = 25˚C, V_{cc} = 5V, R_{source} = 37.5Ω, inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current[1]	no load		60	80	mA
V_{in}	Video Input Voltage Range	Referenced to GND, if DC-coupled		1.4		Vpp
V_{il}	Digital Input Low[1]	F_{cSEL}	0		0.8	V
V_{ih}	Digital Input High[1]	F_{cSEL}	2.4		V_{cc}	V

Standard Definition Electrical Characteristics

T_c = 25˚C, V_{in} = 1V_{pp}, V_{cc} = 5V, R_{source} = 37.5Ω, all inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{SD}	Channel Gain[1]	All SD Channels	5.6	6.0	6.4	dB
f_{1dBSD}	-1dB Bandwidth[1]	All SD Channels	5.2	7.15		MHz
f_{cSD}	-3dB Bandwidth[1]	All SD Channels	6.5	8.0		MHz
f_{SBSD}	Attenuation(stopband reject)[1]	All SD Channels at f = 27MHz	43	50		dB
DG	Differential Gain	All SD Channels		0.7		%
DP	Differential Phase	All SD Channels		1.0		˚
THD	Output Distortion	V_{OUT} = 1.4V_{pp}, 3.58MHz		0.35		%
X_{TALKSD}	Crosstalk (ch-to-ch)	at 1MHz		-54		dB
SNR	Signal-to-Noise Ratio[2]	NTC-7 weighting, 100kHz to 4.2MHz		72		dB
t_{pdSD}	Propagation Delay	Delay from input to output, 4.5MHz		90		ns

Progressive Scan Electrical Characteristics

T_c = 25˚C, V_{in} = 1V_{pp}, V_{cc} = 5V, R_{source} = 37.5Ω, F_{cSEL} = 0, all inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{PS}	Channel Gain[1]	All PS Channels	5.6	6.0	6.4	dB
f_{1dBSPS}	-1dB Bandwidth[1]	All PS Channels	12	14		MHz
f_{cPS}	-3dB Bandwidth[1]	All PS Channels	13	16		MHz
f_{SBPS}	Attenuation(stopband reject)[1]	All PS Channels at f = 54MHz	37	45		dB
THD	Output Distortion (All PS channels)	V_{OUT} = 1.4V_{pp}, 7MHz		0.35		%
X_{TALKPS}	Crosstalk (ch-to-ch)	at 1MHz		-53		dB
SNR	Signal-to-Noise Ratio[2]	unweighted; 100kHz to 15MHz		66		dB
t_{pdPS}	Propagation Delay	Delay from input to output		47		ns

Notes:

1. 100% tested at 25˚C
2. SNR = 20 * log (714mV/rms noise)

High Definition Electrical Characteristics

T_c = 25˚C, V_{in} = 1V_{pp}, V_{cc} = 5V, R_{source} = 37.5Ω, F_{cSEL} = 1, all inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω loads, referenced to 400kHz; unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{HD}	Channel Gain[1]	All HD Channels	5.6	6.0	6.4	dB
f_{1dBHD}	-1dB Bandwidth[1]	All HD Channels	28	31		MHz
f_{cHD}	-3dB Bandwidth[1]	All HD Channels	30	34		MHz
f_{SBHD}	Attenuation(stopband reject)[1]	All HD Channels at f = 74.25MHz	30	41		dB
THD	Output Distortion (all HD channels)	V_{OUT} = 1.4V_{pp}, 22MHz		0.9		%
X_{TALKHD}	Crosstalk (ch-to-ch)	at 1MHz		-54		dB
SNR	Signal-to-Noise Ratio[2]	unweighted, 100kHz to 30MHz		60		dB
t_{pdHD}	Propagation Delay	Delay from input to output		25		ns

Notes:

1. 100% tested at 25˚C
2. SNR = 20 * log (714mV/rms noise)

Typical Performance Characteristics

T_c = 25˚C, V_{in} = 1V_{pp}, V_{CC} = 5V, R_{source} = 37.5Ω, inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω loads; unless otherwise noted.

Figure 1. SD Gain vs. Frequency

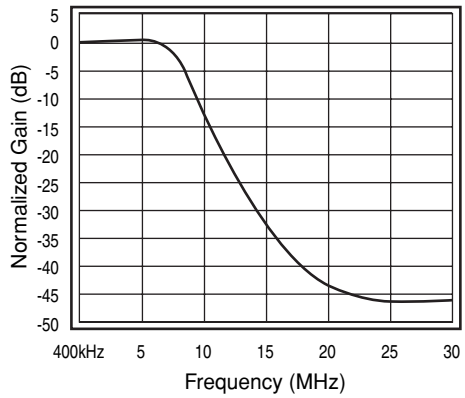


Figure 2. SD Flatness vs. Frequency

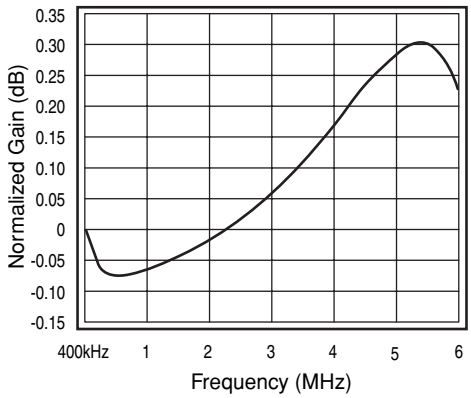


Figure 3. PS Gain vs. Frequency

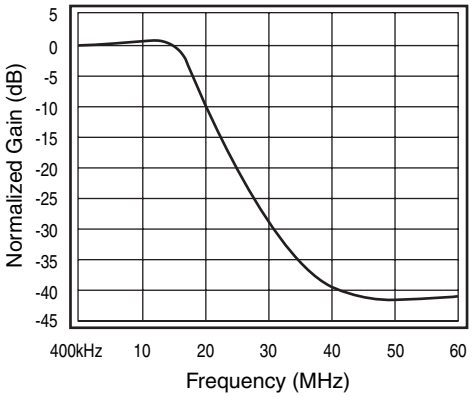


Figure 4. PS Flatness vs. Frequency

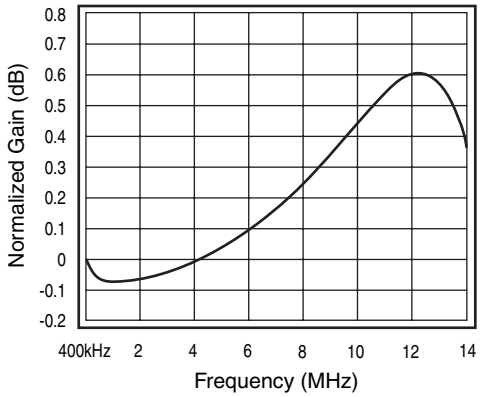


Figure 5. HD Gain vs. Frequency

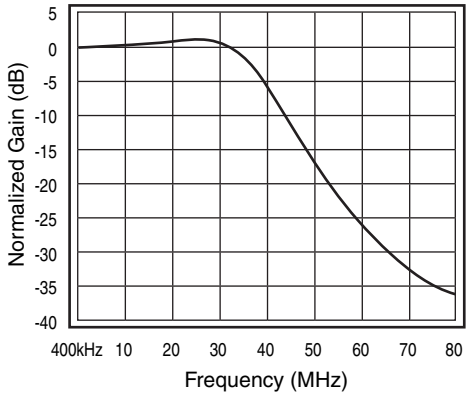
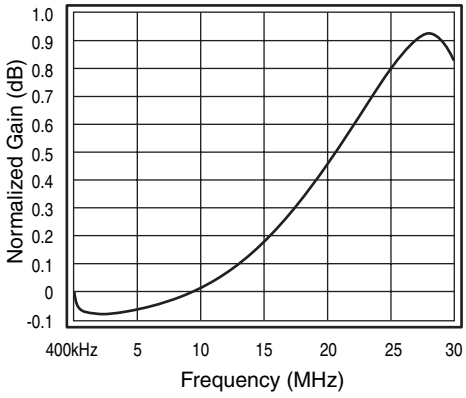


Figure 6. HD Flatness vs. Frequency



Typical Performance Characteristics

T_c = 25˚C, V_{in} = 1V_{pp}, V_{CC} = 5V, R_{source} = 37.5Ω, inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω loads; unless otherwise noted.

Figure 7. SD Group Delay vs. Frequency

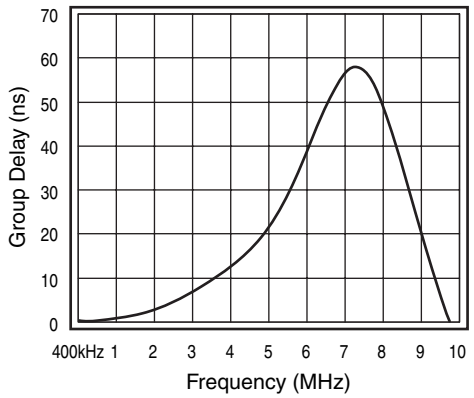


Figure 8. Noise vs. Frequency

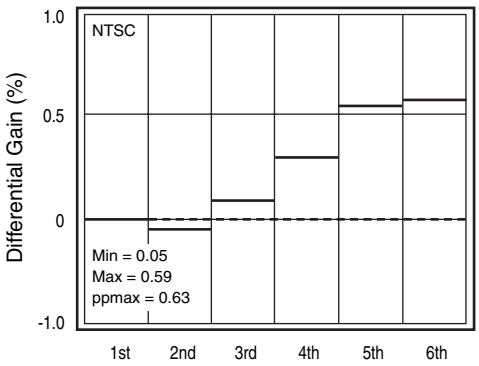


Figure 9. PS Group Delay vs. Frequency

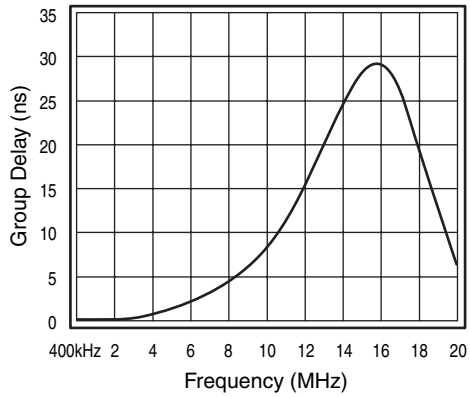


Figure 10. SD Differential Gain

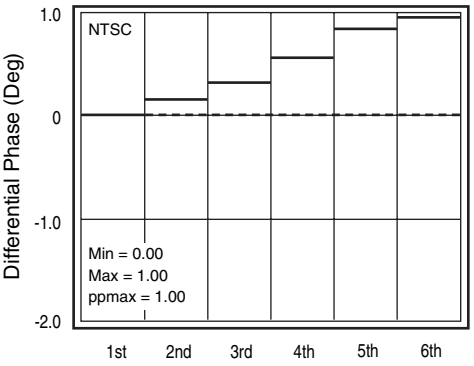
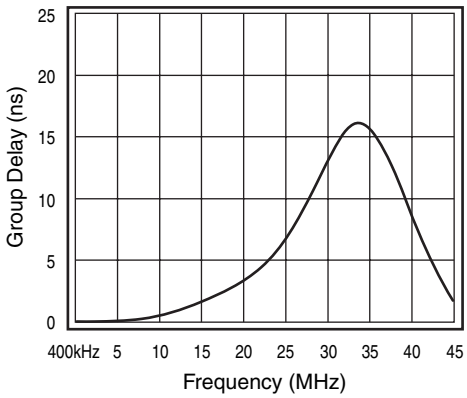


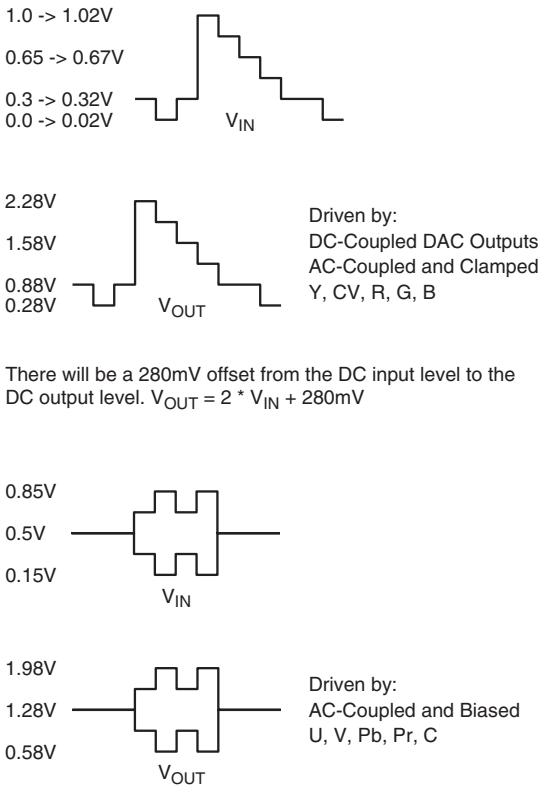
Figure 11. HD Group Delay vs. Frequency



Applications Information

Functional Description

The FMS6690 Low Cost Video Filter (LCVF) provides 6dB gain (9dB optional, contact factory for further information) from input to output. In addition, the input will be slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in the diagram below.



There will be a 280mV offset from the DC input level to the DC output level. $V_{OUT} = 2 * V_{IN} + 280mV$

Figure 12. Typical Voltage Levels

The FMS6690 provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp will not operate. This allows DAC outputs to directly drive the FMS6690 without an AC coupling capacitor. The worst-case sync tip compression due to the clamp will not exceed 7mV. The input level set by the clamp combined with the internal DC offset will keep the output within its acceptable range. When the input is AC-coupled, the diode clamp will set the sync tip (or lowest voltage) just below ground.

For symmetric signals like C, U, V, Cb, Cr, Pb and Pr, the average DC bias is fairly constant and the inputs can be AC-coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown below:

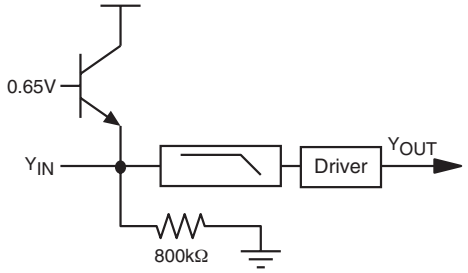


Figure 13. Input Clamp Circuit

I/O Configurations

For DC-coupled DAC drive with DC-coupled outputs, use this configuration:

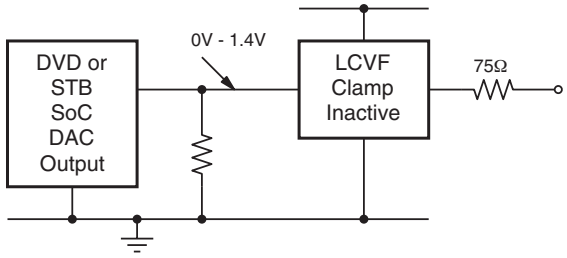


Figure 14. DC-coupled Inputs and Outputs

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC-coupled as follows:

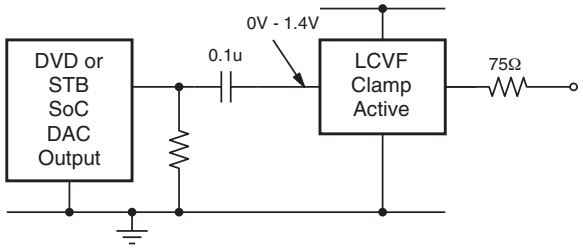


Figure 15. AC-coupled Inputs, DC-coupled Outputs

When the FMS6690 is driven by an unknown external source or a SCART switch with its own clamping circuitry, the inputs should be AC-coupled as follows:

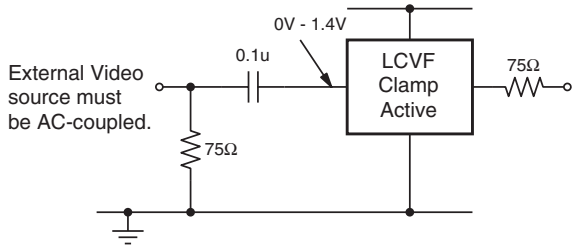


Figure 16. SCART Configuration with DC-coupled Outputs

The same method can be used for biased signals with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is 800kΩ ±20% so the external resistance should be 7.5MΩ to set the DC level to 500mV. If a pull-up resistance less than 7.5MΩ is desired, an external pull-down can be added such that the DC input level is set to 500mV.

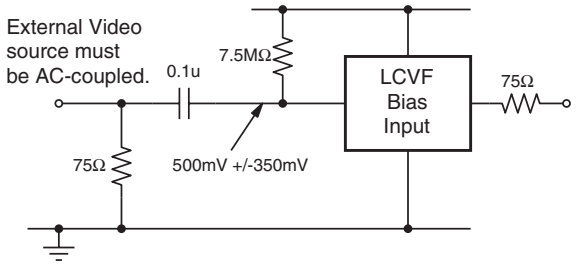


Figure 17. Biased SCART with DC-coupled Outputs

The same circuits can be used with AC-coupled outputs if desired.

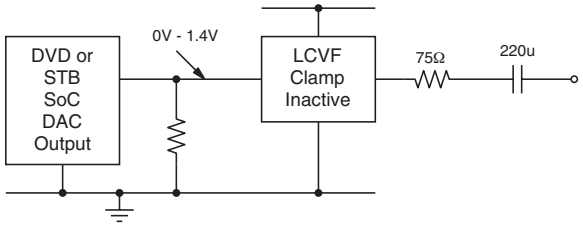


Figure 18. DC-coupled Inputs, AC-coupled Outputs

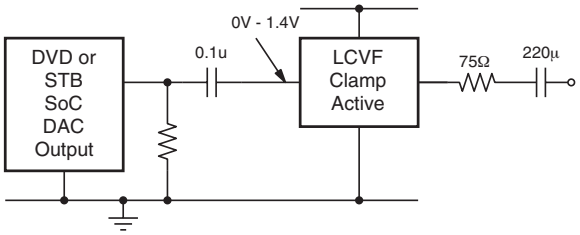


Figure 19. AC-coupled Inputs, AC-coupled Outputs

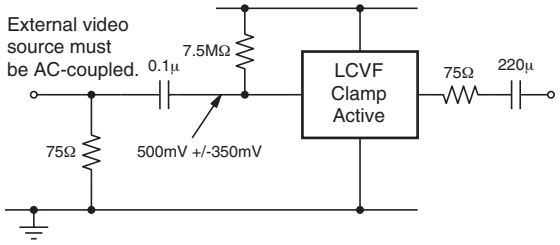


Figure 20. Biased SCART with AC-coupled Outputs

NOTE: The video tilt or line time distortion will be dominated by the AC-coupling capacitor. The value may need to be increased beyond 220µF in order to obtain satisfactory operation in some applications.

Power Dissipation

The FMS6690 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the FMS6690's power dissipation and internal temperature rise.

$T_j = T_A + P_d \bullet \Theta_{JA}$

where $P_d = P_{CH1} + P_{CH2} + P_{CHx}$

and $P_{CHx} = V_s \bullet I_{CH} - (V_O^2/R_L)$

where

$V_O = 2V_{in} + 0.280V$

$I_{CH} = (I_{CC} / 6) + (V_O/R_L)$

V_{in} = RMS value of input signal

I_{CC} = 60mA

V_s = 5V

R_L = channel load resistance

Board layout can also affect thermal characteristics. Refer to the *Layout Considerations* Section for more information.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6690DEMO, to use as a guide for layout and to aid in device testing and characterization. The FMS6690DEMO is a 4-layer board with a full power and ground plane. Following this layout configuration will provide the optimum performance and thermal characteristics. For optimum results, follow the steps below as a basis for high frequency layout:

- Include 10µF and 0.1µF ceramic bypass capacitors
- Place the 10µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- For multi-layer boards, use a large ground plane to help dissipate heat
- For 2 layer boards, use a ground plane that extends beyond the device by at least 0.5"
- Minimize all trace lengths to reduce series inductances

Typical Application Diagram

The following circuit may be used for direct DC-coupled drive by DACs with an output voltage range of 0V to 1.4V. AC-coupled or DC-coupled outputs may be used with AC-coupled outputs offering slightly lower power dissipation.

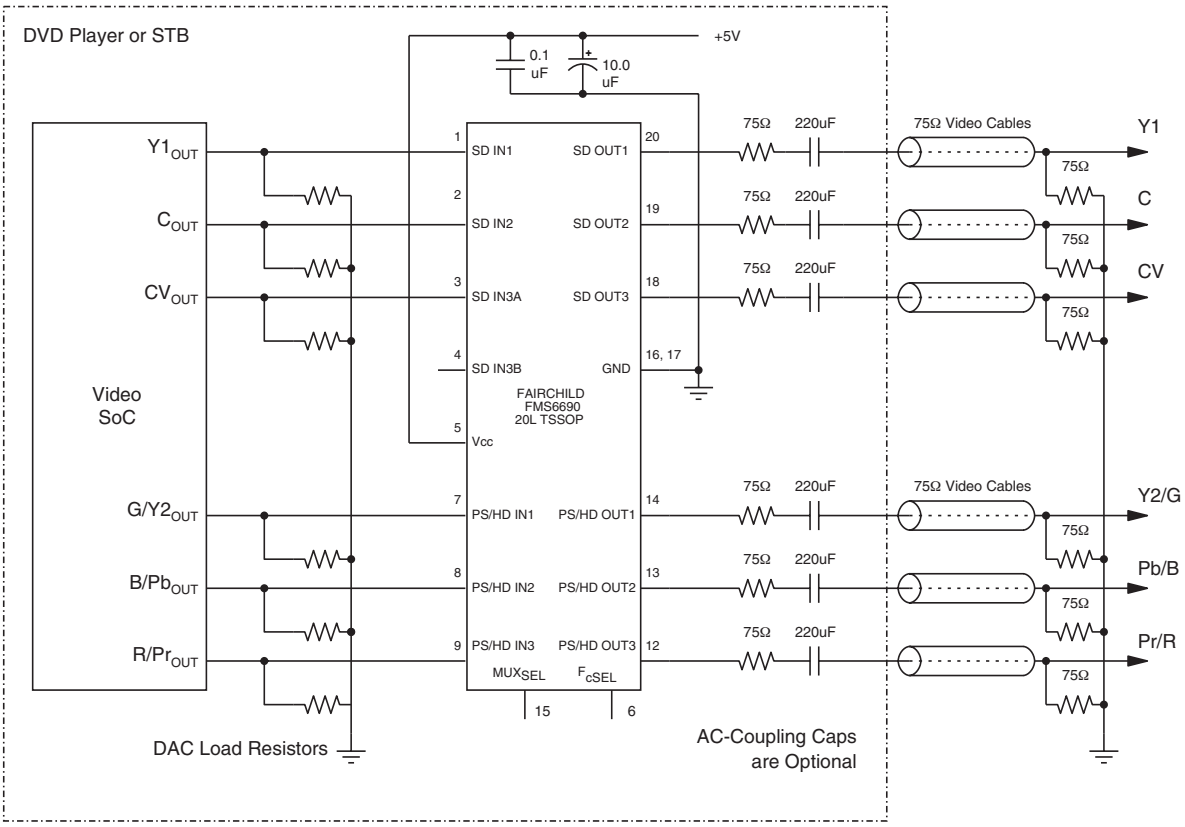
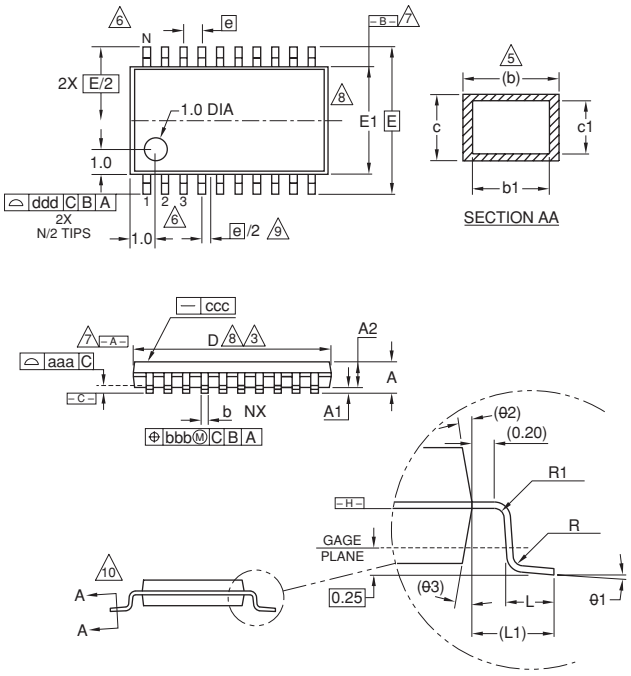


Figure 21. Typical Application Diagram

Mechanical Dimensions

20-Lead Thin Shrink Outline Package (TSSOP)



TSSOP-20			
SYMBOL	**MIN**	**NOM**	**MAX**
A	–	–	1.10
A1	0.05	–	0.15
A2	0.85	0.90	0.95
L	0.50	0.60	0.75
R	0.09	–	–
R1	0.09	–	–
b	0.19	–	0.30
b1	0.19	0.22	0.25
c	0.09	–	0.20
c1	0.09	–	0.16
θ1	0°	–	8°
L1	1.0 REF		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		
e	0.65 BSC		
θ2	12° REF		
θ3	12° REF		
D	6.50	6.50	6.60
E1	4.30	4.40	4.50
E	6.4 BSC		
e	0.65 BSC		
N	20		

NOTES:

1 All dimensions are in millimeters (angle in degrees).

2 Dimensioning and tolerancing per ASME Y14.5–1994.

3 Dimensions "D" does not include mold flash, protusions or gate burrs. Mold flash protusions or gate burrs shall not exceed 0.15 per side .

4 Dimension "E1" does not include interlead flash or protusion. Interlead flash or protusion shall not exceed 0.25 per side.

5 Dimension "b" does not include dambar protusion. Allowable dambar protusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar connot be located on the lower radius of the foot. Minimum space between protusion and adjacent lead is 0.07mm for 0.5mm pitch packages.

6 Terminal numbers are shown for reference only.

7 Datums – A – and – B – to be determined at datum plane – H –.

8 Dimensions "D" and "E1" to be determined at datum plane – H –.

9 This dimensions applies only to variations with an even number of leads per side. For variation with an odd number of leads per side, the "center" lead must be coincident with the package centerline, Datum A.

10 Cross sections A – A to be determined at 0.10 to 0.25mm from the leadtip.

Ordering Information

Model	Part Number	Lead Free	Package	Container	Pack Qty
FMS6690	FMS6690MTC20	Yes	TSSOP-20	Rail	94
FMS6690	FMS6690MTC20X	Yes	TSSOP-20	Reel	2500

Temperature range for all parts: 0˚C to 70˚C.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

