FAIRCHILD
SEMICONDUCTOR®

July 2001

FGH30N6S2 / FGP30N6S2 / FGB30N6S2

600V, SMPS II Series N-Channel IGBT

General Description

The FGH30N6S2, FGP30N6S2, and FGB30N6S2 are Low Gate Charge, Low Plateau Voltage SMPS II IGBTs combining the fast switching speed of the SMPS IGBTs along with lower gate charge and plateau voltage and avalanche capability (UIS). These LGC devices shorten delay times, and reduce the power requirement of the gate drive. These devices are ideally suited for high voltage switched mode power supply applications where low conduction loss, fast switching times and UIS capability are essential. SMPS II LGC devices have been specially designed for:

- Power Factor Correction (PFC) circuits
- Full bridge topologies
- Half bridge topologies
- Push-Pull circuits
- Uninterruptible power supplies
- Zero voltage and zero current switching circuits

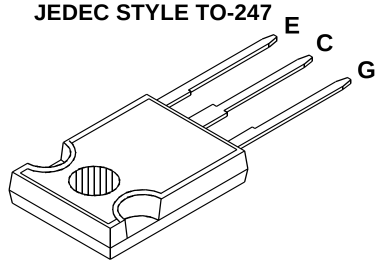
Formerly Developmental Type TA49367.

Features

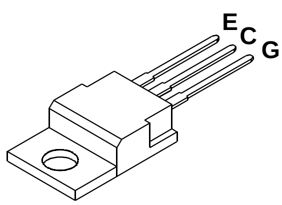
- 100kHz Operation at 390V, 14A
- 200kHZ Operation at 390V, 9A
- 600V Switching SOA Capability
- Typical Fall Time. . . . . 90ns at TJ = 125^{o}C
- Low Gate Charge . . . . 23nC at V_{GE} = 15V
- Low Plateau Voltage . . . . .6.5V Typical
- UIS Rated 150mJ
- Low Conduction Loss

Package

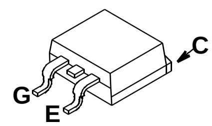
JEDEC STYLE TO-247



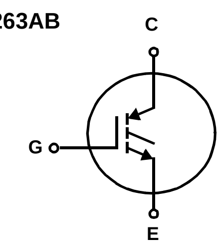
JEDEC STYLE TO-220AB



JEDEC STYLE TO-263AB



Symbol



Device Maximum Ratings T_C= 25°C unles s otherwise noted

Symbol	Parameter	Ratings	Units
BV_{CES}	Collector to Emitter Breakdown Voltage	600	V
I_{C25}	Collector Current Continuous, T_C = 25°C	45	A
I_{C110}	Collector Current Continuous, T_C = 110°C	20	A
I_{CM}	Collector Current Pulsed (Note 1)	108	A
V_{GES}	Gate to Emitter Voltage Continuous	±20	V
V_{GEM}	Gate to Emitter Voltage Pulsed	±30	V
SSOA	Switching Safe Operating Area at T_J = 150°C , Figure 2	60A at 600V	
E_{AS}	Pulsed Avalanche Energy, I_{CE} = 20A, L = 1.3mH, V_{DD} = 50V	150	mJ
P_D	Power Dissipation Total T_C = 25°C	167	W
	Power Dissipation Derating T_C > 25°C	1.33	W/°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
T_{STG}	Storage Junction Temperature Range	-55 to 150	°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. Pulse width limited by maximum junction temperature.

Package Marking and Ordering Information

Device Marking	Device	Package	Tape Width	Quantity
30N6S2	FGH30N6S2	TO-247	-	-
30N6S2	FGP30N6S2	TO-220AB	-	-
30N6S2	FGB30N6S2	TO-263AB	24mm	800

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off State Characteristics							
BV_{CES}	Collector to Emitter Breakdown Voltage	I_C = 250μA, V_{GE} = 0		600	-	-	V
BV_{ECS}	Emitter to Collector Breakdown Voltage	I_C = 10mA, V_{GE} = 0		10	25	-	V
I_{CES}	Collector to Emitter Leakage Current	V_{CE} = 600V	T_J = 25° C	-	-	100	μA
			T_J = 125°C	-	-	2	mA
I_{GES}	Gate to Emitter Leakage Current	V_{GE} = ± 20V		-	-	±250	nA
On State Characteristics							
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = 12A, V_{GE} = 15V	T_J = 25°C	-	2.0	2.5	V
			T_J = 125°C	-	1.7	2.0	V
Dynamic Characteristics							
$Q_{G(ON)}$	Gate Charge	I_C = 12A, V_{CE} = 300V	V_{GE} = 15V	-	23	29	nC
			V_{GE} = 20V	-	26	33	nC
$V_{GE(TH)}$	Gate to Emitter Threshold Voltage	I_C = 250μA, V_{CE} = 600V		3.5	4.3	5.0	V
V_{GEP}	Gate to Emitter Plateau Voltage	I_C = 12A, V_{CE} = 300V		-	6.5	8.0	V
Switching Characteristics							
SSOA	Switching SOA	T_J = 150°C , R_G = 10Ω, V_{GE} = 15V, L = 100μH, V_{CE} = 600V		60	-	-	A
$t_{d(ON)I}$	Current Turn-On Delay Time	IGBT and Diode at T_J = 25° C, I_{CE} = 12A, V_{CE} = 390V, V_{GE} = 15V, R_G = 10Ω, L = 200μH, Test Circuit - Figure 20		-	6	-	ns
t_{rI}	Current Rise Time			-	10	-	ns
$t_{d(OFF)I}$	Current Turn-Off Delay Time			-	40	-	ns
t_{fI}	Current Fall Time			-	53	-	ns
E_{ON1}	Turn-On Energy (Note 2)			-	55	-	μJ
E_{ON2}	Turn-On Energy (Note 2)			-	110	-	μJ
E_{OFF}	Turn-Off Energy (Note 3)			-	100	150	μJ
$t_{d(ON)I}$	Current Turn-On Delay Time	IGBT and Diode at T_J = 125°C, I_{CE} = 12A, V_{CE} = 390V, V_{GE} = 15V, R_G = 10Ω, L = 200μH, Test Circuit - Figure 20		-	11	-	ns
t_{rI}	Current Rise Time			-	17	-	ns
$t_{d(OFF)I}$	Current Turn-Off Delay Time			-	73	100	ns
t_{fI}	Current Fall Time			-	90	100	ns
E_{ON1}	Turn-On Energy (Note 2)			-	55	-	μJ
E_{ON2}	Turn-On Energy (Note 2)			-	160	200	μJ
E_{OFF}	Turn-Off Energy (Note 3)			-	250	350	μJ
Thermal Characteristics							
$R_{\theta JC}$	Thermal Resistance Junction-Case			-	-	0.75	°C/ W

NOTE:

2. Values for two Turn-On loss conditions are shown for the convenience of the circuit designer. E_{ON1} is the turn-on loss of the IGBT only. E_{ON2} is the turn-on loss when a typical diode is used in the test circuit and the diode is at the same T_J as the IGBT. The diode type is specified in figure 20.

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

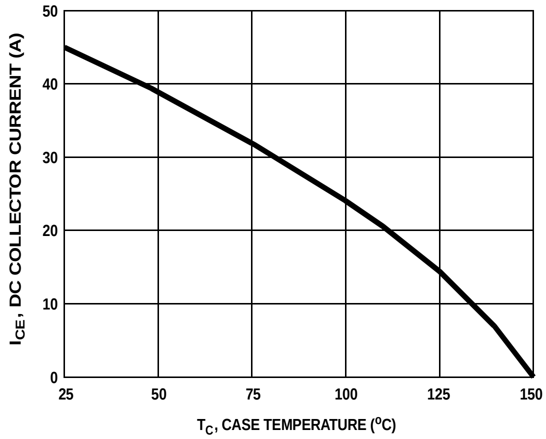


Figure 1. DC Collector Current vs Case Temperature

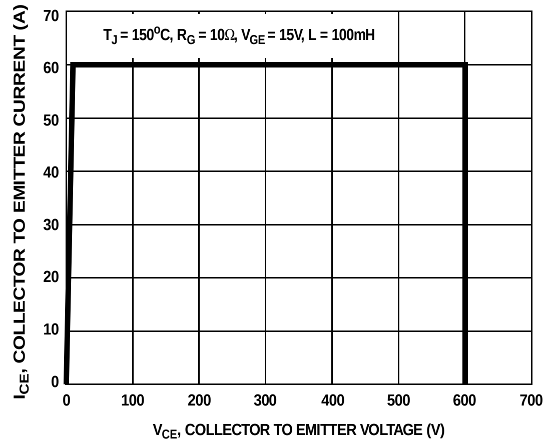


Figure 2. Minimum Switching Safe Operating Area

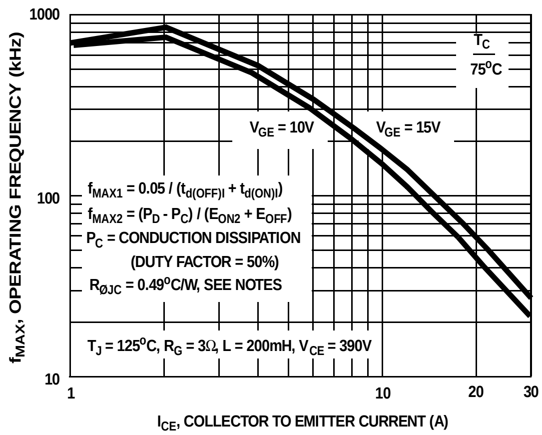


Figure 3. Operating Frequency vs Collector to Emitter Current

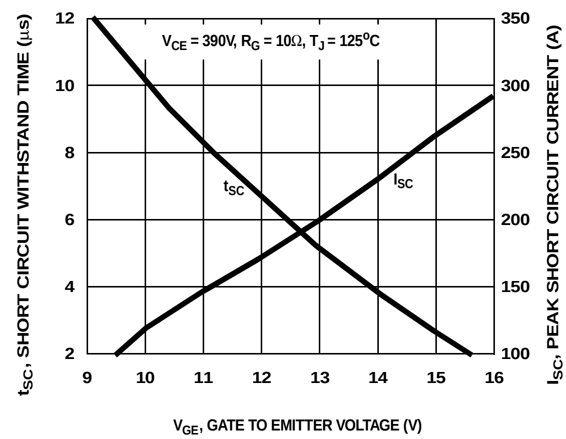


Figure 4. Short Circuit Withstand Time

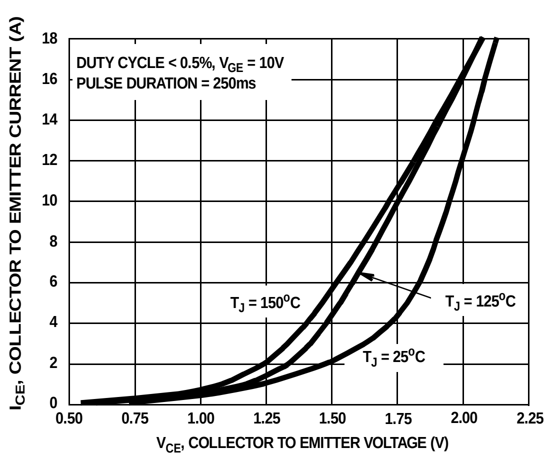


Figure 5. Collector to Emitter On-State Voltage

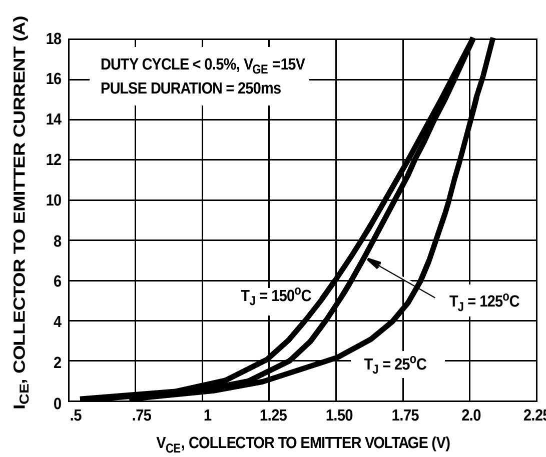


Figure 6. Collector to Emitter On-State Voltage

Typical Performance Curves (Continued)

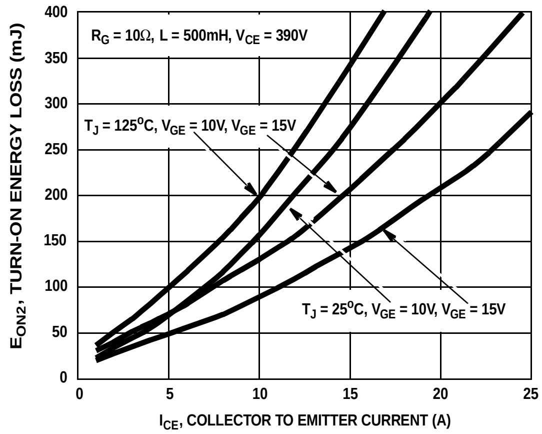


Figure 7. Turn-On Energy Loss vs Collector to Emitter Current

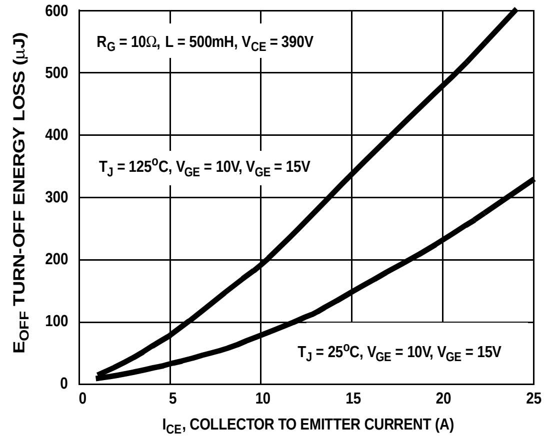


Figure 8. Turn-Off Energy Loss vs Collector to Emitter Current

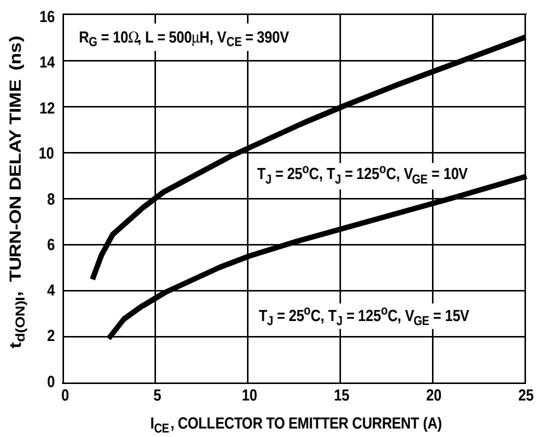


Figure 9. Turn-On Delay Time vs Collector to Emitter Current

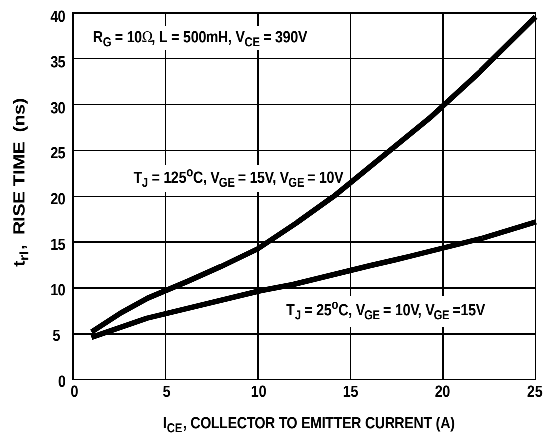


Figure 10. Turn-On Rise Time vs Collector to Emitter Current

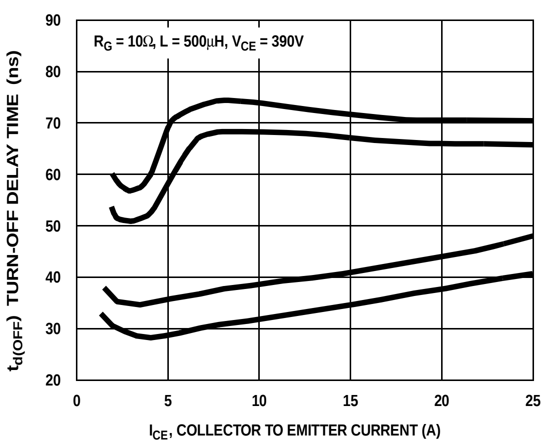


Figure 11. Turn-Off Delay Time vs Collector to Emitter Current

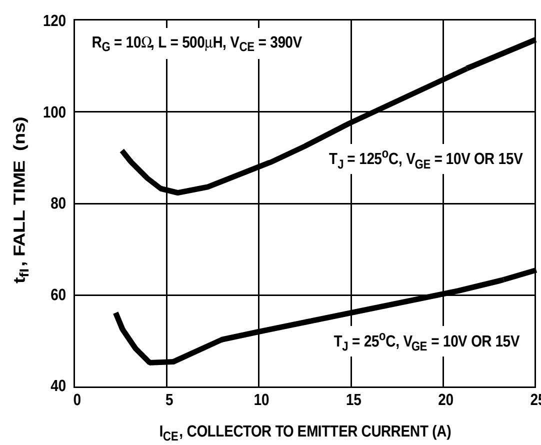


Figure 12. Fall Time vs Collector to Emitter Current

Typical Performance Curves (Continued)

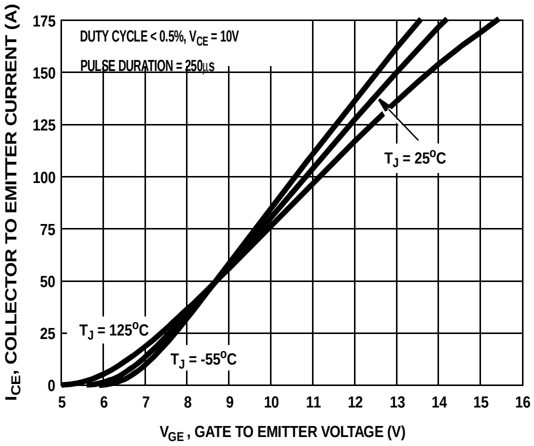


Figure 13. Transfer Characteristic

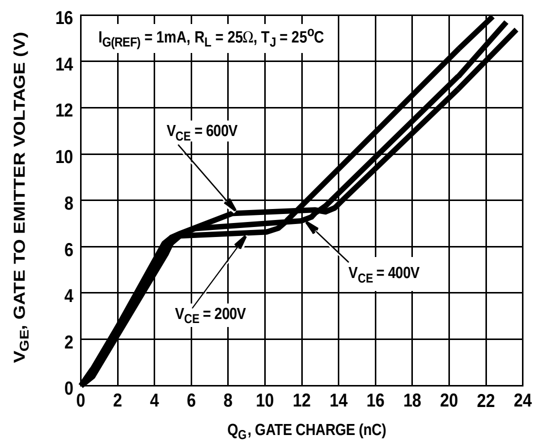


Figure 14. Gate Charge

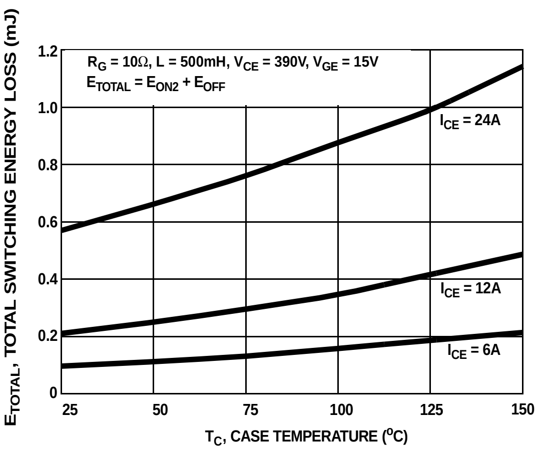


Figure 15. Total Switching Loss vs Case Temperature

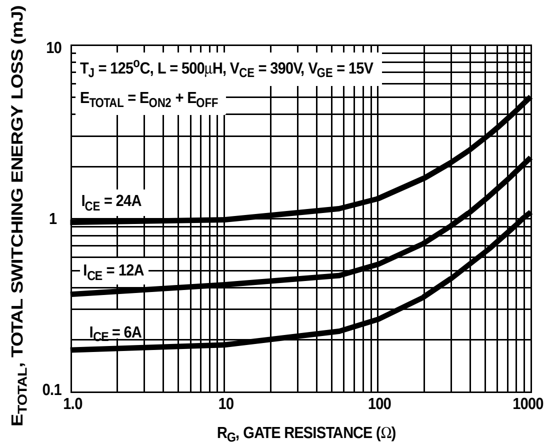


Figure 16. Total Switching Loss vs Gate Resistance

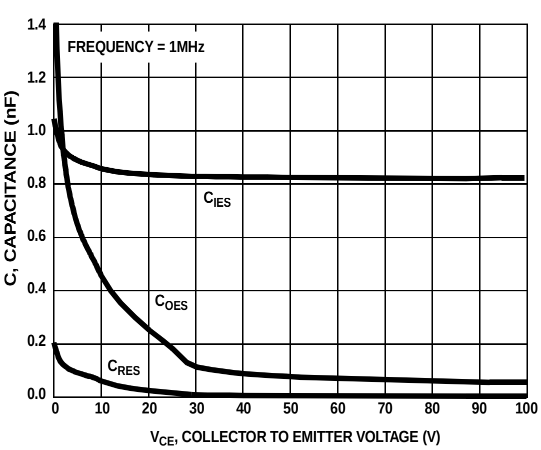


Figure 17. Capacitance vs Collector to Emitter Voltage

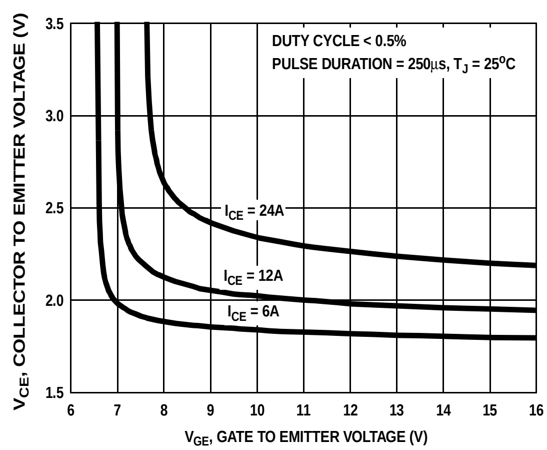


Figure 18. Collector to Emitter On-State Voltage vs Gate to Emitter Voltage

Typical Performance Curves (Continued)

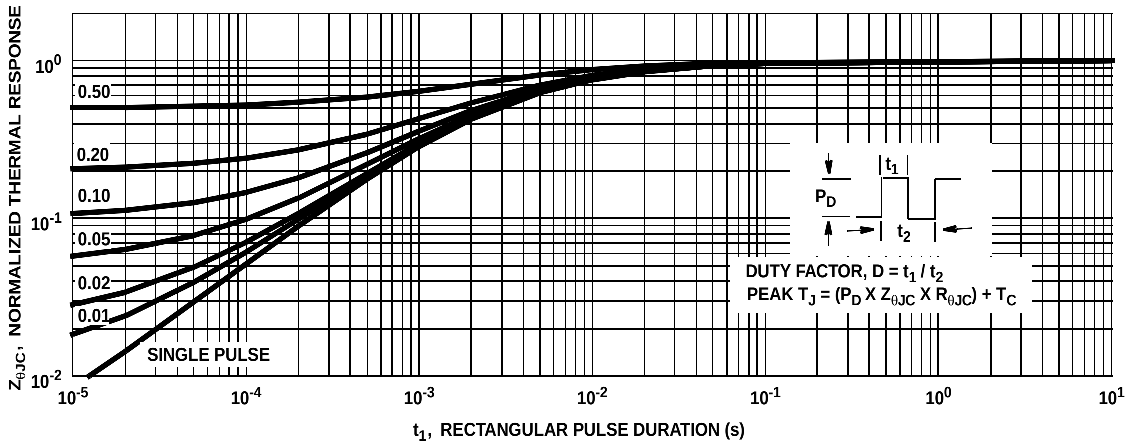


Figure 19. IGBT Normalized Transient Thermal Impedance, Junction to Case

Test Circuit and Waveforms

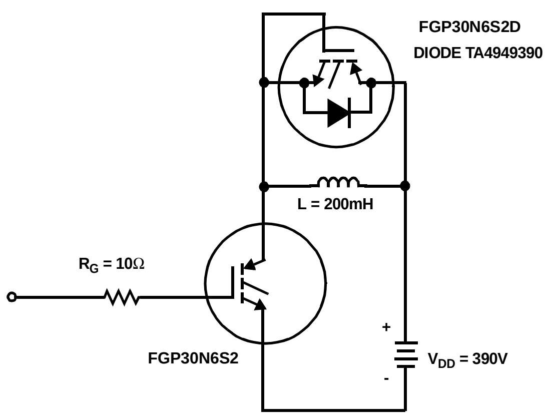


Figure 20. Inductive Switching Test Circuit

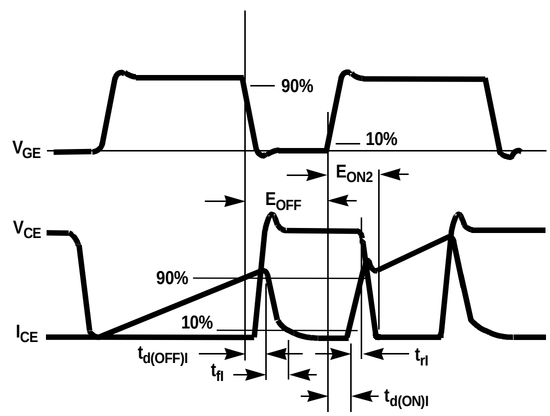


Figure 21. Switching Test Waveforms

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 21. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JM}. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON2})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON2} and E_{OFF} are defined in the switching waveforms shown in Figure 21. E_{ON2} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$)

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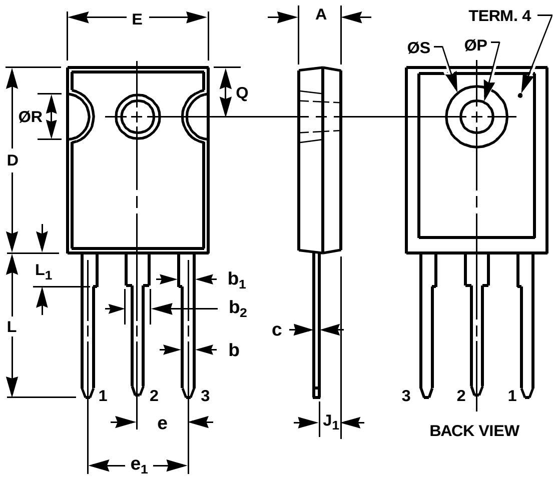
TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



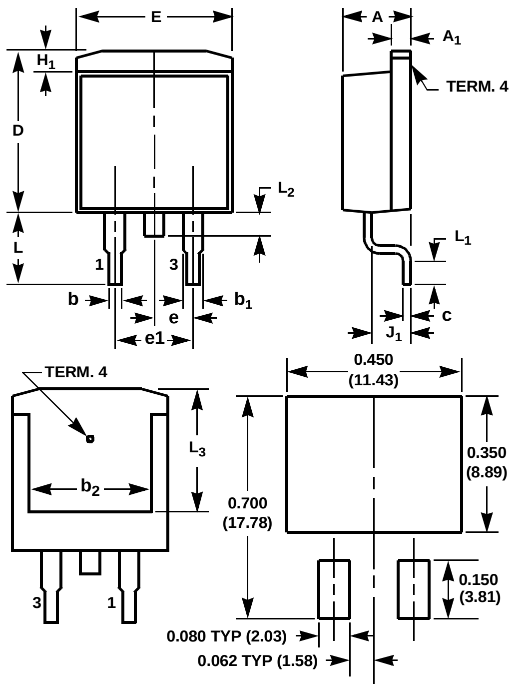
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

TO-263AB

SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

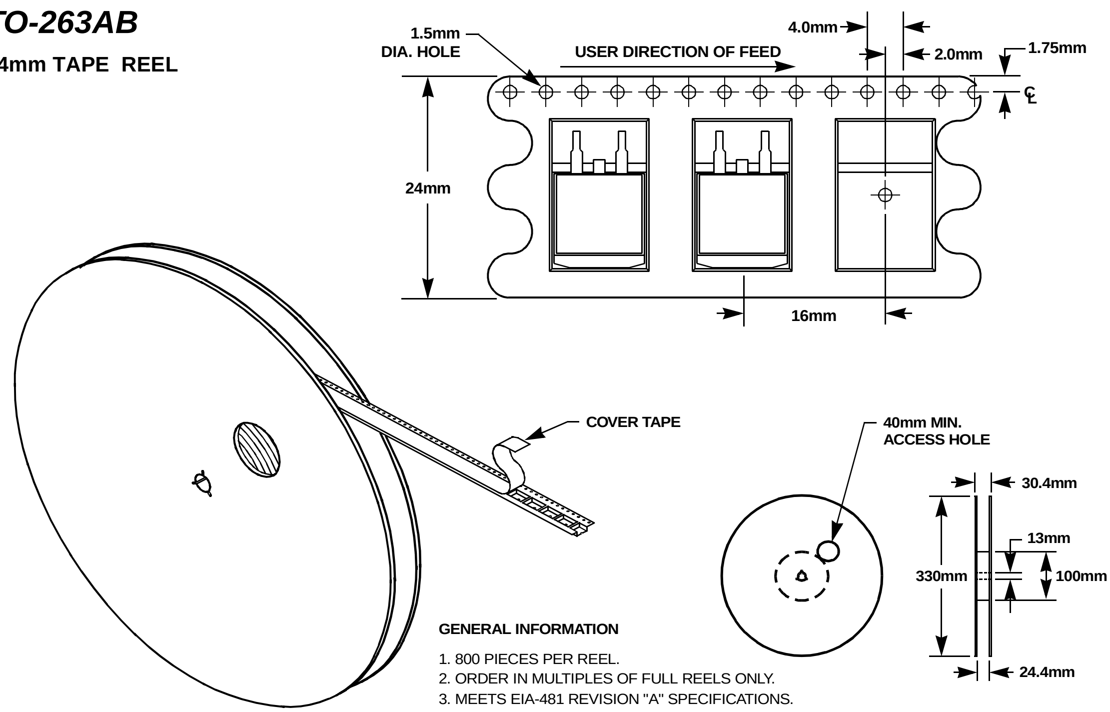
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4, 5
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	3
L_3	0.315	-	8.01	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 10 dated 5-99.

TO-263AB

24mm TAPE REEL

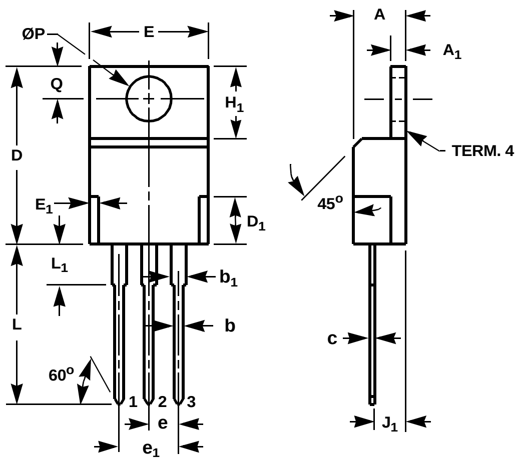


GENERAL INFORMATION

1. 800 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

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Definition of Terms

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