

**April 2013** 

# FGD4536 360 V PDP Trench IGBT

#### **Features**

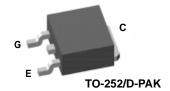
- · High Current Capability
- Low Saturation Voltage: V<sub>CE(sat)</sub> = 1.59 V @ I<sub>C</sub> = 50 A
- High Input Impedance
- · Fast Switching
- · RoHS Compliant

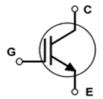
## **Applications**

• PDP TV, Consumer Appliances

## **General Description**

Using novel trench IGBT technology, Fairchild<sup>®</sup>'s new series of trench IGBTs offer the optimum performance for consumer appliances and PDP TV applications where low conduction and switching losses are essential.





## **Absolute Maximum Ratings**

Symbol	Description		Ratings	Unit
V <sub>CES</sub>	Collector to Emitter Voltage		360	V
V <sub>GES</sub>	Gate to Emitter Voltage		± 30	V
I <sub>C pulse(1)*</sub>	Pulsed Collector Current	$@ T_C = 25^{\circ}C$	220	Α
P <sub>D</sub>	Maximum Power Dissipation	$@ T_C = 25^{\circ}C$	125	W
• Б	Maximum Power Dissipation	$@ T_C = 100^{\circ}C$	50	W
T <sub>J</sub>	Operating Junction Temperature		-55 to +150	°C
T <sub>stg</sub>	Storage Temperature Range		-55 to +150	
TL	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds		300	°C

#### **Thermal Characteristics**

Symbol	Parameter	Тур.	Max.	Unit
$R_{\theta JC}(IGBT)$	Thermal Resistance, Junction to Case	-	1.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	-	62.5	°C/W

#### Notes

(1) Half Sine Wave, D < 0.01, pluse width <  $1\mu$ sec

<sup>\*</sup> Ic\_pluse limited by max Tj

# **Package Marking and Ordering Information**

<b>Device Marking</b>	Device	Package	Reel Size	Tape Width	Quantity
FGD4536	FGD4536TM	TO252	380mm	16mm	-

# Electrical Characteristics of the IGBT $T_C = 25\%$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	teristics					
BV <sub>CES</sub>	Collector to Emitter Breakdown Voltage	$V_{GE} = 0V, I_{C} = 250\mu A$	360	-	-	V
$\frac{\Delta BV_{CES}}{\Delta T_{J}}$	Temperature Coefficient of Breakdown Voltage	$V_{GE} = 0V, I_C = 250\mu A$	-	0.4	-	V/°C
I <sub>CES</sub>	Collector Cut-Off Current	$V_{CE} = V_{CES}, V_{GE} = 0V$	-	-	100	μΑ
I <sub>GES</sub>	G-E Leakage Current	$V_{GE} = V_{GES}, V_{CE} = 0V$	-	-	±400	nA
On Charac	teristics					
V <sub>GE(th)</sub>	G-E Threshold Voltage	$I_{C} = 250 \mu A, V_{CE} = V_{GE}$	2.4	3.3	4.0	V
		I <sub>C</sub> = 20A, V <sub>GE</sub> = 15V	-	1.19	-	V
V	Collector to Emitter	I <sub>C</sub> = 30A, V <sub>GE</sub> = 15V	-	1.33	-	V
V <sub>CE(sat)</sub> Collector to Emitter Saturation Voltage		I <sub>C</sub> = 50A, V <sub>GE</sub> = 15V, T <sub>C</sub> = 25°C	-	1.59	1.8	V
		I <sub>C</sub> = 50A, V <sub>GE</sub> = 15V, T <sub>C</sub> = 125°C	-	1.66	-	V
Dynamic C	haracteristics					
C <sub>ies</sub>	Input Capacitance		-	1295	-	pF
C <sub>oes</sub>	Output Capacitance	V <sub>CE</sub> = 30V <sub>,</sub> V <sub>GE</sub> = 0V, f = 1MHz	-	56	-	pF
C <sub>res</sub>	Reverse Transfer Capacitance	1 - 1W1112	-	43	-	pF
Switching	Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time		-	5	-	ns
t <sub>r</sub>	Rise Time	$V_{CC} = 200V, I_{C} = 20A,$	-	20	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$R_G = 5\Omega$ , $V_{GE} = 15V$ , ResistiveLoad, $T_C = 25^{\circ}C$	-	41	-	ns
t <sub>f</sub>	Fall Time	, 0	-	182	-	ns
t <sub>d(on)</sub>	Turn-On Delay Time		-	5	-	ns
t <sub>r</sub>	Rise Time	$V_{CC}$ = 200V, $I_{C}$ = 20A, $R_{G}$ = 5 $\Omega$ , $V_{GE}$ = 15V, Resistive Load, $T_{C}$ = 125°C	-	21	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	43	-	ns
t <sub>f</sub>	Fall Time		-	249	-	ns
Qg	Total Gate Charge	V = 200V L : 20A	-	47	-	nC
Q <sub>ge</sub>	Gate to Emitter Charge	$V_{CE} = 200V_{,} I_{C} = 20A_{,}$ $V_{GE} = 15V_{,}$	-	5.4	-	nC
Q <sub>gc</sub>	Gate to Collector Charge		-	15	-	nC

**Figure 1. Typical Output Characteristics** 

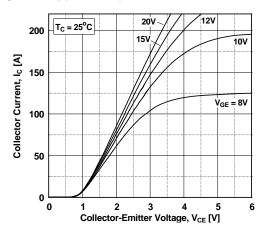


Figure 3. Typical Saturation Voltage Characteristics

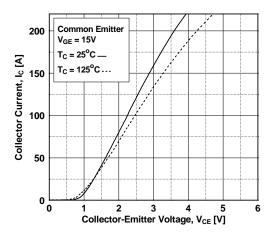


Figure 5. Saturation Voltage vs. Case
Temperature at Variant Current Level

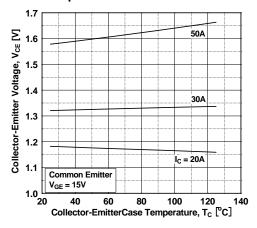


Figure 2. Typical Output Characteristics

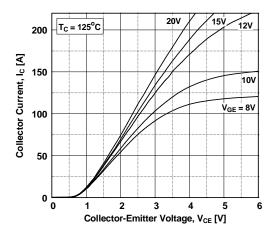


Figure 4. Transfer Characteristics

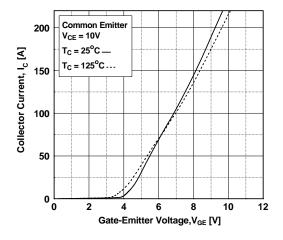


Figure 6. Saturation Voltage vs.  $V_{GE}$ 

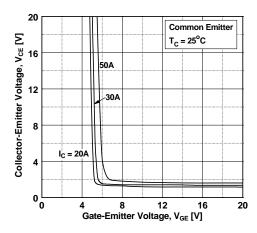


Figure 7. Saturation Voltage vs. V<sub>GE</sub>

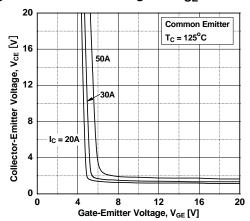


Figure 9. Gate charge Characteristics

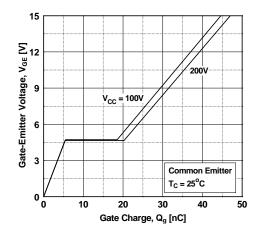
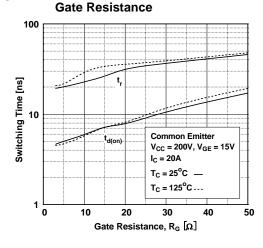


Figure 11. Turn-on Characteristics vs.



**Figure 8. Capacitance Characteristics** 

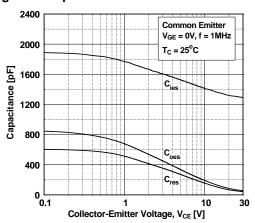


Figure 10. SOA Characteristics

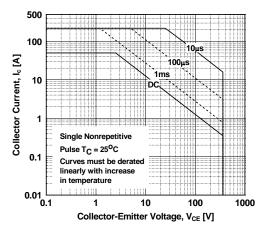


Figure 12. Turn-off Characteristics vs.
Gate Resistance

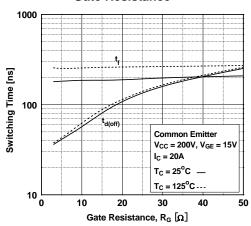


Figure 13. Turn-on Characteristics vs. Collector Current

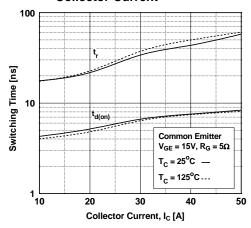


Figure 14. Turn-off Characteristics vs. Collector Current

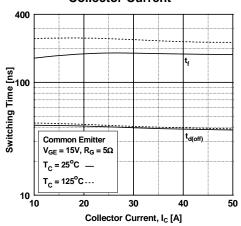


Figure 15. Switching Loss vs. Gate Resistance

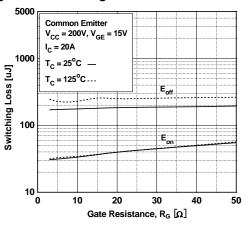


Figure 16. Switching Loss vs. Collector Current

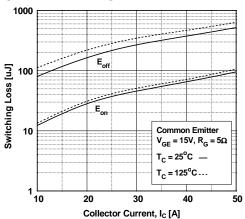


Figure 17. Turn off Switching SOA Characteristics

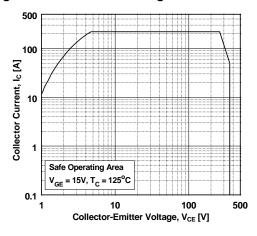
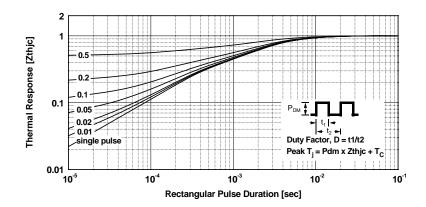
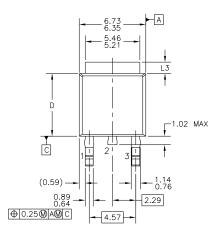


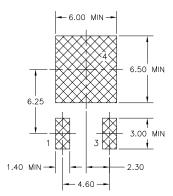
Figure 18.Transient Thermal Impedance of IGBT



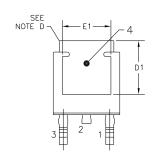
#### **Mechanical Dimensions**

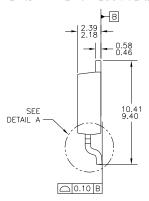
# **D-PAK**

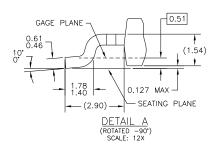




LAND PATTERN RECOMMENDATION







- NOTES: UNLESS OTHERWISE SPECIFIED

  A) ALL DIMENSIONS ARE IN MILLIMETERS.

  B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.

  C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

  D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.

  E) DIMENSIONS L5,D,E1&D1 TABLE:

  | DEFION AB | OPTION AB | L3 0.89-1.27 1.552-2.03 |
  | L3 0.89-1.27 1.552-2.03 |
  | L1 4.32 WIM 3.81 WIM | L4.57 WIM |
  | D1 5.21 WIM 1.8.17 WIM |
  | F) PRESENCE OF TRIMMED CENTER LEAD



PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.		
No Identification Needed Full Production Datasheet contains final specifications. Fairchild Semiconduct make changes at any time without notice to improve the design		Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.		
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