

**MKT Capacitors**

**S B 32520**  
**... B 32529**

SIEMENS AKTIENGESELLSCHAFT 47E D

A-05-17-05

**Metalized polyester film capacitors in accordance with DIN 44112**

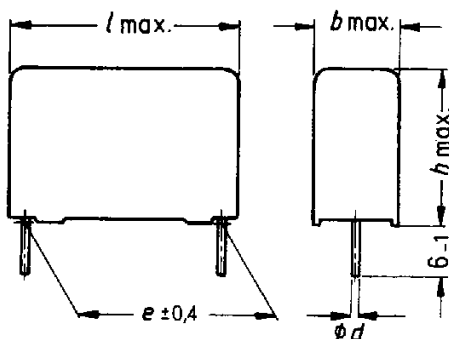
$V_R = 63$  to  $630$  Vdc

**With quality assessment according to CECC 30401-043, edition 1, June 1983.**

Self-healing capacitor with polyethyleneterephthalate dielectric. Encapsulated in a flame-retardant rectangular plastic case (in accordance with UL 94 V-0). Epoxy resin sealed for humidity resistance. For improved solderability, the package is provided with spacers. Connections: parallel leads, tinned, plug-in in the lead spacing. Particularly suited for space-saving assembly at high packing density on any PC board.

**Packaging on continuous tapes**

Capacitors with 5 mm and 7.5 mm lead spacing, as well as capacitors with a lead spacing of 7.5/5 mm (leads crimped to a lead spacing of 5 mm) are also available on continuous tape. For taping instructions and ordering code information refer to page 46.



Dimensions in mm

$l$	Lead spacing $e$	dia. $d$
7.5	5	0.5
10	7.5	0.6
13	10	0.6
18	15	0.8
27	22.5	0.8
31.5	27.5	0.8

<p><b>DIN climatic category</b> in acc. with DIN 40040 Lower category temperature Upper category temperature Humidity category</p> <p>Failure rate (<math>40^\circ\text{C}/104^\circ\text{F}</math>, <math>V_R</math>)</p> <p>Load duration</p>	<p><b>F M E / J R</b></p> <p><b>F</b> - <math>55^\circ\text{C}/-67^\circ\text{F}</math> <b>M</b> <math>+100^\circ\text{C}/+212^\circ\text{F}</math><sup>1)</sup> <b>E</b> average relative humidity <math>\leq 75\%</math>; 95% for 30 days per year continuously; 85% for the remaining days occasionally; rare, brief dew precipitation permitted <b>J</b> <math>30 \times 10^{-9}/\text{h} = 30</math> fit for conversion tables for other stresses and temperatures see page 42. <b>R</b> <math>\geq 10^5</math> h</p>
<p><b>Failure criteria</b> Total failure Failure due to variations</p>	<p>Short or open circuit Capacitance change <math>\frac{\Delta C}{C} &gt; \pm 10\%</math> Dissipation factor <math>\tan \delta &gt; 2 \times</math> upper category values Insulation resistance <math>&lt; 150 \text{ M}\Omega</math> (<math>\leq 0.33 \mu\text{F}</math>) <math>&lt; 50 \text{ s}</math> (<math>&gt; 0.33 \mu\text{F}</math>)</p>

<sup>1)</sup> Shelf and service life at temperatures  $> 100 \dots 125^\circ\text{C}/212 \dots 257^\circ\text{F}$ , 1000 h max.,  $V_C = 0.5 V_R$ .

MKT-Capacitors

A-05-17-05

B32520  
... B32529

SI SIEMENS AKTIENGESELLSCHAFT 47E D

Lead spacing		LS 27.5mm			
Rated dc voltage		100V	250V	400V	630V
Rated capacitance		Dimensions b x h x l (mm) and ordering code			
CR	Tolerance	B32524 -			
4700	pF				
6800	pF				
0.01	μF				
0.015	μF				
0.022	μF				
0.033	μF				
0.047	μF				
0.068	μF				
0.1	μF				
0.15	μF	± 20% M ± 10% K ± 5% J			
0.22	μF				
0.33	μF				11.5x21.0x31.5 M8334
0.47	μF			13.5x23.0x31.5 M8474	
0.68	μF			11.5x21.0x31.5 M6684	15.0x24.5x31.5 M8684
1	μF			11.5x21.0x31.5 M6105	
1.5	μF		11.5x21.0x31.5 M3155	13.5x23.0x31.5 M6155	
2.2	μF		11.5x21.0x31.5 M3225		
3.3	μF		13.5x23.0x31.5 M3335		
4.7	μF	11.5x21.0x31.5 M1475	15.0x24.5x31.5 M3475		
6.8	μF	13.5x23.0x31.5 M1685			
10.0	μF	15.0x24.5x31.5 M1106			

**MKT Capacitors**

A-05-17-05

B 32520  
... B 32529

SIEMENS AKTIENGESELLSCHAFT 47E D

**IEC climatic category**  
in acc. with DIN IEC 68-1

**55/100/56**

**Damp heat test**  
in acc. with  
DIN IEC 68-2-3

**Conditions**

Test temperature +40°C/+104°F  
Relative humidity  $(93 \pm 2) \%$   
Test duration 56 days

**Test criteria**

Capacitance change  $\frac{\Delta C}{C} \leq \pm 5\%$   
Dissipation factor change  $\Delta \tan \delta$  at 1 kHz  $\leq 5 \times 10^{-3}$   
Insulation resistance  $\geq 50\%$  of the minimum value as supplied

**Resistance to vibration**

Test Fc in acc. with  
DIN IEC 68-2-6:  
vibration, sinusoidal

Duration of endurance conditioning 6 h  
Frequency range 10... 55 Hz  
Displacement amplitude 0.75 mm (conforming to 98.1 m/s<sup>2</sup> max. or to 10 g)  
At 10 Hz... 2 kHz capacitors with LS  $\geq 22.5$  mm must additionally be fixed at the case.

**Resistance to soldering heat<sup>1)</sup>**  
Test Tb in acc. with  
DIN IEC 68-2-20

Solder bath temperature max. 260°C/500°F  
Soldering duration max. 5 s  
Capacitance change  $\frac{\Delta C}{C} \leq \pm 2\%$

**Resistance to cleaning agents**

Refer to section "General Information", page 37.

**Capacitance drift  $i_z$**

$\pm 3\%$

**Self inductance**

Lead spacing (mm)	5	7.5	10	15	22.5	27.5
Self inductance (approx. nH)	5	8	9	10	20	20

**Dissipation factor  $\tan \delta$**   
measured at 20°C/68°F

Upper limits/Average production values

	$C_R < 0.1 \mu F$	$C_R \geq 0.1 \dots < 1 \mu F$	$C_R \geq 1 \mu F$
at 1 kHz	8/ $5 \times 10^{-3}$	10/ $6 \times 10^{-3}$	10/ $7 \times 10^{-3}$
at 10 kHz	15/ $12 \times 10^{-3}$	20/ $15 \times 10^{-3}$	-
at 100 kHz	30/ $18 \times 10^{-3}$	-	-

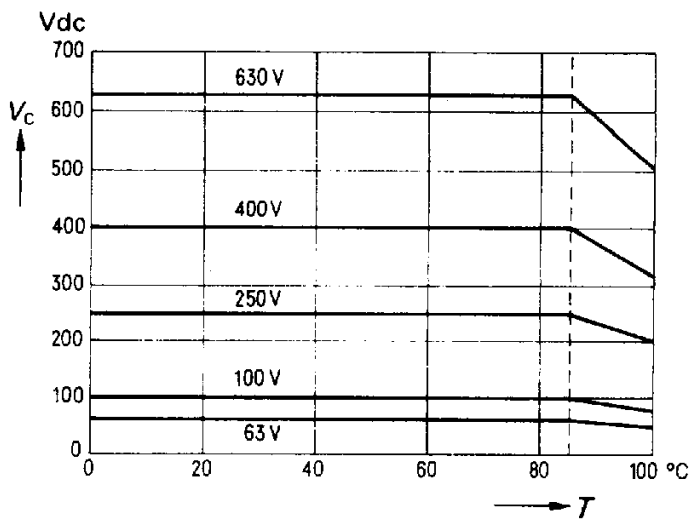
A-05-17-05

B 32520  
...B 32529

SI SIEMENS AKTIENGESELLSCHAFT 47E D

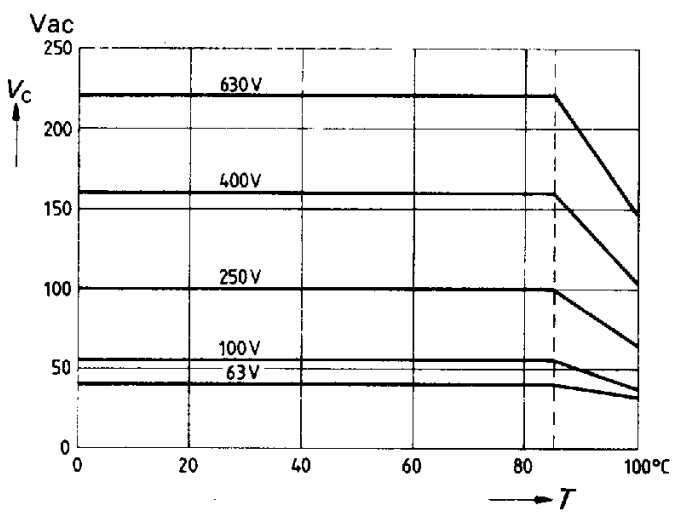
**Category voltage  $V_C$  versus temperature  $T$  at dc operation**

2000 h max.  $1.25 \times V_C$   
for milliseconds (e.g. switchings)  $1.50 \times V_C$

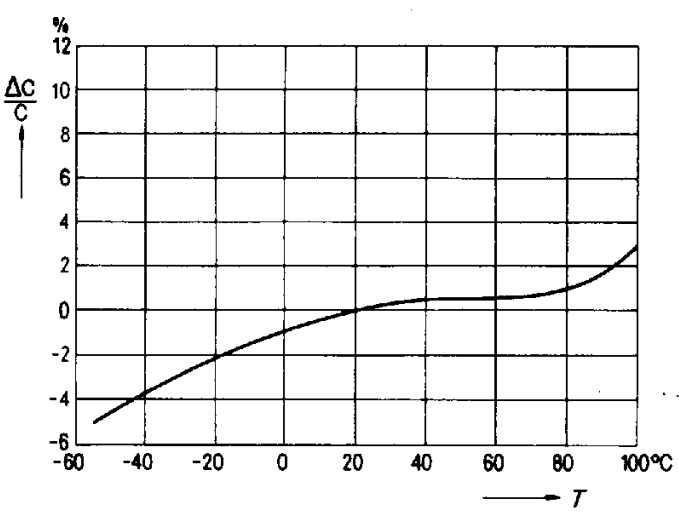


**Category voltage  $V_C$ <sup>1)2)</sup> versus temperature  $T$  at ac operation at 50 Hz**

max. 2000 hours  $1.25 \times V_C$   
for milliseconds (e.g. switchings)  $1.50 \times V_C$



**Capacitance change  $\frac{\Delta C}{C}$  versus temperature  $T$  (typical values, measured at 1 kHz)**



1) The sum of the dc voltage and the peak value of an ac voltage superimposed on the dc voltage may not exceed the rated voltage.  
2) Capacitors of the 630 Vdc series can be used as 250 Vac line power parallel capacitors if it is ensured that voltage peaks occurring occasionally during operation do not exceed 1000 V.

**MKT Capacitors**

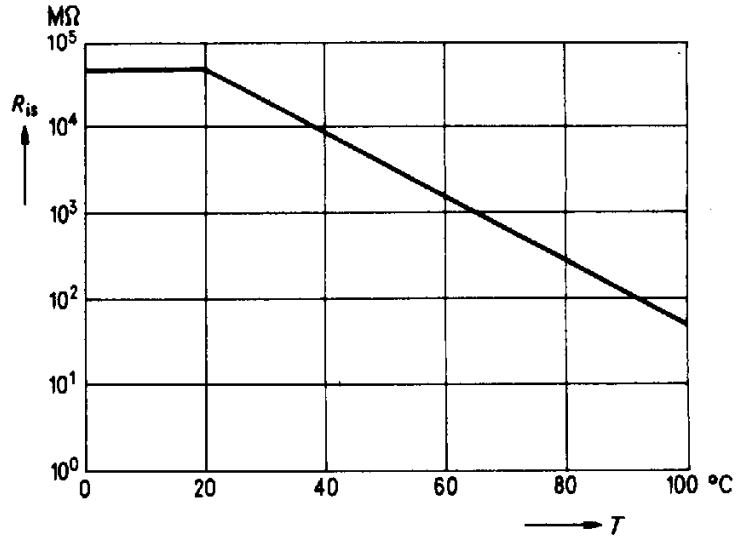
A-05-17-05

B 32520  
... B 32529

SIEMENS AKTIENGESELLSCHAFT 47E D

**Insulation resistance  $R_{is}$  versus temperature  $T$**

Typical values measured at 20°C/68°F and a relative humidity  $\leq 65\%$



**Insulation resistance  $R_{is}$  and time constant  $\tau$**

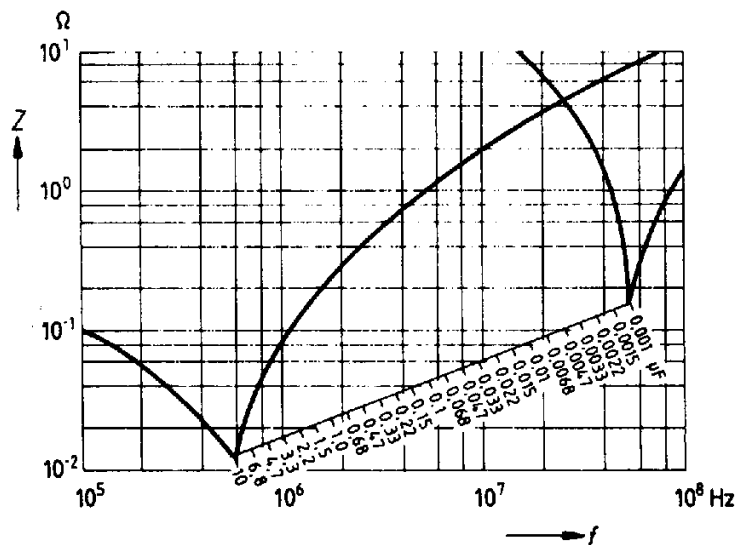
Minimum value as supplied<sup>1)</sup>

$V_R$	$C_R \leq 0.33 \mu F$	$C_R > 0.33 \mu F$
$\leq 100 V$	3750 MΩ	1250 sec
$\geq 250 V$	7500 MΩ	2500 sec

Average value as supplied

$V_R$	$C_R \leq 0.33 \mu F$	$C_R > 0.33 \mu F$
$\leq 100 V$	> 30 000 MΩ	> 10 000 sec
$\geq 250 V$	> 75 000 MΩ	> 25 000 sec

**Impedance  $Z$  versus frequency  $f$  (typical values)**



<sup>1)</sup> The indicated values apply at the time of delivery. During the service life, the insulation may temporarily decrease to approx. 10% of the value at the time of delivery, especially if the max. permissible relative humidity of 95% of the humidity category E is applied for a longer period, or if the capacitor is operated close to the upper category temperature.

MKT-Capacitors

A-05-17-05

B32520  
... B32529

SIEMENS AKTIENGESELLSCHAFT 47E D

Pulse Handling Capability

Rated Voltage		LS 5	LS 7.5	LS 10	LS 15	LS 22.5	LS 27.5
63 V –	$U_{SS}/\tau$ in V/ $\mu$ s $k_0$ in V <sup>2</sup> / $\mu$ s	150 20.000	80 10.000	50 6.300	30 3.800	2 250	
100 V –		200 40.000	100 20.000	75 15.000	50 10.000	2.5 500	2 400
250 V –		400 125.000	200 100.000	150 75.000	100 50.000	4 2.000	3 1.500
400 V –		500 320.000	250 200.000	175 150.000	125 100.000	7 5.600	5 4.000
630 V –					15 19.000	10 12.600	8 10.000

For a voltage deviation of  $V_{pp} < V_R$  the value of the permissible voltage rate of rise  $V_{pp}/\tau$  can be multiplied by the factor  $V_R/V_{pp}$ . The data of the nomogram must be considered in case of periodic pulses. See also calculation example in section "General Information", para. 5.2.6.

AC power handling capability at higher frequencies

The maximum permissible peak voltage  $\hat{V}$  for sinusoidal and non-sinusoidal voltages (pulse, sawtooth, trapezoidal voltages) can be determined from the nomogram.

The nomogram is based on 10°C/50°F inherent temperature rise of the capacitor; this must be considered during operation with regard to the permissible upper category temperature.

The following limits may not be exceeded:

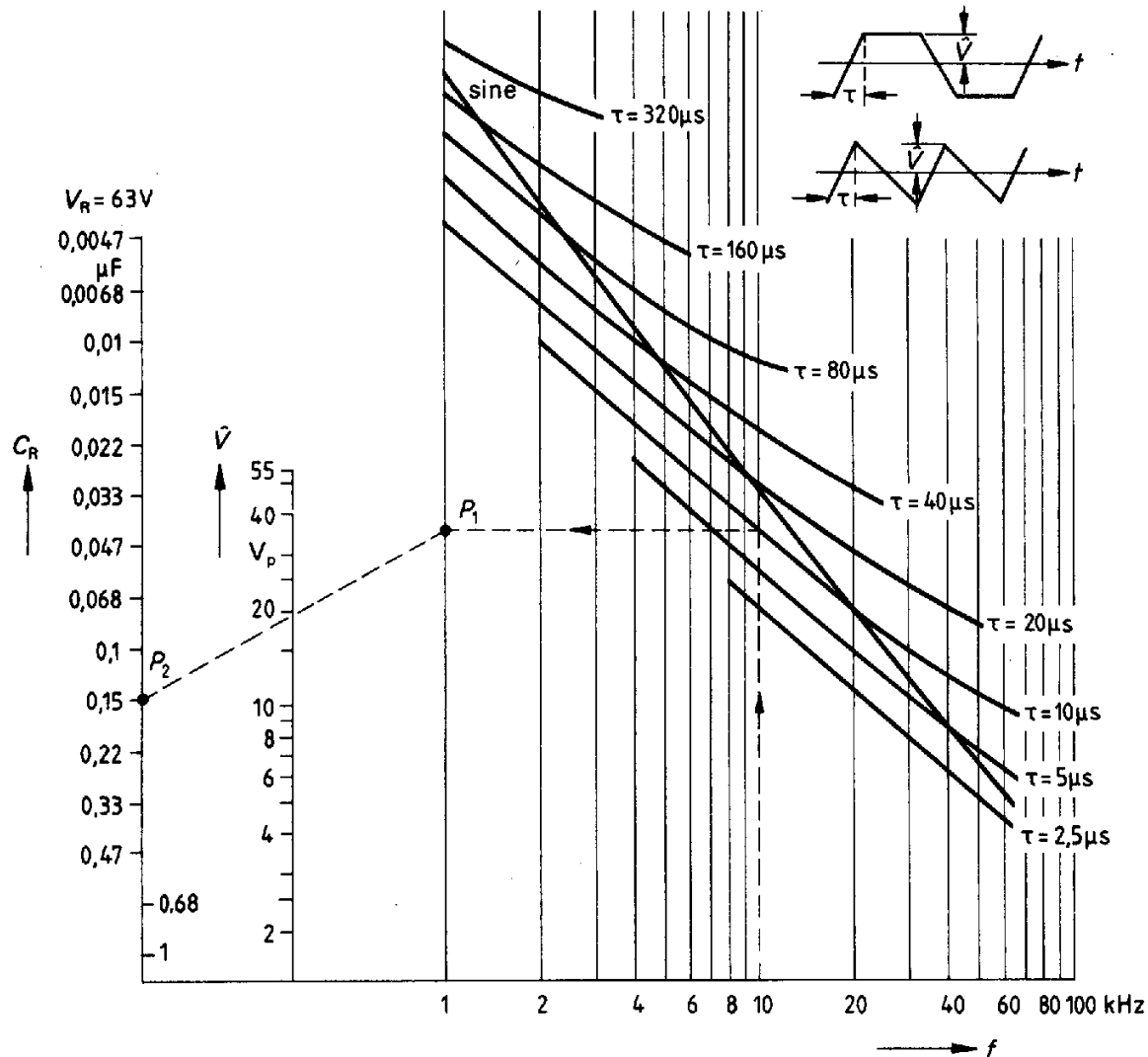
Rated dc voltage $V_R$	63 V	100 V	250 V	400 V	630 V
Limit voltage $\hat{V}_l$	55 V	85 V	140 V	224 V	280 V

**B 32529, LS 5 mm**

**Nomogram to determine the permissible peak voltage  $\hat{V}$**

Determine the intersections  $P_1$  and  $P_2$  according to the plotted example. The intersection of the line connecting  $P_1$  with  $P_2$  and the  $\hat{V}$  scale gives the maximum permissible peak voltage.

In case of a trapezoidal voltage load, the second harmonic frequency must be considered. With sinusoidal voltage load, the "sine" characteristic applies.



**Example:**

- |                      |                        |   |                    |
|----------------------|------------------------|---|--------------------|
| $f = 10$ kHz         | (repetition frequency) | } | intersection $P_1$ |
| $\tau = 10$ $\mu s$  | (rise time)            |   |                    |
| $C_R = 0.15$ $\mu F$ | (capacitance)          | } | intersection $P_2$ |
| $V_R = 63$ V         | (rated voltage)        |   |                    |

According to the dashed line in the above graph, this results in a max. peak voltage  $\hat{V}$  of approx. 19 V.

A-05-17-05

B 32520

SIEMENS AKTIENGESELLSCHAFT 47E D

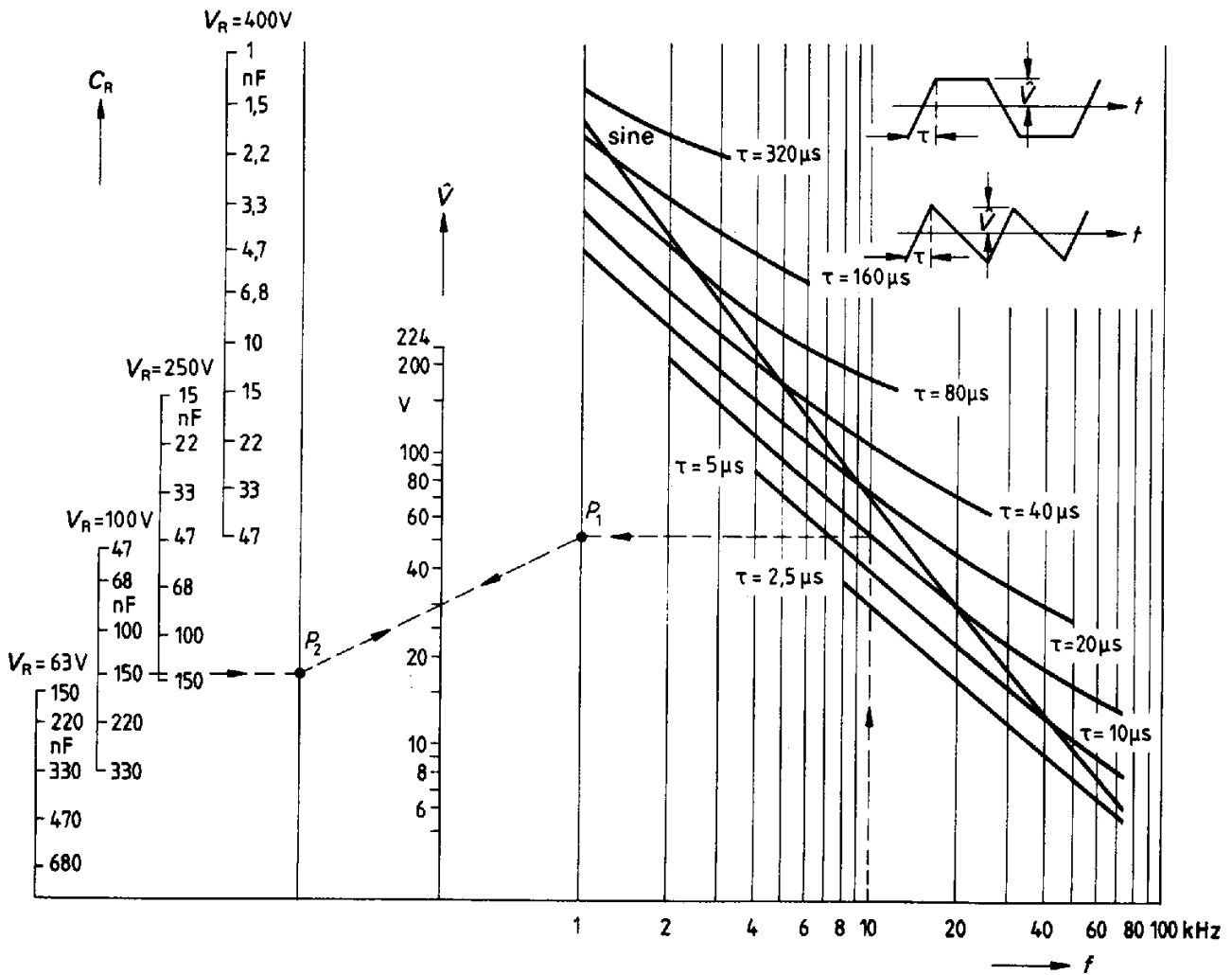
... B 32529

**B 32520, LS 7.5 mm**

Nomogram to determine the permissible peak voltage  $\hat{V}$

Determine the intersections  $P_1$  and  $P_2$  according to the plotted example. The intersection of the line connecting  $P_1$  with  $P_2$  and the  $\hat{V}$  scale gives the maximum permissible peak voltage.

In case of a trapezoidal voltage load with two steep edges, the second harmonic frequency must be considered. With sinusoidal voltage load, the "sine" characteristic applies.



**Example:**

- |                     |                        |   |                    |
|---------------------|------------------------|---|--------------------|
| $f = 10$ kHz        | (repetition frequency) | } | intersection $P_1$ |
| $\tau = 10$ $\mu$ s | (rise time)            |   |                    |
| $C_R = 150$ nF      | (capacitance)          | } | intersection $P_2$ |
| $V_R = 100$ V       | (rated voltage)        |   |                    |

According to the dashed line in the above graph, this results in a max. peak voltage  $\hat{V}$  of approx. 30 V.



**MKT Capacitors**

A-05-17-05

**B 32520**

SIEMENS AKTIENGESELLSCHAFT 47E D D

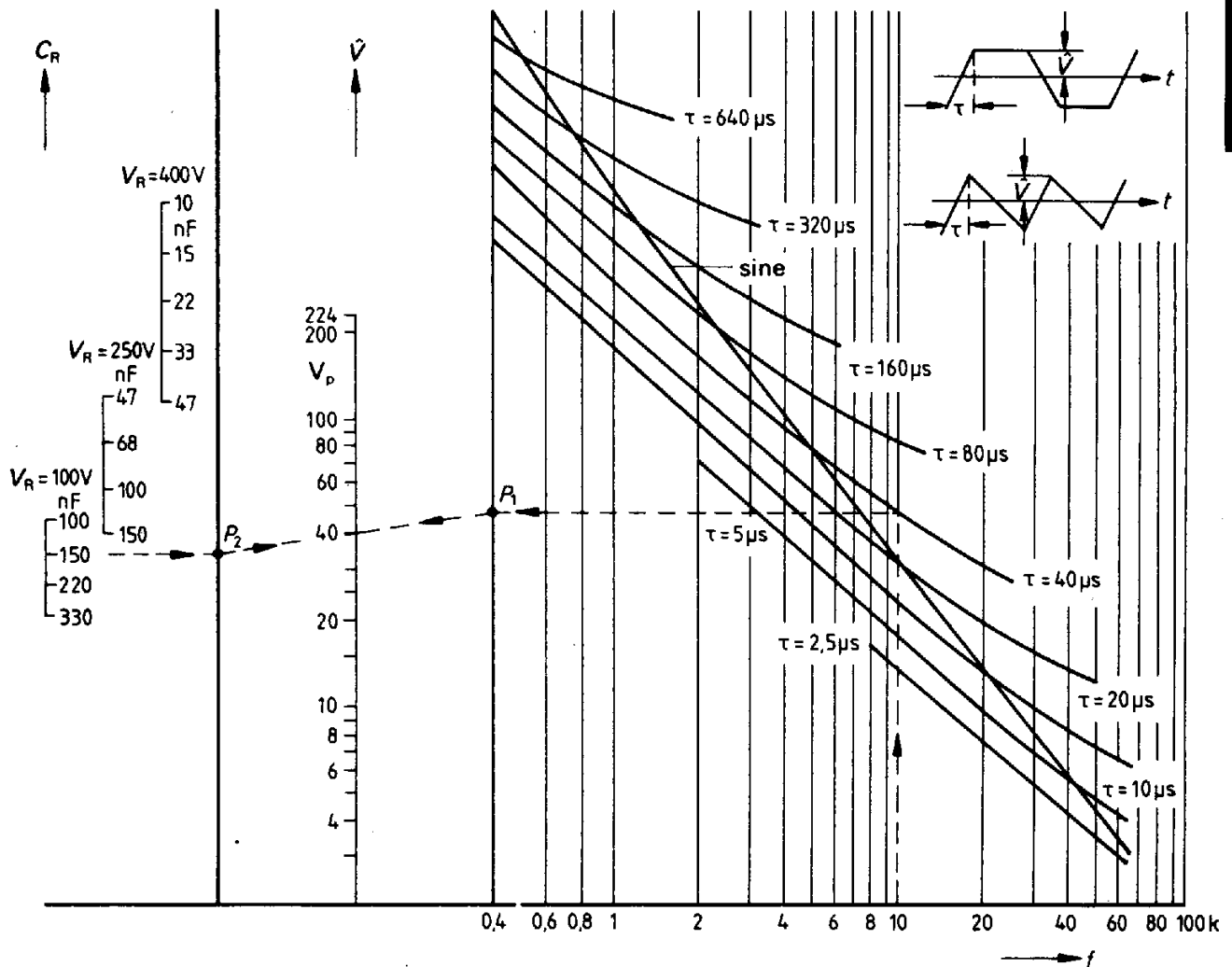
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**B 32521, LS 10 mm**

Nomogram to determine the permissible peak voltage  $\hat{V}$

Determine the intersections  $P_1$  and  $P_2$  according to the plotted example. The intersection of the line connecting  $P_1$  with  $P_2$  and the  $\hat{V}$  scale gives the maximum permissible peak voltage.

In case of a trapezoidal voltage load with two step edges, the second harmonic frequency must be considered. With sinusoidal voltage load, the "sine" characteristic applies.



**Example:**

- |                     |                        |   |                    |
|---------------------|------------------------|---|--------------------|
| $f = 10$ kHz        | (repetition frequency) | } | intersection $P_1$ |
| $\tau = 40$ $\mu$ s | (rise time)            |   |                    |
| $C_R = 150$ nF      | (capacitance)          | } | intersection $P_2$ |
| $V_R = 100$ V       | (rated voltage)        |   |                    |

According to the dashed line in the above graph, this results in a max. peak voltage  $\hat{V}$  of approx. 40 V.

A-05-17-05

B 32520

SIEMENS AKTIENGESELLSCHAFT 47E D

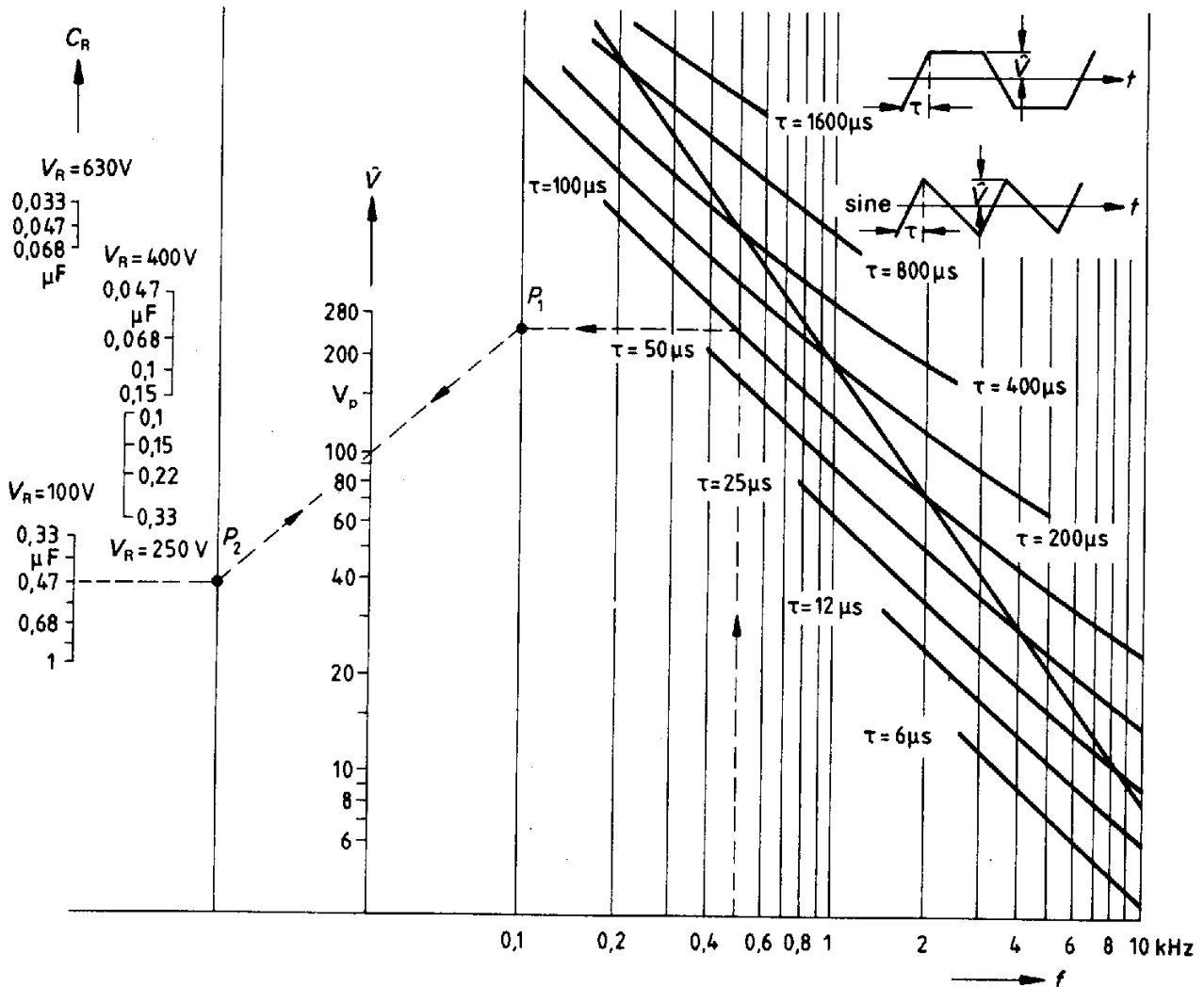
... B 32529

**B 32522, LS 15 mm**

Nomogram to determine the permissible peak voltage  $\hat{V}$

Determine the intersections  $P_1$  and  $P_2$  according to the plotted example. The intersection of the line connecting  $P_1$  with  $P_2$  and the  $\hat{V}$  scale gives the maximum permissible peak voltage.

In case of a trapezoidal voltage load with two steep edges, the second harmonic frequency must be considered. With sinusoidal voltage load, the "sine" characteristic applies.



**Example:**

- $f = 0.5 \text{ kHz}$  (repetition frequency)
  - $\tau = 100 \mu\text{s}$  (rise time)
  - $C_R = 0.47 \mu\text{F}$  (capacitance)
  - $V_R = 100 \text{ V}$  (rated voltage)
- } intersection  $P_1$
- } intersection  $P_2$

According to the dashed line in the above graph, this results in a max. peak voltage  $\hat{V}$  of approx. 100 V.

For loads at frequencies  $> 10 \text{ kHz}$ , please contact us.

**MKT Capacitors**

A-05-17-05

B 32520

...B 32529

SIEMENS AKTIENGESELLSCHAFT 47E D

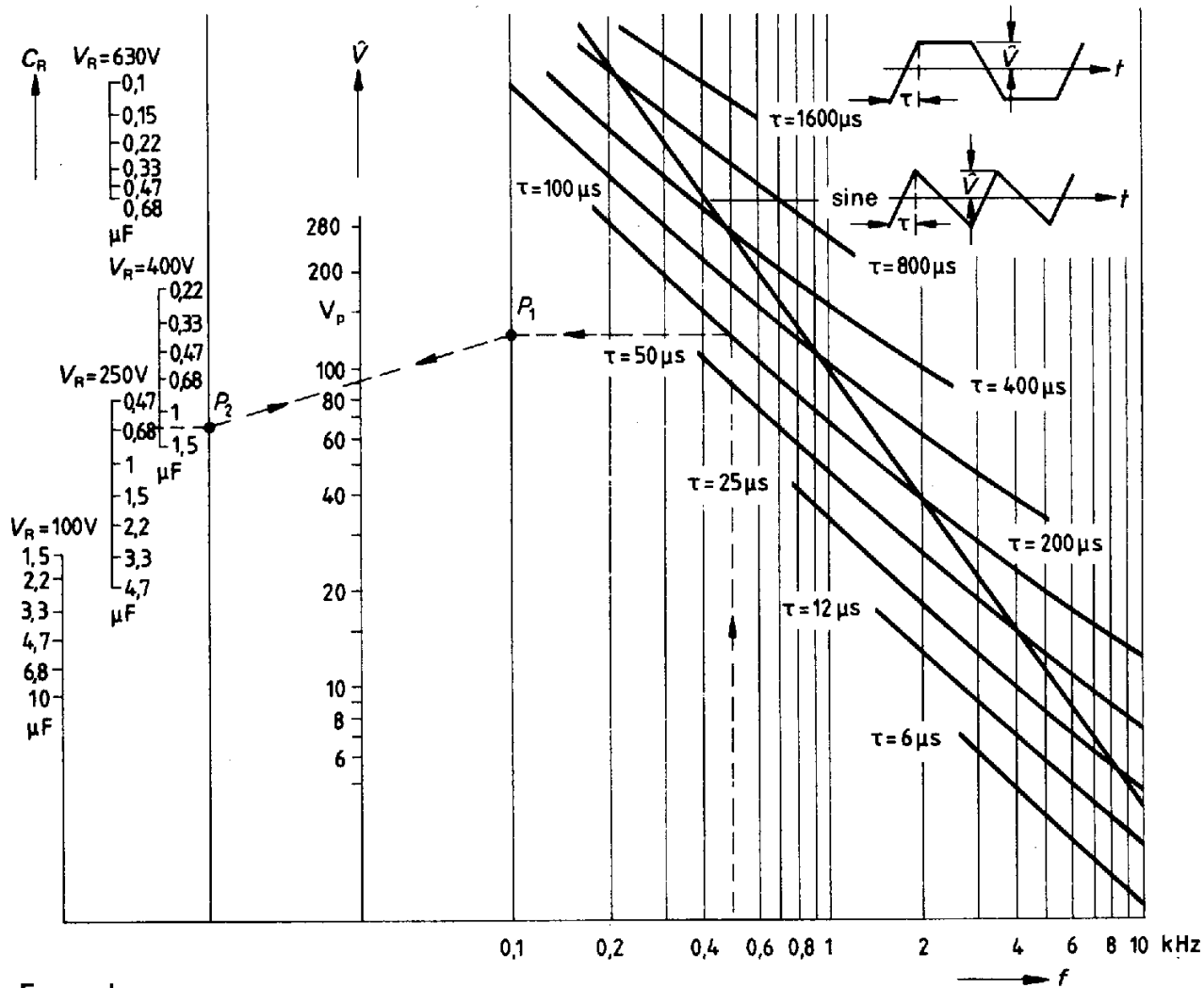
**B 32523, LS 22.5 mm**

**B 32524, LS 27.5 mm**

**Nomogram to determine the permissible peak voltage  $\hat{V}$**

Determine the intersections  $P_1$  and  $P_2$  according to the plotted example. The intersection of the line connecting  $P_1$  with  $P_2$  and the  $\hat{V}$  scale gives the maximum permissible peak voltage.

In case of a trapezoidal voltage load with two steep edges, the second harmonic frequency must be considered. With sinusoidal voltage load, the "sine" characteristic applies.



**Example:**

- $f = 0.5$  kHz (repetition frequency)
  - $\tau = 100 \mu s$  (rise time)
  - $C_R = 0.68 \mu F$  (capacitance)
  - $V_R = 250$  V (rated voltage)
- } intersection  $P_1$
- } intersection  $P_2$

According to the dashed line in the above graph, this results in a max. peak voltage  $\hat{V}$  of approx. 90 V.

For loads at frequencies  $> 10$  kHz, please contact us.