Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver

Datasheet

The LXT908 Universal 10BASE-T and AUI Transceiver (call hereafter LXT908 Transceiver) is designed for IEEE 802.3 physical layer applications. It provides all the active circuitry to interface most standard 802.3 controllers to either the 10BASE-T media or Attachment Unit Interface (AUI). In addition to standard 10 Mbps Ethernet, the LXT908 Transceiver also supports full-duplex operation at 20 Mbps.

LXT908 Transceiver functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link testing and reversed polarity detection/correction. The LXT908 Transceiver can be used to drive either the AUI drop cable or the 10BASE-T twisted-pair cable with only a simple isolation transformer. Integrated filters simplify the design work required for FCC-compliant EMI performance.

The LXT908 Transceiver is fabricated with an advanced CMOS process and requires only a single 3.3V power supply.

Applications

- Access devices (DSL, Cable Modems, and Set-top Boxes)
- Routers/Bridges/Switches/Hubs
- Telecom Backplane
- USB to Ethernet Converters

Product Features

Functional Features

- Improved Filters - Simplifies FCC Compliance
- Integrated Manchester Encoder/Decoder
- 10BASE-T compliant Transceiver
- AUI Transceiver
- Supports Standard and Full-Duplex Ethernet

Diagnostic Features

- Four LED Drivers
- AUI/RJ-45 Loopback

Convenience Features

- Automatic/Manual AUI/RJ-45 Selection
- Automatic Polarity Correction
- SQE Disable/Enable function
- Power Down Mode with tri-stated outputs
- Four loopback modes
- Single 3.3V operation
- Available in 64-pin LQFP and 44-pin PLCC package
- Commercial (0 to +70°C) and Extended (-40 to +85°C) temperature range

Order Number: 249049-003
29-Oct-2005

The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at http://www.intel.com.

Contents

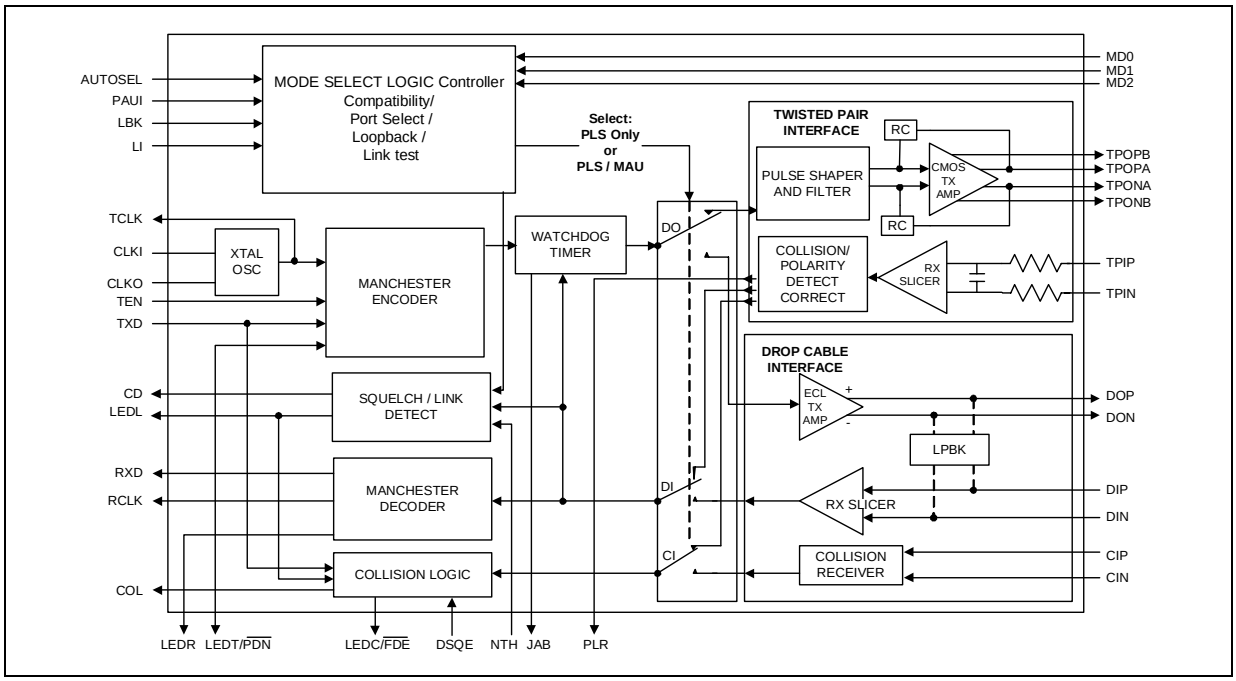
Figures

Tables

Revision History

Date	Revision	Page	Description
29-Oct-2005	003	43	Added Section 5.1, “Top-Label Marking”: Table 48 “Sample LQFP Package - Intel® LXT908 Transceiver” and Table 49 “Sample Pb-Free (RoHS-Compliant) LQFP Package - Intel® LXT908 Transceiver” under
		45	Modified Table 14 “Product Information” for RoHS information.
		46	Modified Figure 52 “Ordering Information - Sample” .
June 2001	2001	1	Added new set of applications
		19	Added 01. µF label to capacitor at bottom of Figure 9
		20	Added 01. µF label to capacitor at bottom of Figure 10
		21	Added 01. µF label to capacitor at bottom of Figure 11
		22	Added 01. µF label to capacitor at bottom of Figure 12
		23	Added 01. µF label to capacitor at bottom of Figure 13
		26	Added second para. under “Test Specifications” regarding Quality and Reliability issues
		26	Removed “Ambient operating temperature” from Absolute Maximum Ratings table.
		43	Added Appendix: Product Ordering Information

Figure 1. Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2. Pin Assignments

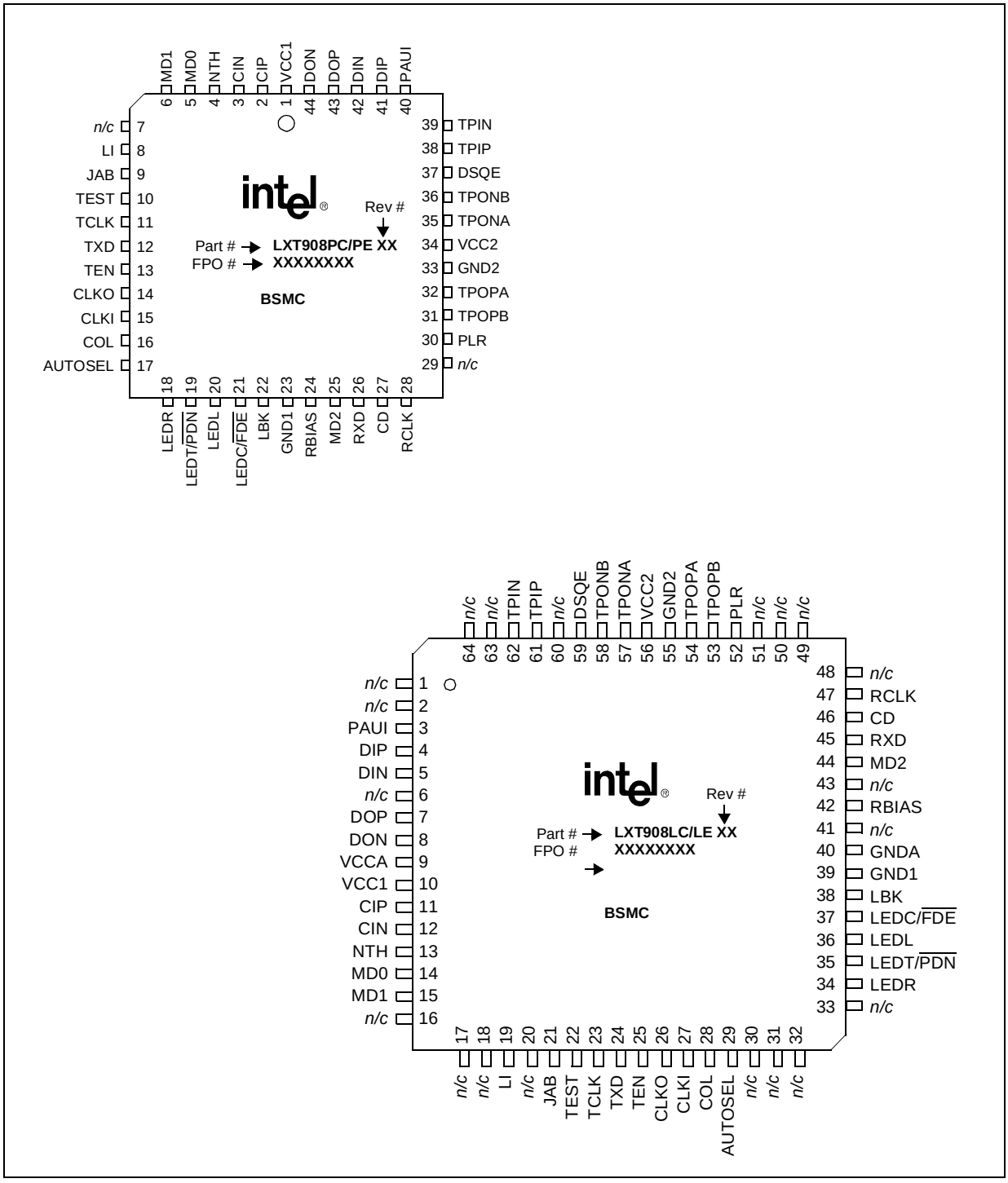


Table 1. Signal Descriptions (Sheet 1 of 3)

Pin#		Symbol	I/O	Description
PLCC	LQFP			
1 34	10 56	VCC1 VCC2	– –	**Power 1 and 2.** Connect to positive power supply terminal (+3.3V DC).
–	9	VCCA	–	**Analog Supply.** (+3.3V)
2 3	11 12	CIP CIN	I I	**AUI Collision Pair.** Differential input pair connected to the AUI transceiver CI circuit. The input is collision signaling or SQE.
4	13	NTH	I	**Normal Threshold.** When NTH is High, the normal TP squelch threshold is in effect. When NTH is Low, the normal TP squelch threshold is reduced by 4.5 dB.
5 6 25	14 15 44	MD0 MD1 MD2	I I I	**Mode Select 0 (MD0), Mode Select 1 (MD1) and Mode Select 2 (MD2).** Mode select pins determine the controller compatibility mode as specified in Table 2 on page 13.
7, 29	1, 2, 6, 16, 17, 18, 20, 30, 31, 32, 33, 41, 43, 48, 49, 50, 51, 60, 63, 64	N/C	–	**No Connect.** These pins may be left unconnected or tied to ground.
8	19	LI	I	**Link Test Enable.** Controls Link Integrity Test; enabled when High, disabled when Low.
9	21	JAB	O	**Jabber Indicator.** Output goes High to indicate Jabber state.
10	22	TEST	I	**Test.** This pin must be tied High.
11	23	TCLK	O	**Transmit Clock.** A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller. TCLK goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
12	24	TXD	I	**Transmit Data.** Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.
13	25	TEN	I	**Transmit Enable.** Enables data transmission and starts the Watch-Dog Timer. Synchronous to TCLK (see Test Specifications for details).
14 15	26 27	CLKO CLKI	O I	**Crystal Oscillator.** A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI, with CLKO left open.
16	28	COL	O	**Collision Detect.** Output driving the collision detect input of the controller. COL goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
17	29	AUTOSEL	I	**Automatic Port Select.** When High, automatic port selection is enabled (the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver defaults to the AUI port only if TP link integrity = Fail). When Low, manual port selection is enabled (the PAUI pin determines the active port).
18	34	LEDR	O	**Receive LED.** Open drain driver for the receive indicator LED. Output is pulled Low during receive, except when data is being looped back to DIN/DIP from a remote transceiver (external MAU). LED “On” time (Low output) is extended by approximately 100 ms.

Table 1. Signal Descriptions (Sheet 2 of 3)

Pin#		Symbol	I/O	Description
PLCC	LQFP			
19	35	LEDT/ $\overline{\text{PDN}}$	O I	**Transmit LED (LEDT)/Power Down ($\overline{\text{PDN}}$).** Open drain driver for the transmit indicator LED. Output is pulled Low during transmit. **Do not allow this pin to float. If unused, tie High.** LED “On” time (Low output) is extended by approximately 100 ms. If externally tied Low, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver goes to power-down state. In power-down state, TCLK, COL, RXD, CD, and RCLK (pins 11, 16, 26, 27, and 28, respectively) are tri-stated.
20	36	LEDL	O I	**Link LED.** Open drain driver for link integrity indicator LED. Output is pulled Low during link test pass. If externally tied Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver Low, internal circuitry is forced to “Link Pass” state and the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver will continue to transmit link test pulses.
21	37	LEDC/ $\overline{\text{FDE}}$	O I	**Collision LED (LEDC)/Full Duplex Enable ($\overline{\text{FDE}}$).** Open drain driver for the collision indicator LED pulls Low during collision. LED “On” time (Low output) is extended by approximately 100 ms. If externally tied Low, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver disables the internal TP loopback and collision detection circuits to allow full-duplex operation or external twisted-pair loopback.
22	38	LBK	I	**Loopback.** Enables internal loopback mode. Refer to Functional Description and Test Specifications for details.
23 33	39 55	GND1 GND2	– –	**Ground Returns 1 and 2.** Connect to negative power supply terminal (ground).
–	40	GNDA	–	Analog Ground. Ground for analog plane.
24	42	RBIAS	I	**Bias Control.** A 12.4 kΩ 1% resistor to ground at this pin controls operating circuit bias.
26	45	RXD	O	**Receive Data.** Output signal connected directly to the receive data input of the controller. RXD goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
27	46	CD	O	**Carrier Detect.** An output to notify the controller of activity on the network. CD goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
28	47	RCLK	O	**Receive Clock.** A recovered 10 MHz clock that is synchronous to the received data and connected to the controller receive clock input. RCLK goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
30	52	PLR	O	**Polarity Reverse.** Output goes High to indicate reversed polarity at the TP input.
32 35 31 36	54 57 53 58	TPOPA TPONA TPOPB TPONB	O O O O	**Twisted-Pair Transmit Pairs A & B.** Two differential driver pair outputs (A and B) to the twisted-pair cable. The outputs are pre-equalized. Each pair must be shorted together with an 11.5 Ω 1% resistor to match an impedance of 100Ω.
37	59	DSQE	I	**Disable SQE.** When DSQE is High, the SQE function is disabled. When DSQE is Low, the SQE function is enabled. SQE must be disabled for normal operation in Hub/Switch applications.
3839	61 62	TPIP TPIN	I I	**Twisted-Pair Receive Pair.** A differential input pair from the TP cable. Receive filter is integrated on chip. No external filters are required.

Table 1. Signal Descriptions (Sheet 3 of 3)

Pin#		Symbol	I/O	Description
PLCC	LQFP			
40	3	PAUI	I	**Port/AUI Select.** In Manual Port Select mode (AUTOSEL Low), PAUI selects the active port. When PAUI is High, the AUI port is selected. When PAUI is Low, the TP port is selected. In Auto Port Select mode, PAUI must be tied to ground.
41 42	4 5	DIP DIN	I I	**AUI Receive Pair.** Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
43 44	7 8	DOP DON	O O	**AUI Transmit Pair.** A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.

2.0 Functional Description

2.1 Introduction

The LXT908 Universal 10BASE-T and AUI Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as an AUI (PLS-Only device) for use with 10BASE-2 or 10BASE-5 coaxial cable networks, or as an Integrated PLS/MAU for use with 10BASE-T twisted-pair (TP) networks. In addition to standard 10 Mbps operation, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver also supports full-duplex 20 Mbps operation.

The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver interfaces a back-end controller to either an AUI drop cable or a twisted-pair cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data Output (DO), Data Input (DI), and Collision (CI). The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the three basic interfaces, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver Transmit function refers to data transmitted by the back end to the AUI cable (PLS-Only mode) or to the twisted-pair network (Integrated PLS/MAU mode). The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver Receive function refers to data received by the back end from the AUI cable (PLS-Only) or from the twisted-pair network (Integrated PLS/MAU mode). In the integrated PLS/MAU mode, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver performs all required MAU functions defined by the IEEE 802.3 10BASE–T specification, such as collision detection, link integrity testing, signal quality error messaging, jabber control, and loopback. In the PLS-Only mode, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver receives incoming signals from the AUI DI circuit with
±18 ns of jitter and drives the AUI DO circuit.

2.1.1 Controller Compatibility Modes

The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver is compatible with most industry-standard controllers including devices produced by Advanced Micro Devices (AMD), Motorola, Intel, Fujitsu, National Semiconductor, Seeq, and Texas Instruments, as well as custom controllers. Five different control signal timing and polarity schemes (Modes 1 through 5) are required to achieve this compatibility. Mode select pins (MD2:0) determine Controller compatibility modes as listed in Table 2 on page 13. Refer to Test Specifications for a complete set of timing diagrams for each mode.

2.1.2 Transmit Function

The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver receives NRZ data from the controller at the TXD input as shown in Figure 1, “Block Diagram” on page 7, and passes it through a Manchester encoder. The encoded data is then transferred to either the AUI cable (the DO circuit) or the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in Figure 3. The TPO

output is pre-distorted and pre-filtered to meet the 10BASE-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC-compliant EMI performance. During idle periods, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver transmits link integrity test pulses on the TPO circuit (if LI is enabled and integrated PLS/ MAU mode is selected). External resistors control the termination impedance.

Figure 3. TPO Output Waveform

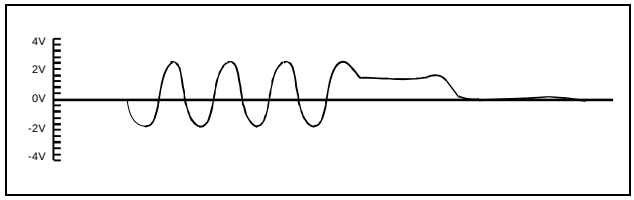


Table 2. Controller Compatibility Mode Options

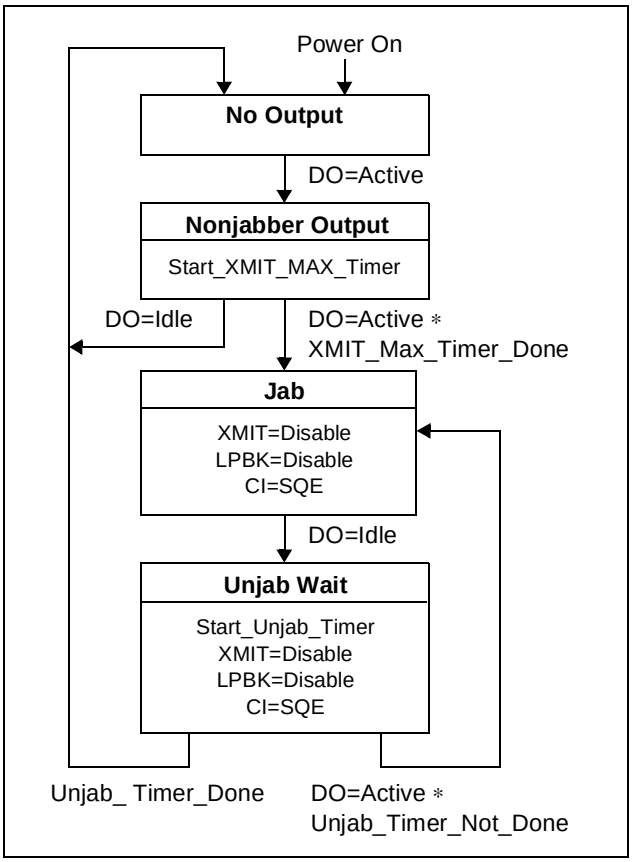
Controller Mode	MD2	MD1	MD0
Mode 1 - For AMD AM7990, Motorola 68EN360, MPC860 or compatible controllers	Low	Low	Low
Mode 2 - For Intel 82596 or compatible controllers	Low	Low	High
Mode 3 - For Fujitsu MB86950, MB86960 or compatible controllers (Seeq 8005)[1]	Low	High	Low
Mode 4 - For National Semiconductor 8390 or compatible controllers (TI TMS380C26)	Low	High	High
Mode 5 - For custom controllers (Mode 3 with TCLK, RCLK and COL inverted)	High	High	Low

1. SEEQ controllers require inverters on CLKI, LBK, RCLK, and COL in Mode 3; or on CLKI, LBK, and TCLK in Mode 5.

2.1.3 Jabber Control Function

Figure 4 on page 14 is a state diagram of the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver Jabber control function. The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver on-chip Watch-Dog Timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the Watch-Dog Timer disables the transmit and loopback functions, and activates the JAB pin. Once the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

Figure 4. Jabber Control Function



2.1.4 Receive Function

The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver receive function acquires timing and data from the twisted-pair network (TPI circuit) or from the AUI (DI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder then output as decoded NRZ data and recovered clock on the RXD and RCLK pins, respectively.

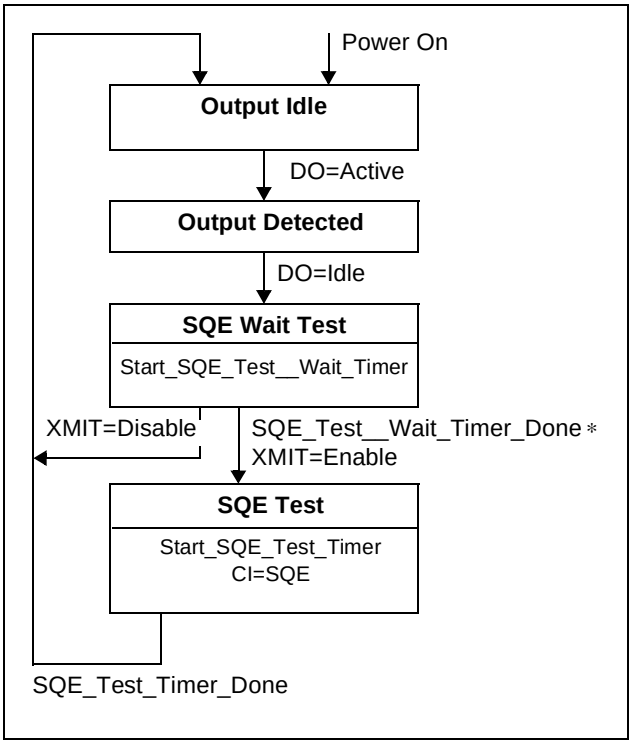
An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75 percent of the threshold level (unsquelched) for 8 bit times (typical), the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver receive function enters the idle state. If the polarity of the TPI circuit is reversed, Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver detects the polarity reverse and reports it via the PLR output. The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver automatically corrects reversed polarity.

2.1.5 SQE Function

In the integrated PLS/MAU mode, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver supports the signal quality error (SQE) function as shown in Figure 5 on page 15, although the SQE function can be disabled. After every successful transmission on the 10BASE-T

network when SQE is enabled, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver transmits the SQE signal for 10BT ± 5BT over the internal CI circuit, which is indicated on the COL pin of the device. SQE must be disabled for normal operation in hub and switch applications. In twisted-pair applications, the SQE function is disabled when DSQE is set High, and enabled when DSQE is Low. When using the 10BASE-2 port of the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver, the SQE function is determined by the external MAU attached.

Figure 5. SQE Function



2.1.6 Polarity Reverse Function

The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever a correct polarity frame or a correct link pulse is received, these two counters are reset to zero. If the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. If Link Integrity Testing is disabled, polarity detection is based only on received data. Polarity correction is always enabled.

2.1.7 Loopback Function

The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver provides the normal loopback function specified by the 10BASE-T standard for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the

Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. This “normal” loopback function is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Normal loopback is also disabled during link fail and jabber states.

The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver also provides three additional loopback functions. An external loopback mode, useful for system-level testing, is controlled by pin 21 (LEDC). When LEDC is tied Low, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver disables the collision detection and internal loopback circuits, to allow external loopback or full-duplex operation.

“Normal” twisted-pair loopback is controlled by pin 22 (LBK). When the twisted-pair port is selected and LBK is High, twisted-pair loopback is “forced”, overriding collisions on the twisted-pair circuit. When LBK is Low, normal loopback is in effect.

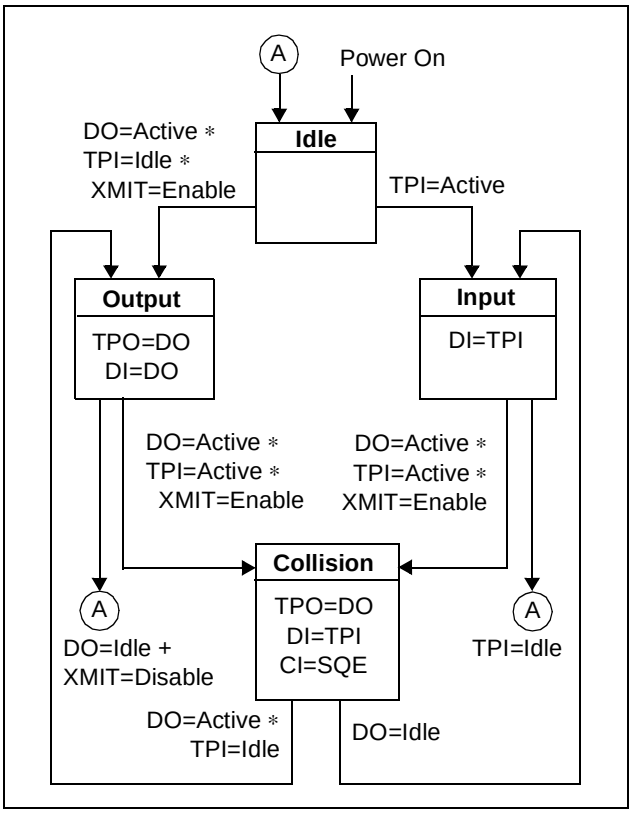
AUI loopback is also controlled by the LBK pin. When the AUI port is selected and LBK is High, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK is Low, no AUI loopback occurs.

2.1.8 Collision Detection Function

The collision detection function operates on the twisted-pair side of the interface. For standard (half-duplex) 10BASE-T operation, a collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 6 is a state diagram of the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver collision detection function. Refer to Test Specifications for collision detection and COL/CI output timing.

Note: For full-duplex operation, the collision detection circuitry must be disabled.

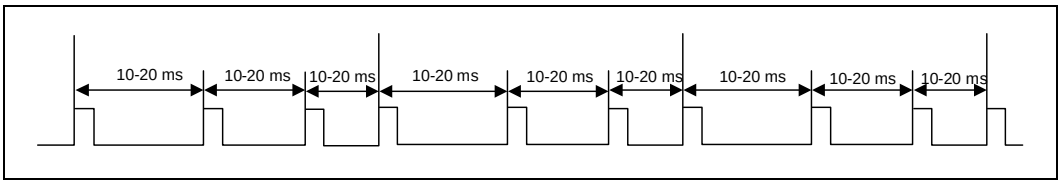
Figure 6. Collision Detection Function



2.1.9 Link Pulse Transmission

The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver transmits standard link pulses which meet the 10BASE-T specifications. Figure 7 shows the link integrity pulse timing.

Figure 7. Transmitted Link Integrity Pulse Timing

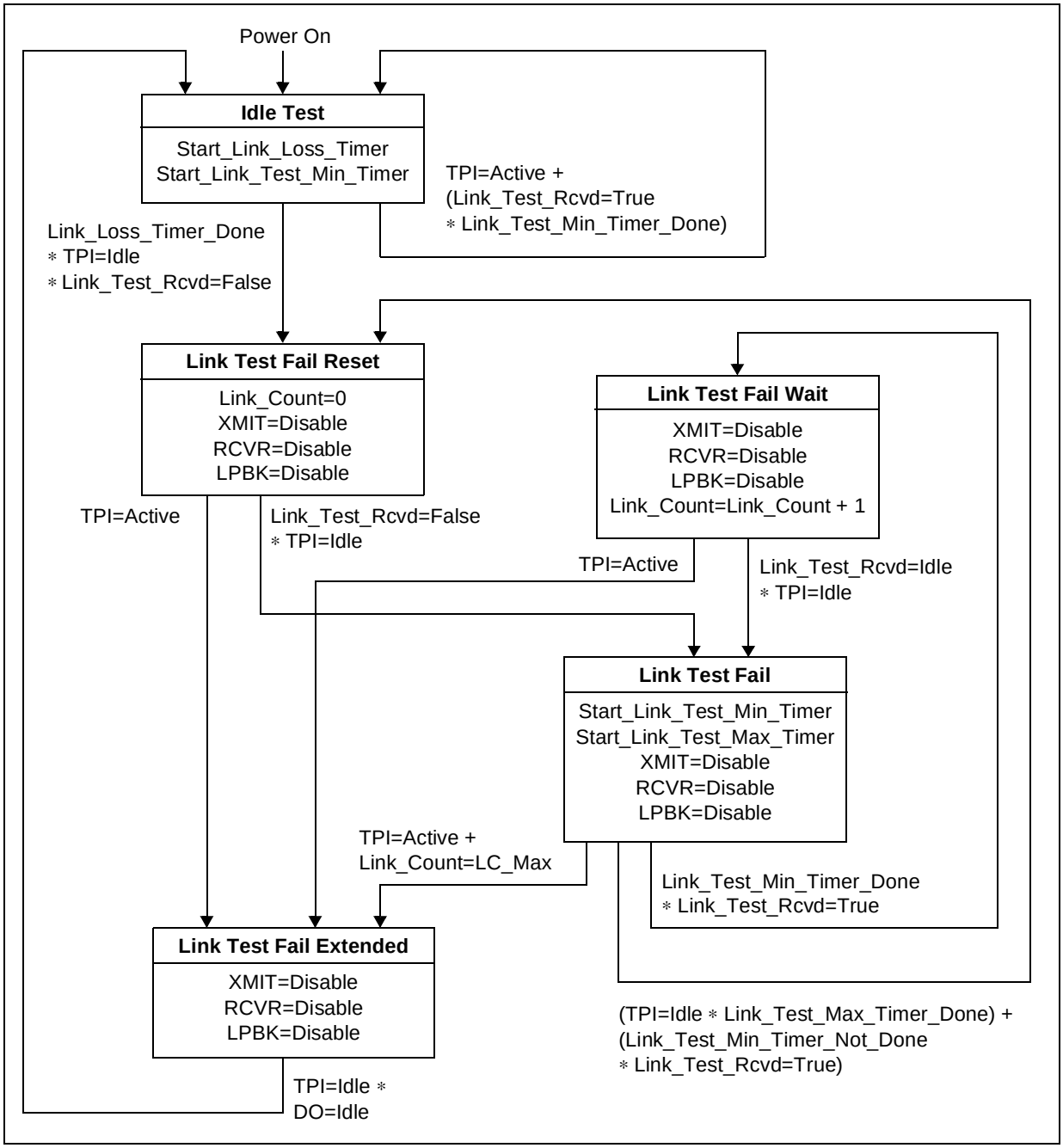


2.1.10 Link Integrity Test Function

Figure 8 on page 18 is a state diagram of the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when pin 8 (LI) is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic.

If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver ignores any link integrity pulse with interval less than 2 - 7 ms. The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

Figure 8. Link Integrity Test Function



3.0 Application Information

Figure 9 on page 20 through Figure 15 on page 26 show typical Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver applications.

3.1 External Components

3.1.1 Crystal Information

Suitable crystals are available from various manufacturers. Table 3 lists suitable crystals based on a limited evaluation. Designers should test and validate all crystals before using them in production.

Table 3. Suitable Crystals

Manufacturer	Part Number
MTRON	MP-1
	MP-2

3.1.2 Magnetic Information

The twisted-pair interface requires a 1:1 ratio for the receive transformer, and a 1:2 ratio for the transmit transformer. The AUI interface requires a 1:1 ratio for data-in, data-out, and collision-pair transformers. A cross-reference list of suitable magnetics and part numbers is available in Application Note 73, Magnetic Manufacturers (248991-001), that can be found on the Intel website (www.intel.com). Designers should test and validate all magnetics before committing to a specific component.

3.2 Layout Requirements

3.2.1 Auto Port Select with External Loopback Control

Figure 9 on page 20 is a typical Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver application. The diagram groups similar pins together, but does not represent the actual Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver pin-out. The controller interface pins (TXD, RXD, TEN, TCLK, RCLK, CD, COL, and LBK) are shown at the top left of the diagram.

Programmable option pins are grouped at the center left of the diagram. The PAUI pin is tied Low and all other option pins are tied High. This setup selects the following options:

- Automatic Port Selection
  (PAUI Low and AUTOSEL High)
- Normal Receive Threshold (NTH High)
- Mode 4, compatible with National NS8390 controllers (MD2:0 = Low, High, High)
- SQE Disabled (DSQE High)
- Link Testing Enabled (LI High)

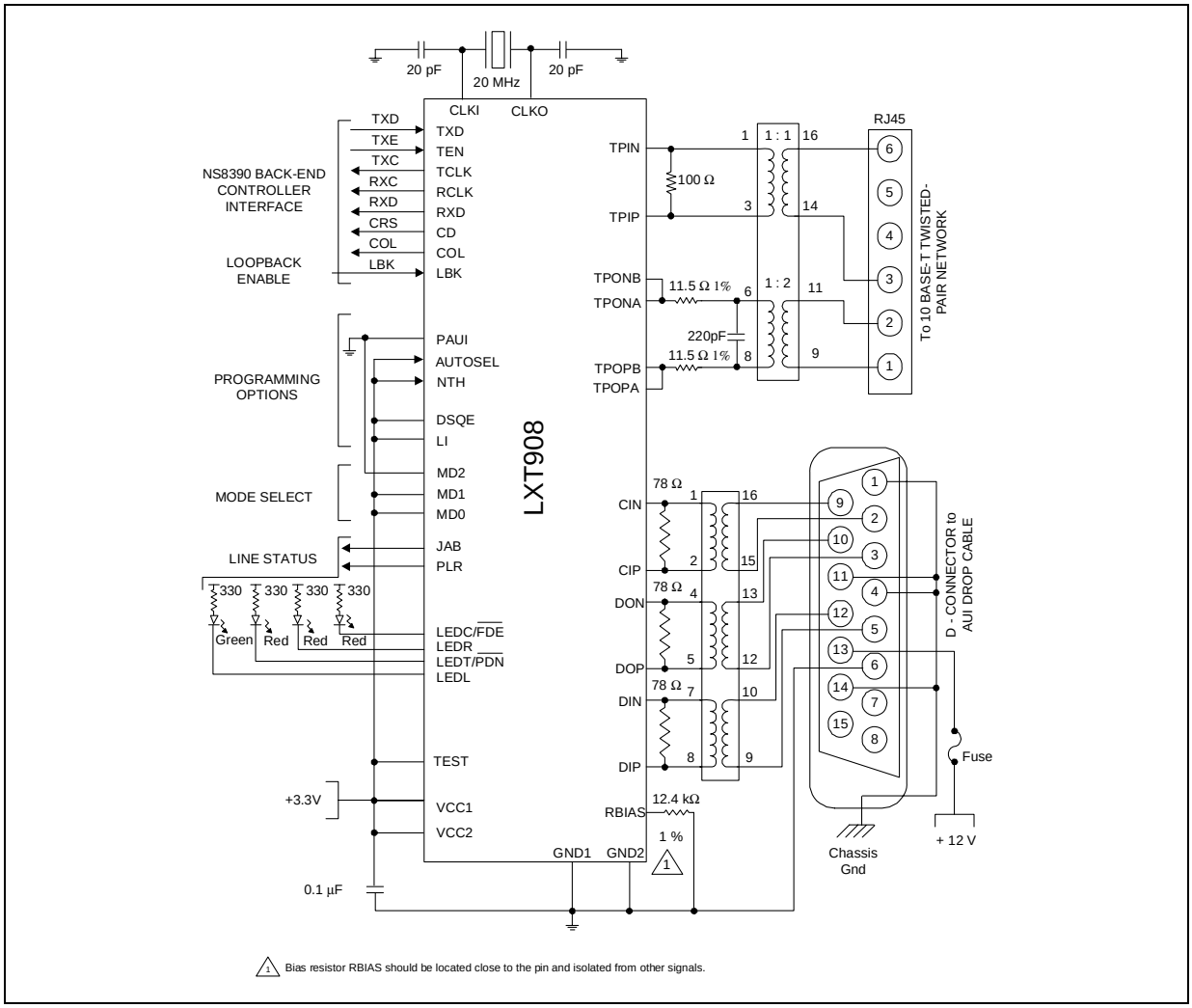
Status outputs are grouped at the lower left of the diagram. Line status outputs drive LED indicators and the Jabber and Polarity status indicators are available, as required.

Power and ground pins are shown at the bottom of the diagram. A single-power supply is used for both VCC1 and VCC2, with a decoupling capacitor installed between the power and ground busses.

An additional power and ground pin (VCCA and GNDA) is supported in designs using the 64-pin LQFP package. A single-power supply is used for all three power and ground pins (VCC1, VCC2, VCCA) and (GND1, GND2, GNDA). Please install a decoupling capacitor between each power and ground buss.

The twisted-pair and AUI interfaces are shown at the upper and lower right of the diagram, respectively. Impedance matching resistors for 100 UTP are installed in each I/O pair, but no external filters are required.

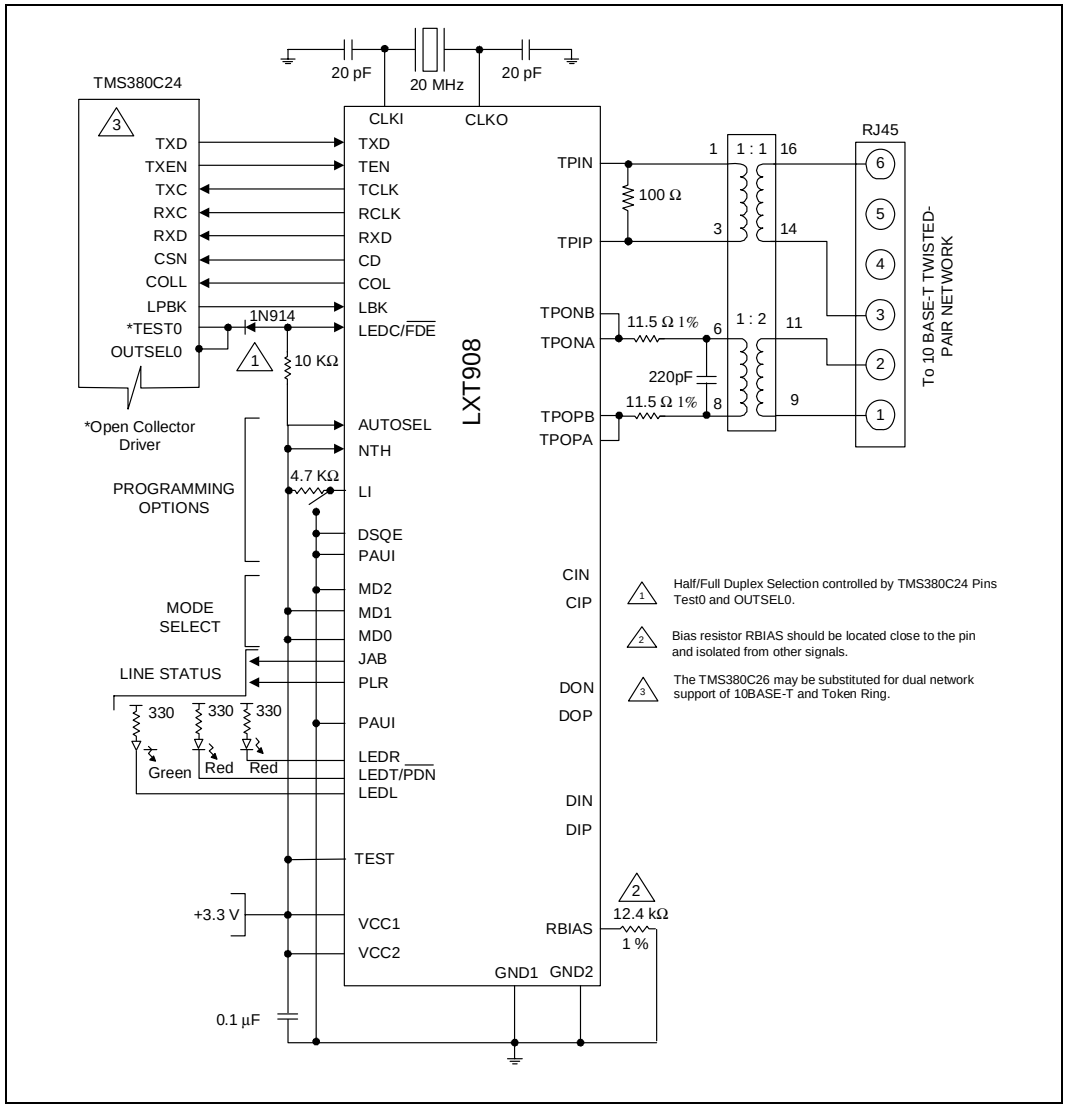
Figure 9. LAN Adapter Board - Auto Port Select with External Loopback Control



3.2.2 Full Duplex Support

Figure 10 shows the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver with a Texas Instruments 380C24 CommProcessor. The 380C24 is compatible with Mode 4 (MD2:0 = Low, High, High). When used with the 380C24 or other full- duplex-capable controllers, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver supports full-duplex Ethernet, effectively doubling the available bandwidth of the network. In this application, the SQE function is enabled (DSQE tied Low), and the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver AUI port is not used.

Figure 10. Full-Duplex Operation

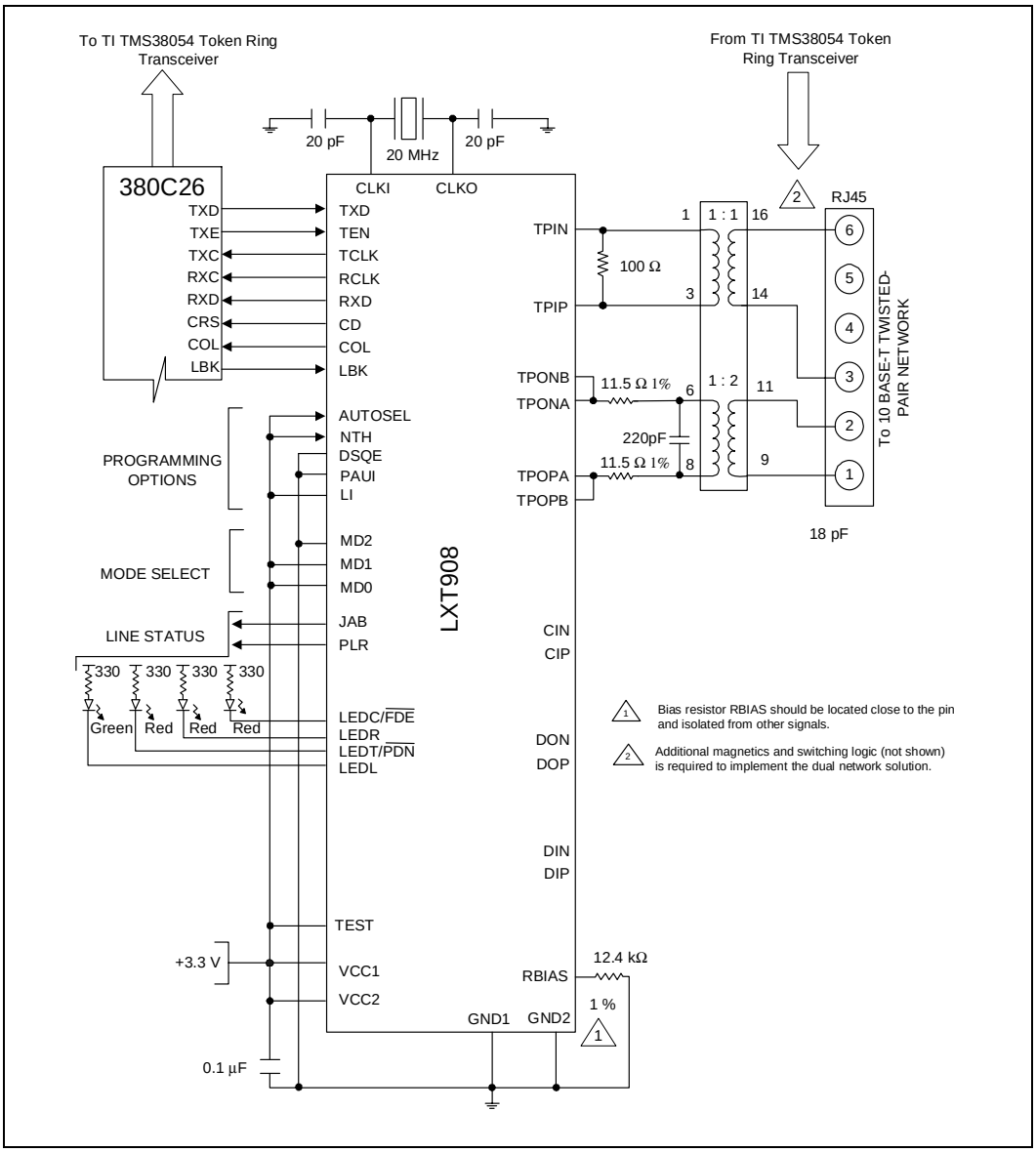


3.2.3 Dual Network Support-10Base T and Token Ring

Figure 11 shows the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver with a Texas Instruments 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD2:0 = Low, High, High).

When used with the 380C26, both the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver and a TMS38054 Token Ring transceiver can be tied to a single RJ-45, allowing dual network support from a single connector. The Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver AUI port is not used.

Figure 11. Intel® LXT908 Transceiver/380C26 Interface for Dual Network Support of 10BASE-T and Token Ring



3.2.4 Manual Port Select & Link Test Function

When MD2:0 = Low, High, Low, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver logic and framing are set to Mode 3 (compatible with Fujitsu MB86950 and MB86960, and Seeq 8005 controllers). Figure 12 shows the setup for Fujitsu controllers. Figure 13 on page 24 shows the four inverters required to interface with the Seeq 8005 controller. As in Figure 9 on page 20, both these Mode 3 applications show the LI pin tied High, enabling Link Testing; and the NTH and DSQE pins are both tied High, selecting the standard receiver threshold and disabling SQE. However, in these applications, AUTOSEL is tied Low, allowing external port selection through the PAUI pin.

Figure 12. LAN Adapter Board - Manual Port Select with Link Test Function

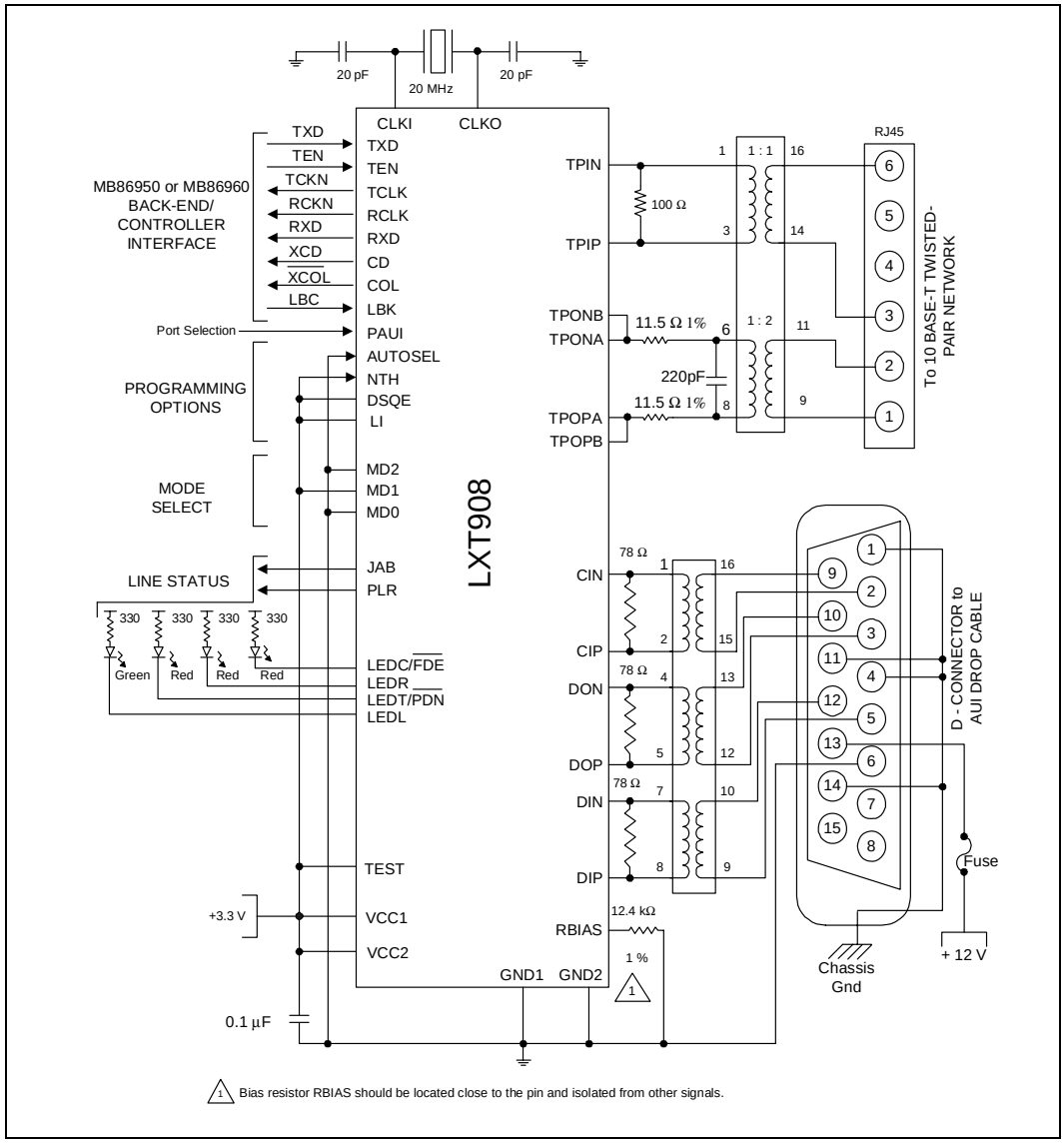
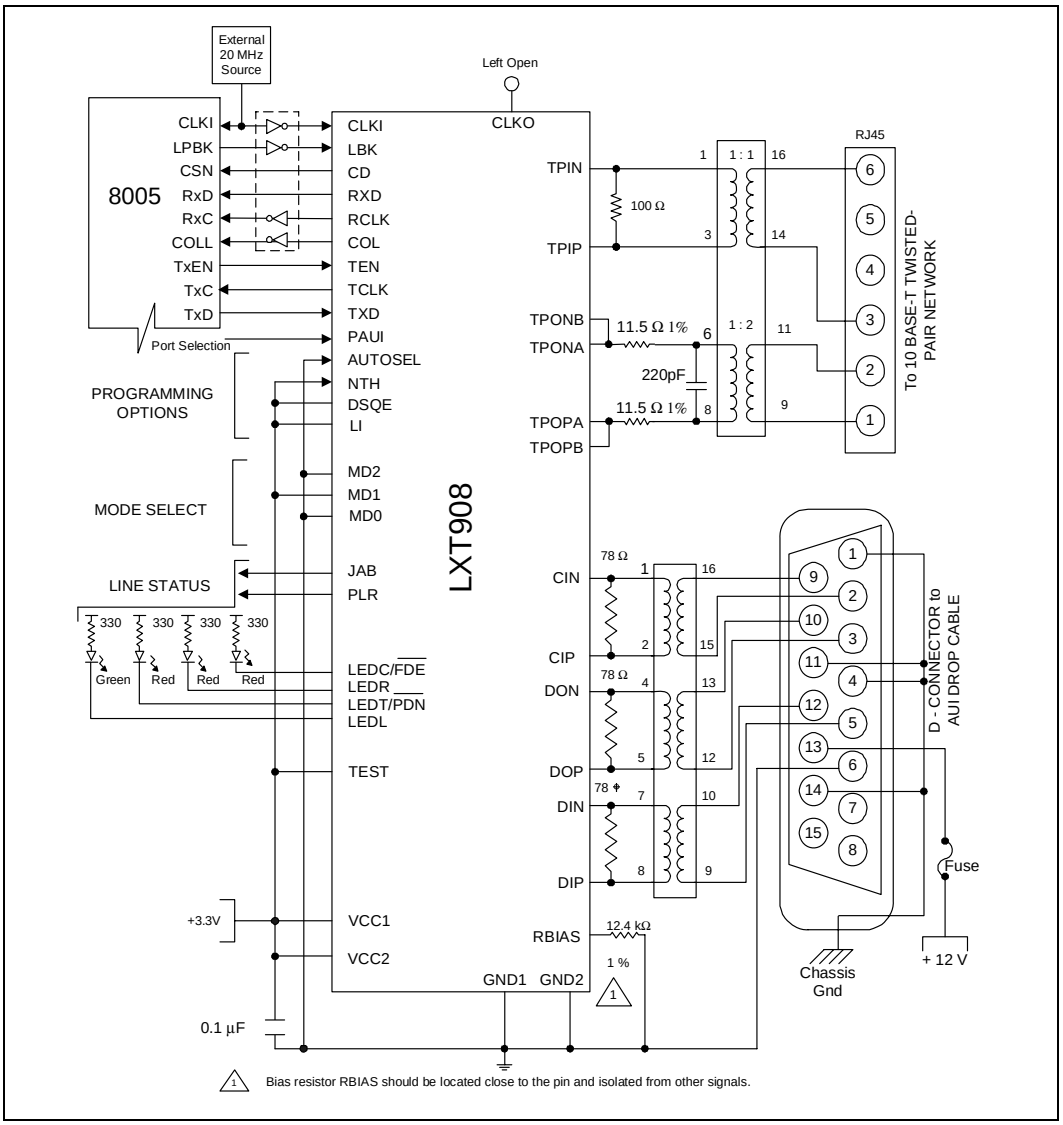


Figure 13. Manual Port Select with Seeq 8005 Controller

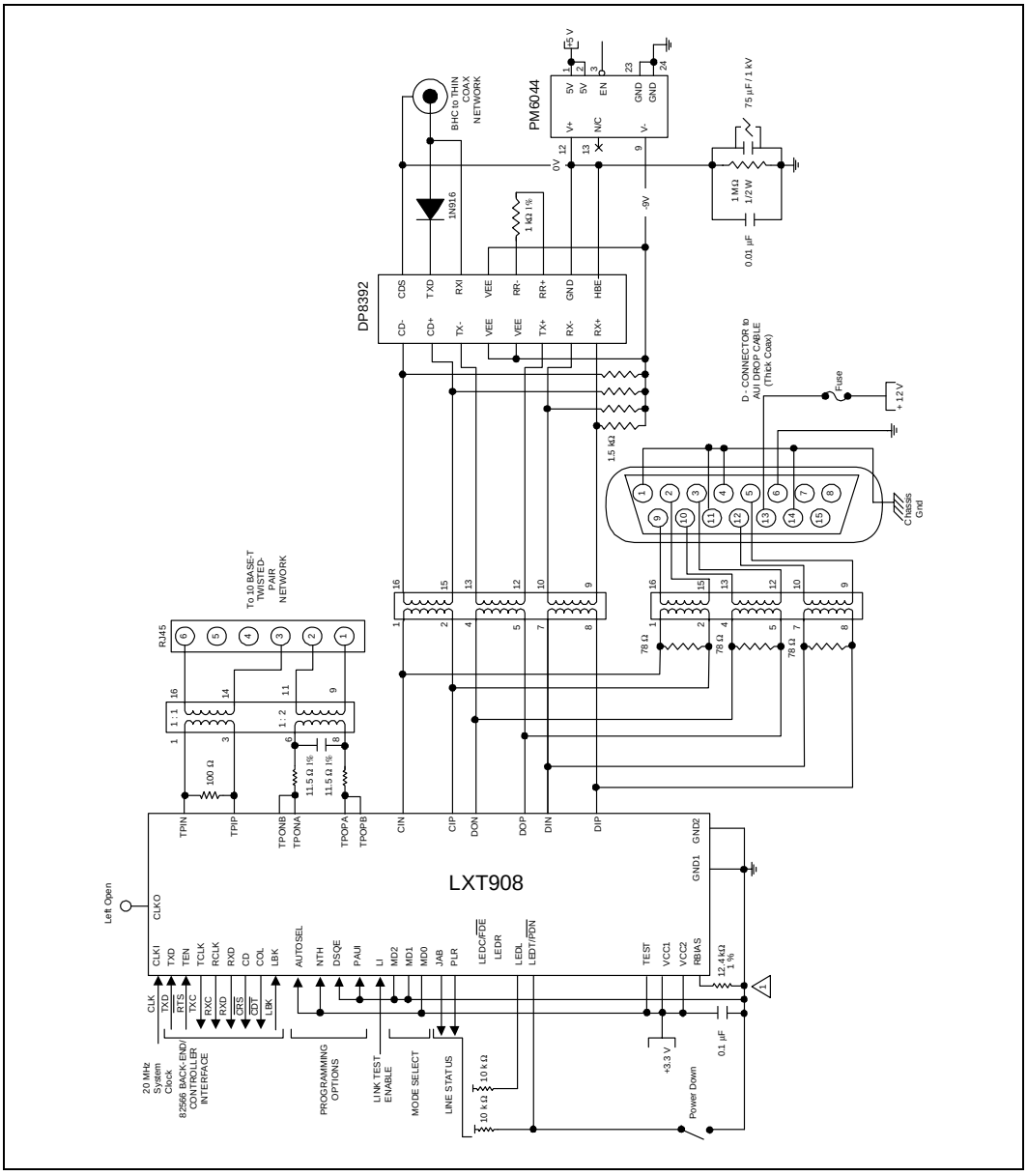


3.2.5 Three Media Application

Figure 14 shows the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver in Mode 2 (compatible with Intel 82596 controllers) with additional media options for the AUI port.

Two transformers are used to couple the AUI port to either a D-connector or a BNC connector. (A DP8392 coax transceiver with PM6044 power supply are required to drive the thin coax network through the BNC.

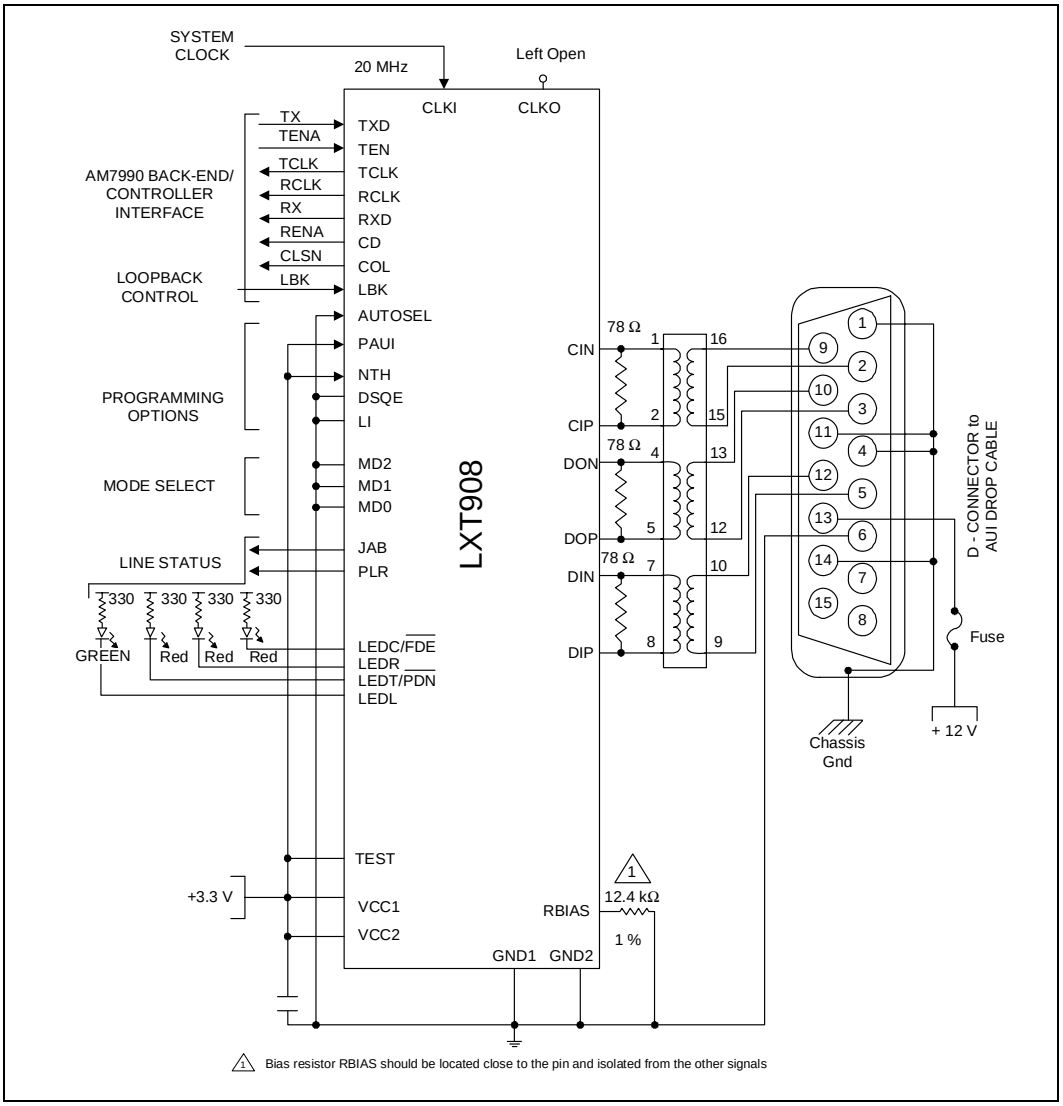
Figure 14. Three Media Application



3.2.6 AUI Encoder/Decoder Only

In the application shown in Figure 15, the DTE is connected to a coaxial network through the AUI. AUTOSEL is tied Low and PAUI is tied High, manually selecting the AUI port. The twisted-pair port is not used. With MD2:0 all tied Low, the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver logic and framing are set to Mode 1 (compatible with AMD and Motorola controllers). The LI pin is tied Low, disabling the link test function. The DSQE pin is also Low, enabling the SQE function. The LBK input controls loopback. A 20 MHz system clock is supplied at CLKI, with CLKO left open.

Figure 15. AUI Encoder/Decoder Only Application



4.0 Test Specifications

Note: Table 4 through Table 13 on page 30 and Figure 16 on page 31 through Figure 45 on page 40 represent the performance specifications of the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver. These specifications are guaranteed by test except where noted "by design." Minimum and maximum values listed in Table 6 through Table 13 on page 30 apply over the recommended operating conditions specified in Table 5.

For all Quality and Reliability issues (for example, parts packaging and thermal specifications), please send your questions to Intel at the following e-mail address: www.qr.requests@intel.com.

Table 4. Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{CC}	-0.3	6	V
Storage temperature	T_{STG}	-65	+150	ºC

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Recommended supply voltage[1]	V_{CC}	3.13	3.3	3.47	V
Recommended operating temperature (Commercial)	T_{OP}	0	–	+70	ºC
Recommended operating temperature (Extended)	T_{OP}	-40	–	+85	ºC

1. Voltages with respect to ground unless otherwise specified.

Table 6. I/O Electrical Characteristics

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage[2]		V_{IL}	–	–	0.8	V	
Input High voltage[2]		V_{IH}	2.0	–	–	V	
Output Low voltage		V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
		V_{OL}	–	–	10	%V_{CC}	I_{OL} < 10 µA
Output Low voltage (Open drain LED driver)		V_{OLL}	–	–	0.7	V	I_{OLL} = 10 mA
Output High voltage		V_{OH}	2.4	–	–	V	I_{OH} = 40 µA
		V_{OH}	90	–	–	%V_{CC}	I_{OH} < 10 µA
Output rise time TCLK & RCLK	CMOS	–	–	3	12	ns	C_{LOAD} = 20 pF
	TTL	–	–	2	8	ns	

1. Typical values are at 25℃ and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.

Table 6. I/O Electrical Characteristics (Continued)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Output fall time TCLK & RCLK	CMOS	–	–	3	12	ns	C_{LOAD}= 20 pF
	TTL	–	–	2	8	ns	
CLKI rise time (externally driven)		–	–	–	10	ns	
CLKI duty cycle (externally driven)		–	–		40/60	%	
Supply current	Normal Mode	I_{CC}	–	65	85	mA	Idle Mode
		I_{CC}	–	95	120	mA	Transmitting on TP
		I_{CC}	–	90	120	mA	Transmitting on AUI
	Power Down Mode	I_{CC}	–	0.75	2	mA	

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.

Table 7. AUI Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	I_{IL}	–	–	-700	µA	–
Input High current	I_{IH}	–	–	500	µA	–
Differential output voltage	V_{OD}	±550	–	±1200	mV	–
Differential squelch threshold	V_{DS}	150	260	350	mV	5 MHz square wave input

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 8. Twisted-Pair Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	
Transmit timing jitter addition[2]	–	–	±6.4	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections[2, 3]	–	–	±3.5	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 8. Twisted-Pair Electrical Characteristics (Continued)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Receive input impedance		ZIN	–	20	–	kΩ	Between TPIP/TPIN, CIP/CIN & DIP/DIN
Differential Squelch Threshold	Normal Threshold NTH = High	VDS	300	395	585	mV	5 MHz square wave input
	Reduced Threshold NTH = Low	VDS	180	250	345	mV	5 MHz square wave input

1. Typical values are at 25℃ and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 9. Switching Characteristics

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Jabber Timing	Maximum transmit time	–	20	–	150	ms
	Unjab time	–	250	–	750	ms
Link Integrity Timing	Time link loss receive	–	50	–	150	ms
	Link min receive	–	2	–	7	ms
	Link max receive	–	50	–	150	ms
	Link transmit period	–	8	10/20	24	ms

1. Typical values are at 25℃ and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 10. RCLK/Start-of-Frame Timing

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Decoder acquisition time	AUI	tDATA	–	900	1100	ns
	TP	tDATA	–	1200	1500	ns
CD turn-on delay	AUI	tCD	–	25	200	ns
	TP	tCD	–	420	550	ns
Receive data setup from RCLK	Mode 1	tRDS	60	70	–	ns
	Modes 2 through 5	tRDS	30	45	–	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	–	ns
	Modes 2 through 5	tRDH	30	45	–	ns
RCLK shut off delay from CD assert (Mode 3 and Mode 5)		tSWS	–	±100	–	ns

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 11. RCLK/End-of-Frame Timing

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Units
RCLK after CD off	Min	t_{RC}	5	1	–	5	–	BT
RXD throughput delay	Max	t_{RD}	400	375	375	375	375	ns
CD turn off delay[2]	Max	t_{CDOFF}	500	475	475	475	475	ns
Receive block out after TEN off	Typ[1]	t_{IFG}	5	50	–	–	–	BT
RCLK switching delay after CD off (Mode 3 and 5)	Typ[1]	t_{SWE}	–	–	120(±80)	–	120(±80)	ns

1. Typical values are at 25℃ and are for design aid only, are not guaranteed, and are not subject to production testing.
2. CD turn-off delay measured from middle of last bit: timing specification is unaffected by the value of the last bit.

Table 12. Transmit Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
TEN setup from TCLK	t_{EHCH}	22	–	–	ns
TXD setup from TCLK	t_{DSCH}	22	–	–	ns
TEN hold after TCLK	t_{CHEL}	5	–	–	ns
TXD hold after TCLK	t_{CHDU}	5	–	–	ns
Transmit start-up delay - AUI	t_{STUD}	–	220	450	ns
Transmit start-up delay - TP	t_{STUD}	–	430	450	ns
Transmit through-put delay - AUI	t_{TPD}	–	–	300	ns
Transmit through-put delay - TP	t_{TPD}	–	305	350	ns

1. Typical values are at 25℃ and are for design aid only, are not guaranteed, and are not subject to production testing.

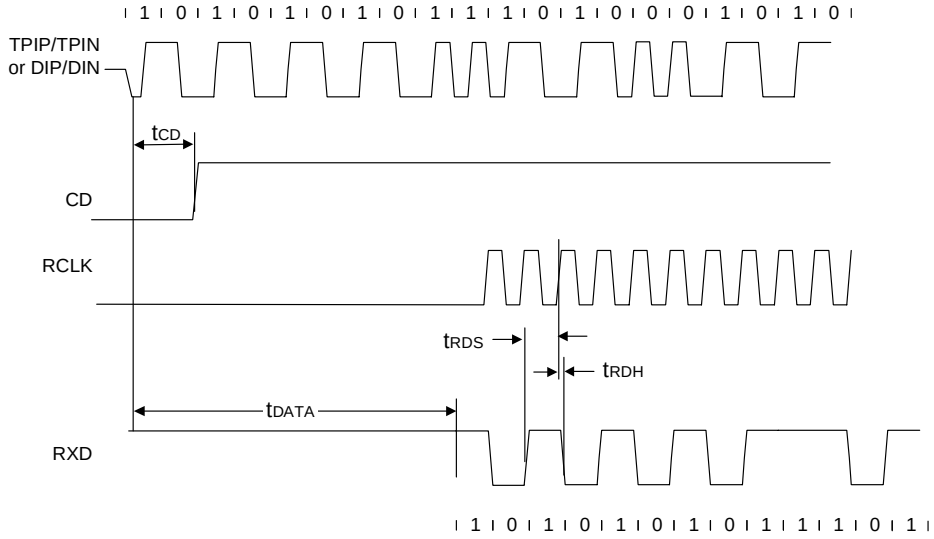
Table 13. Collision, COL/CI Output and Loopback Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
COL turn-on delay	t_{COLD}	–	40	500	ns
COL turn-off delay	t_{COLOFF}	–	420	500	ns
COL (SQE) Delay after TEN off	t_{SQED}	0.65	1.2	1.6	µs
COL (SQE) Pulse Duration	t_{SQEP}	500	1000	1500	ns
LBK setup from TEN	t_{KHEH}	10	25	–	ns
LBK hold after TEN	t_{KHEL}	10	0	–	ns

1. Typical values are at 25℃ and are for design aid only, are not guaranteed, and are not subject to production testing.

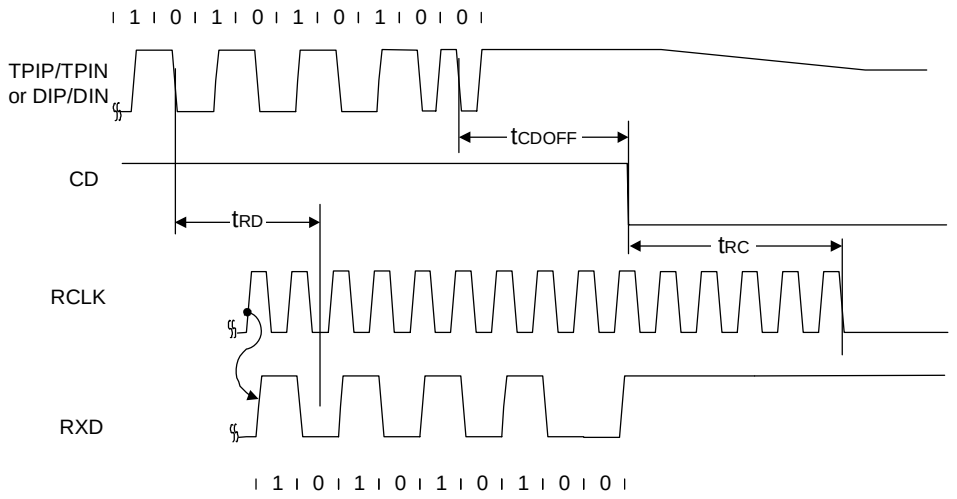
4.1 Timing Diagrams for Mode 1 (MD2, 1, 0 = Low, Low, Low) Figures 16 - 21

Figure 16. Mode 1 RCLK/Start-of-Frame Timing



Note: RXD changes 25 ns after the rising edge of RCLK.

Figure 17. Mode 1 RCLK/End-of-Frame Timing



Note: RXD changes 25 ns after the rising edge of RCLK.

Figure 18. Mode 1 Transmit Timing

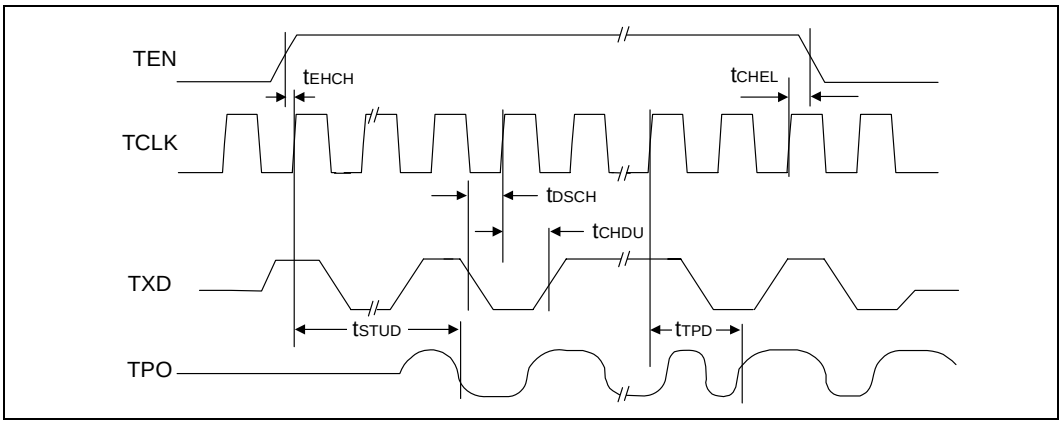


Figure 19. Mode 1 Collision Detect Timing

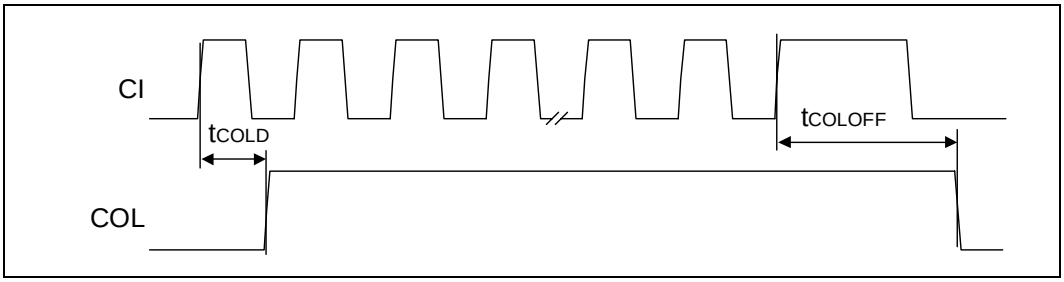


Figure 20. Mode 1 COL/SQE Output Timing/CI Output Timing

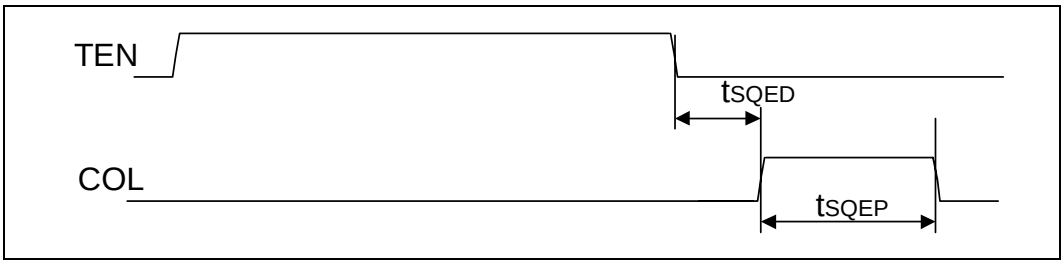
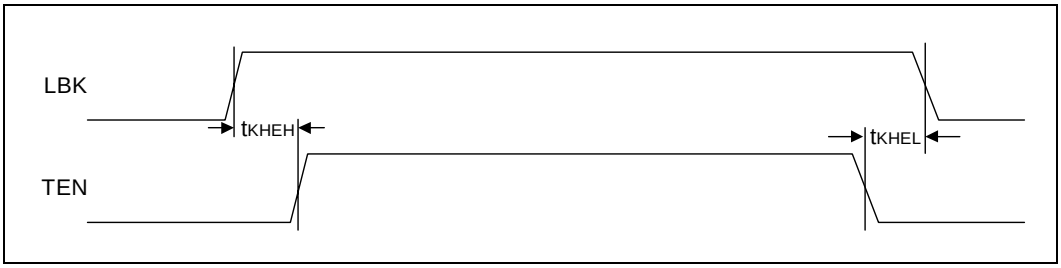
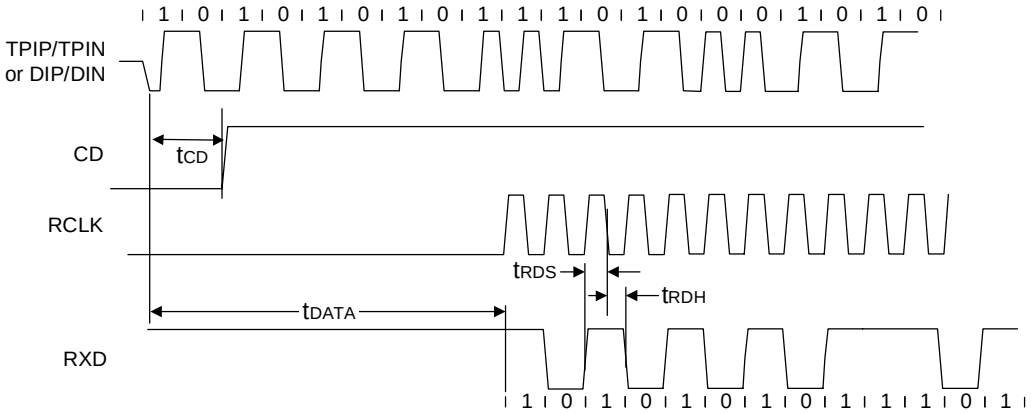


Figure 21. Mode 1 Loopback Timing



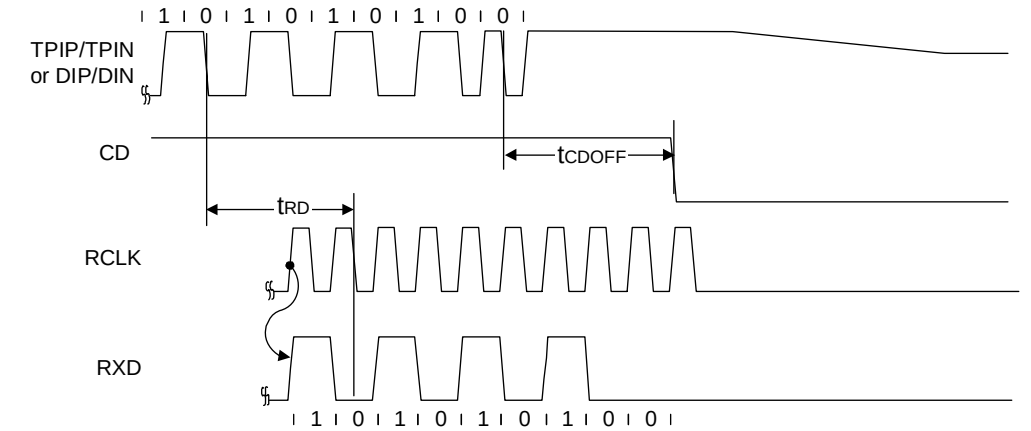
4.2 Timing Diagrams for Mode 2 (MD2, 1, 0 = Low, Low, High) Figures 22 - 27

Figure 22. Mode 2 RCLK/Start-of-Frame Timing



Note: RXD changes at the rising edge of RCLK. The controller should sample at the falling edge.

Figure 23. Mode 2 RCLK/End-of-Frame Timing



Note: RXD changes at the rising edge of RCLK. The controller should sample at the falling edge.

Figure 24. Mode 2 Transmit Timing

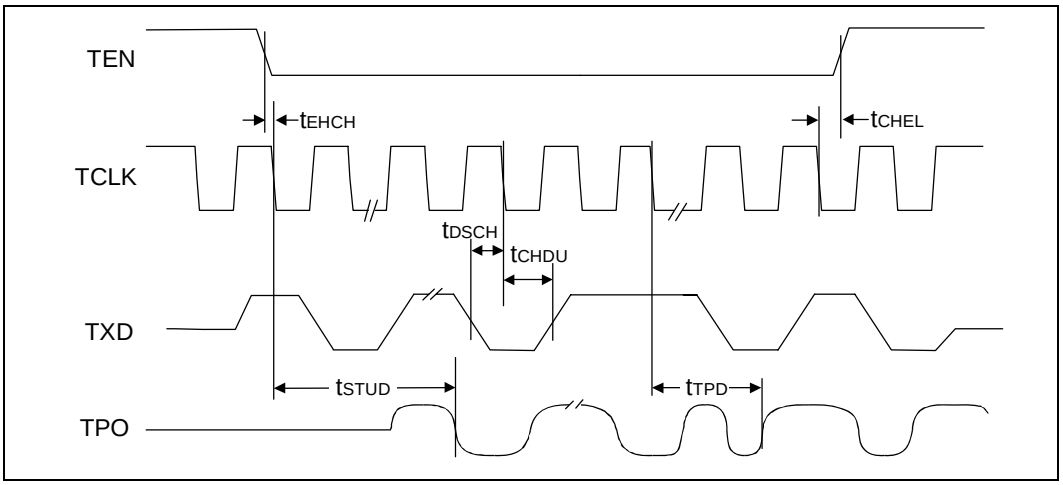


Figure 25. Mode 2 Collision Detect Timing

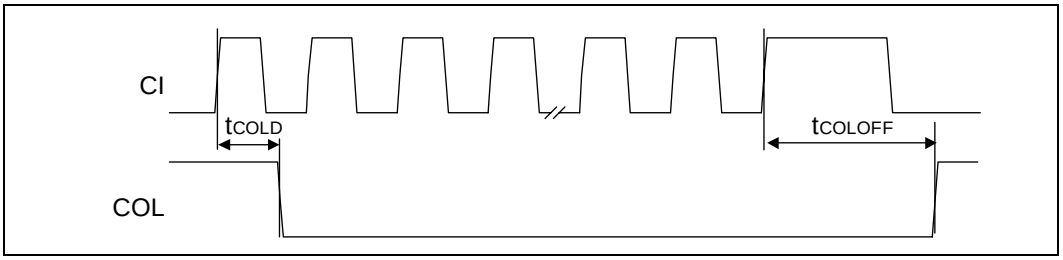


Figure 26. Mode 2 COL/SQE Output Timing

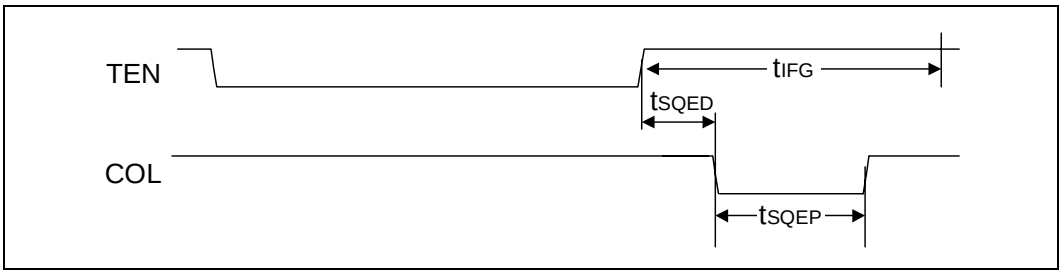
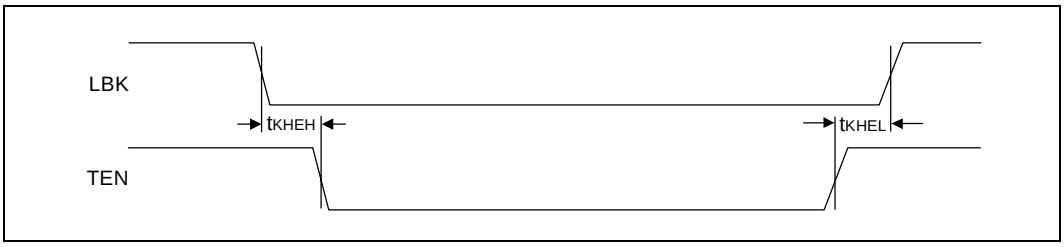
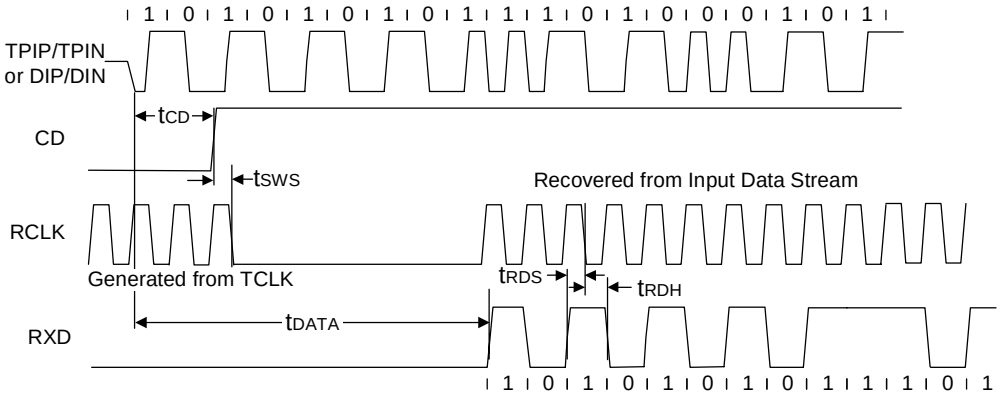


Figure 27. Mode 2 Loopback Timing



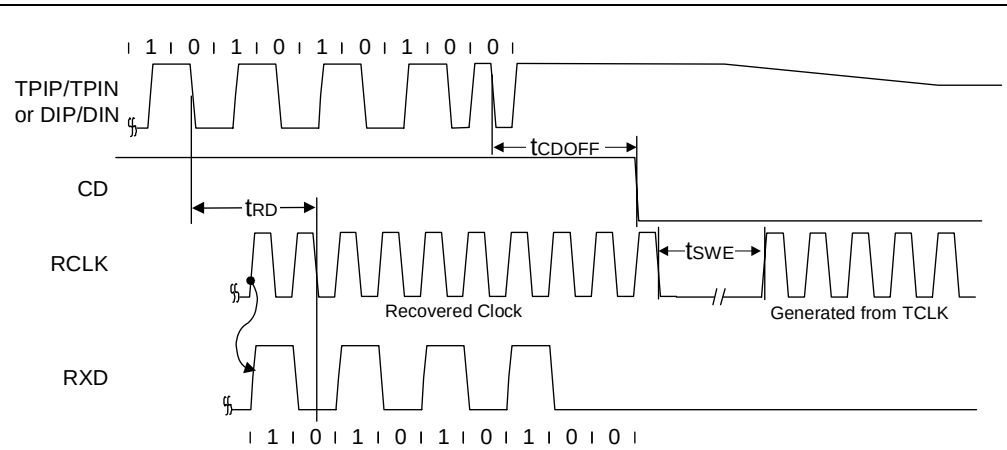
4.3 Timing Diagrams for Mode 3 (MD2, 1, 0 = Low, High, Low) Figures 28 - 33

Figure 28. Mode 3 RCLK/Start-of-Frame Timing



Note: RXD changes at the rising edge of RCLK. The controller should sample at the falling edge.

Figure 29. Mode 3 RCLK/End-of-Frame Timing



Note: RXD changes at the rising edge of RCLK. The controller should sample at the falling edge.

Figure 30. Mode 3 Transmit Timing

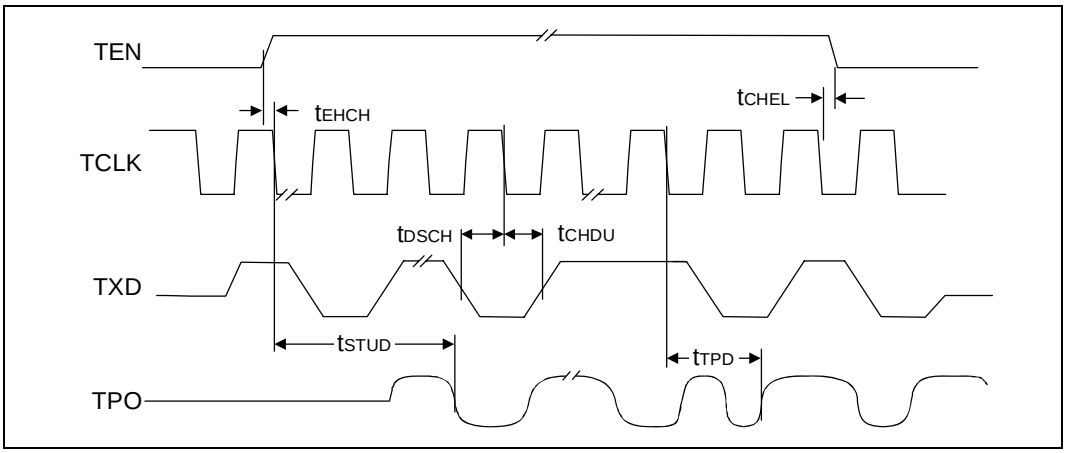


Figure 31. Mode 3 Collision Detect Timing

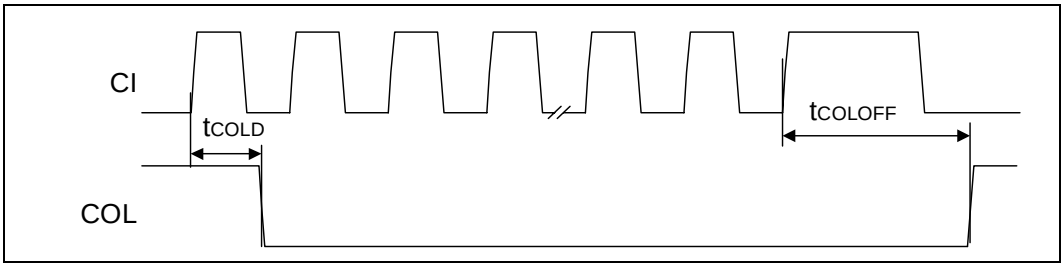


Figure 32. Mode 3 COL/SQE Output Timing

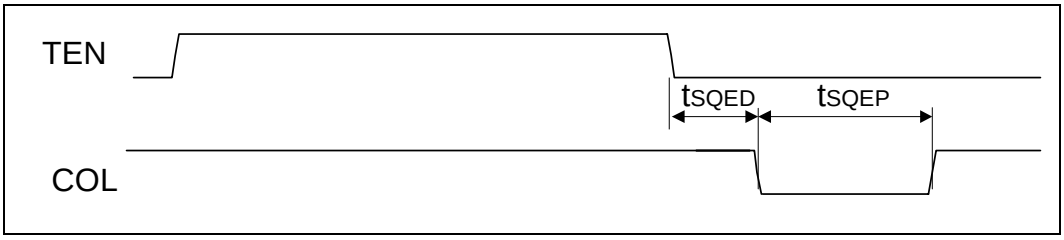
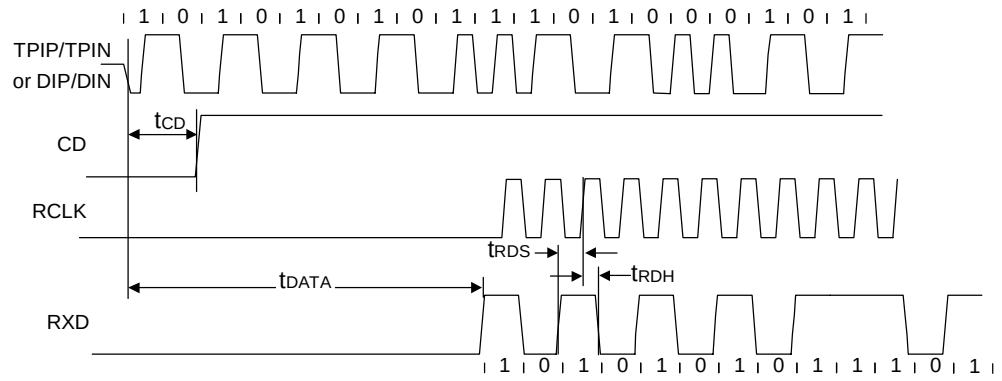


Figure 33. Mode 3 Loopback Timing

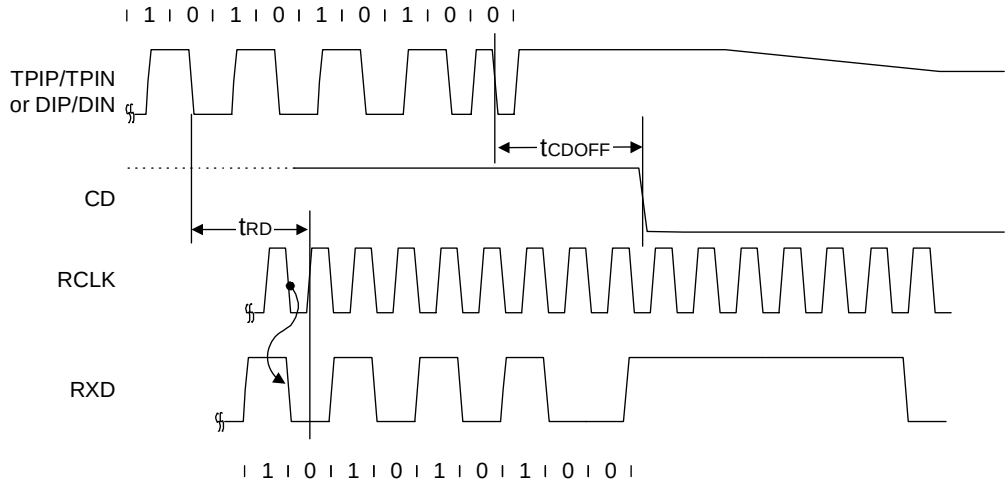
4.4 Timing Diagrams for Mode 4 (MD2, 1, 0 = Low, High, High) Figures 34 - 39

Figure 34. Mode 4 RCLK/Start-of-Frame Timing



Note: RXD changes at the rising edge of RCLK. The controller should sample at the falling edge.

Figure 35. Mode 4 RCLK/End-of-Frame Timing



Note: RXD changes at the rising edge of RCLK. The controller should sample at the falling edge.

Figure 36. Mode 4 Transmit Timing

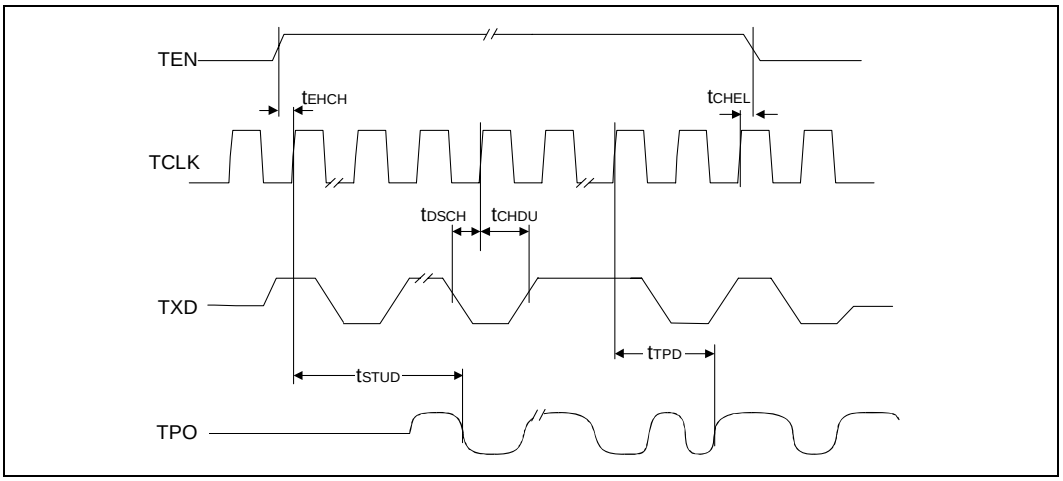


Figure 37. Mode 4 Collision Detect Timing

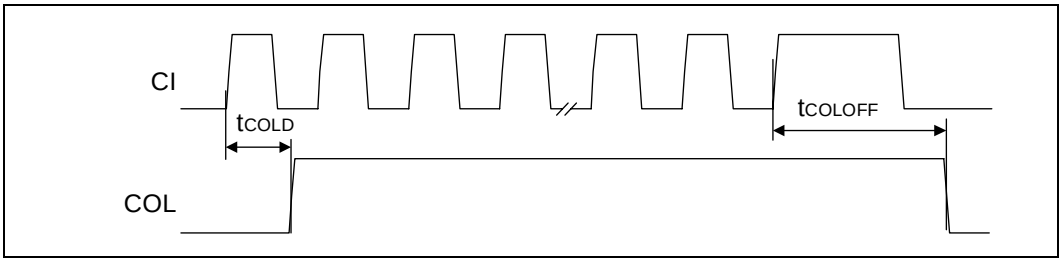


Figure 38. Mode 4 COL/SQE Output Timing

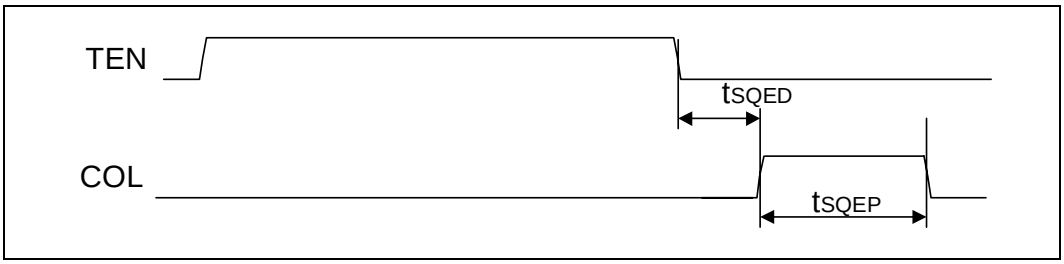
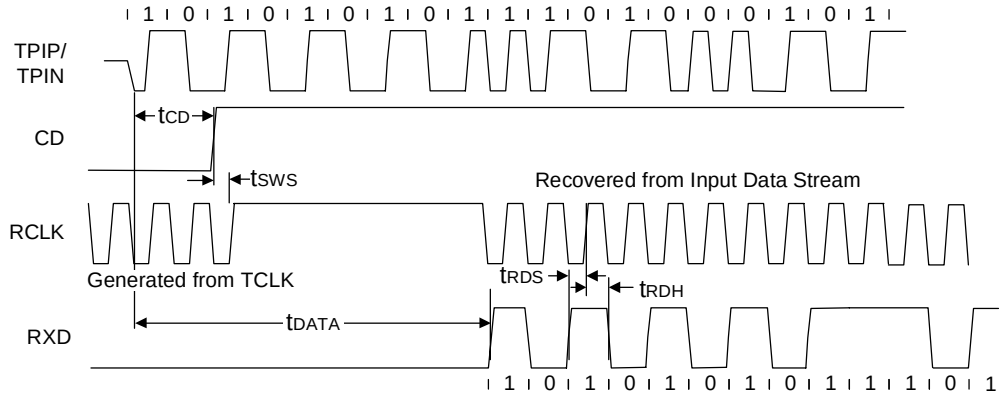


Figure 39. Mode 4 Loopback Timing

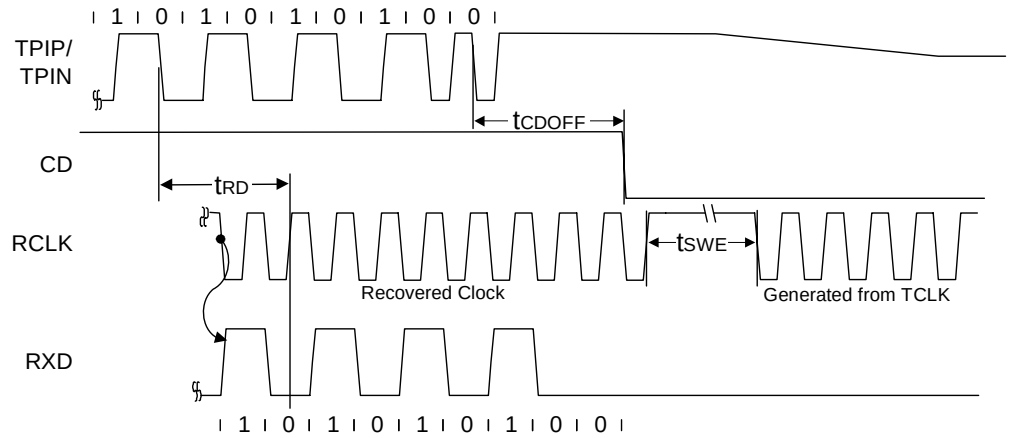
4.5 Timing Diagrams for Mode 5 (MD2, 1, 0 = High, High, Low) Figures 40 - 45

Figure 40. Mode 5 RCLK/Start-of-Frame Timing



Note: RXD changes at the rising edge of RCLK. The controller should sample at the falling edge.

Figure 41. Mode 5 RCLK/End-of-Frame Timing



Note: RXD changes at the rising edge of RCLK. The controller should sample at the falling edge.

Figure 42. Mode 5 Transmit Timing

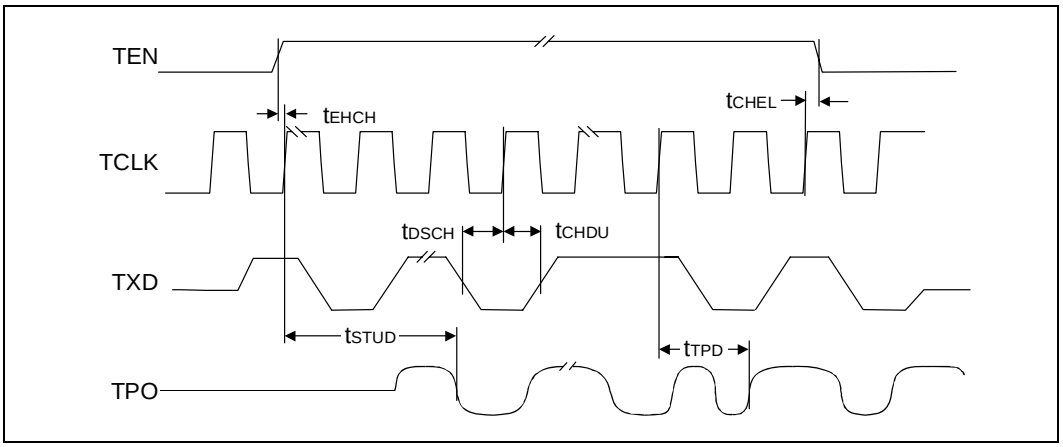


Figure 43. Mode 5 Collision Detect Timing

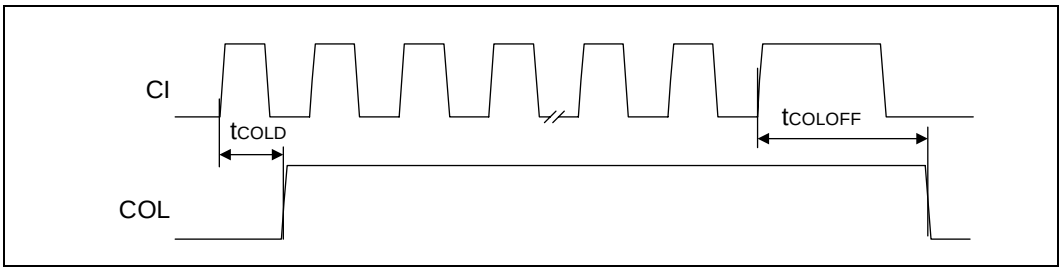


Figure 44. Mode 5 COL/SQE Output Timing

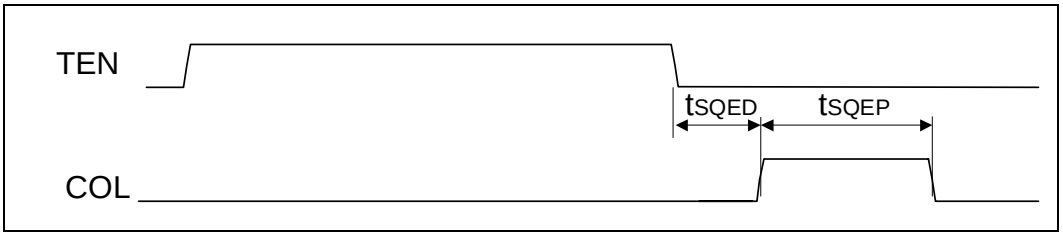


Figure 45. Mode 5 Loopback Timing

5.0 Package Specifications

Figure 46. 44-Pin PLCC Package Specifications

44-Pin Plastic Leaded Chip Carrier

- Part Number LXT908PC - Commercial temperature range (0°C to +70°C)
- Part Number LXT908PE - Extended temperature range (-40°C to +85°C)

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	0.050	–	1.270	–
C	0.026	0.032	0.660	0.813
D	0.685	0.695	17.399	17.653
D1	0.650	0.656	16.510	16.662
F	0.013	0.021	0.330	0.533

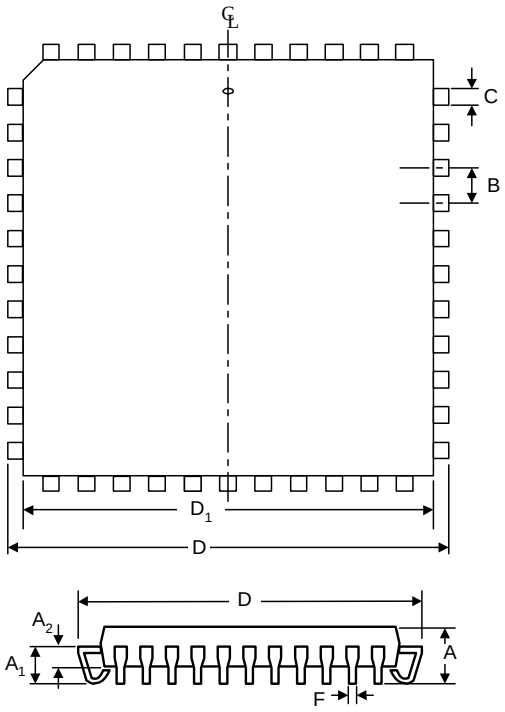
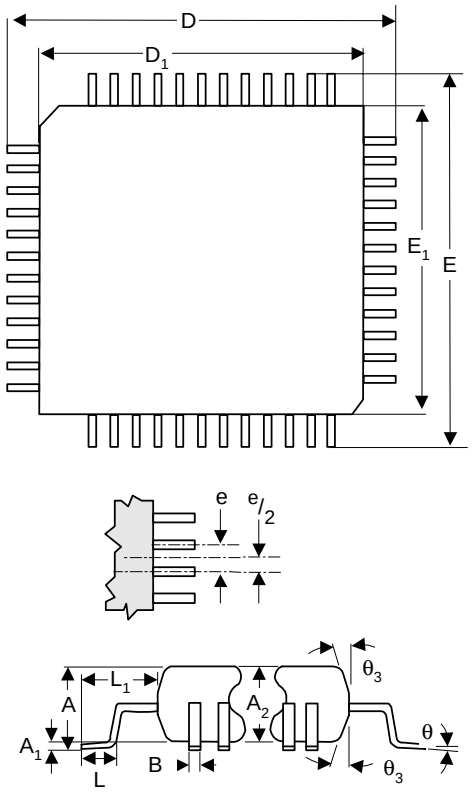


Figure 47. 64-Pin LQFP Package Specifications

64-Pin Low-Profile Quad Flat Package

- Part Number LXT908LC (Commercial Temperature Range)
- Part Number LXT908LE (Extended Temperature Range)

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.063	–	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	.011	0.17	0.27
D	0.472 BSC		12.00 BSC	
D1	0.394 BSC		10.00 BSC	
E	0.472 BSC		12.00 BSC	
E1	0.394 BSC		10.00 BSC	
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
L1	0.039 REF		1.00 REF	
θ_3	11^o	13^o	11^o	13^o
θ	0^o	7^o	0^o	7^o



5.1 Top-Label Marking

Figure 48 shows a sample LQFP package for the LXT908 Transceiver.

Note: In contrast to the Pb-Free (RoHS-compliant) LQFP packages, the non-RoHS-compliant packages do not have the “e3” symbol in the last line of the package label.

Figure 48. Sample LQFP Package - Intel® LXT908 Transceiver

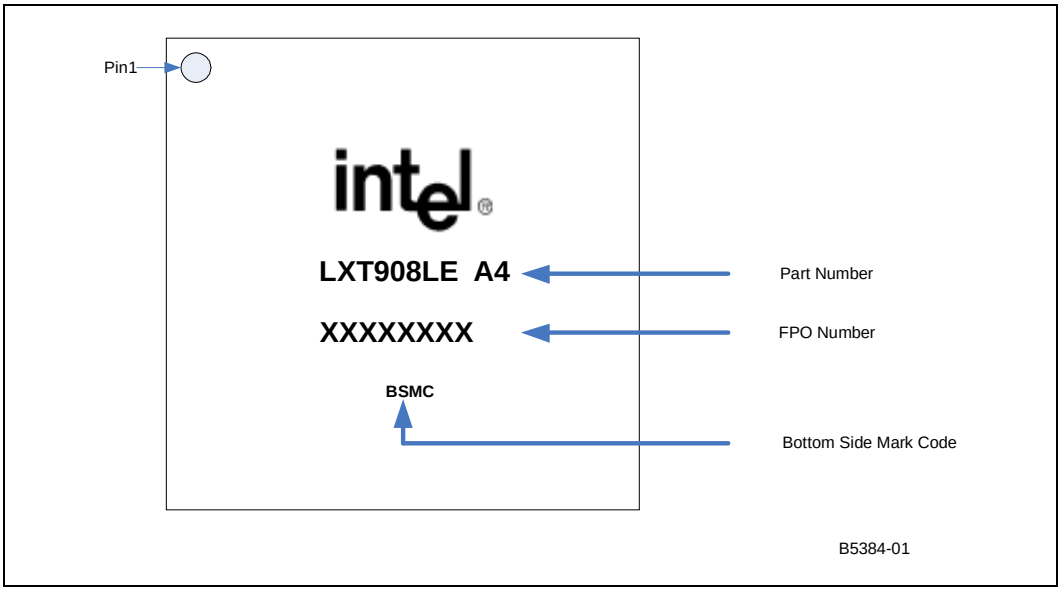


Figure 49 shows a sample Pb-Free (RoHS-compliant) LQFP package for the LXT908 Transceiver.

Figure 49. Sample Pb-Free (RoHS-Compliant) LQFP Package - Intel® LXT908 Transceiver

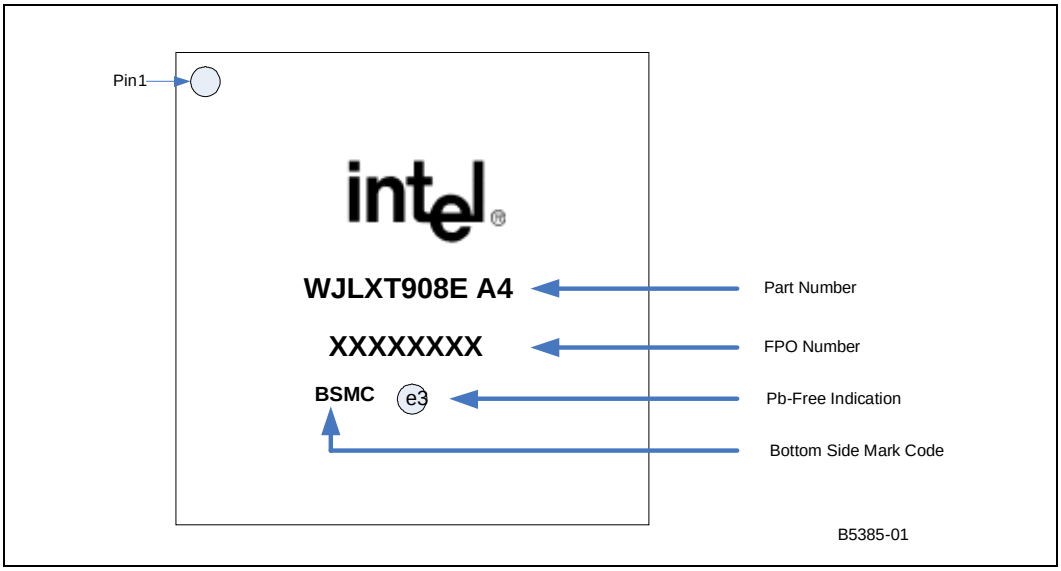


Figure 50 shows a sample PLCC package for the LXT908 Transceiver.

Note: In contrast to the Pb-Free (RoHS-compliant) PLCC packages, the non-RoHS-compliant packages do not have the “e3” symbol in the last line of the package label.

Figure 50. Sample PLCC Package - Intel® LXT908 Transceiver

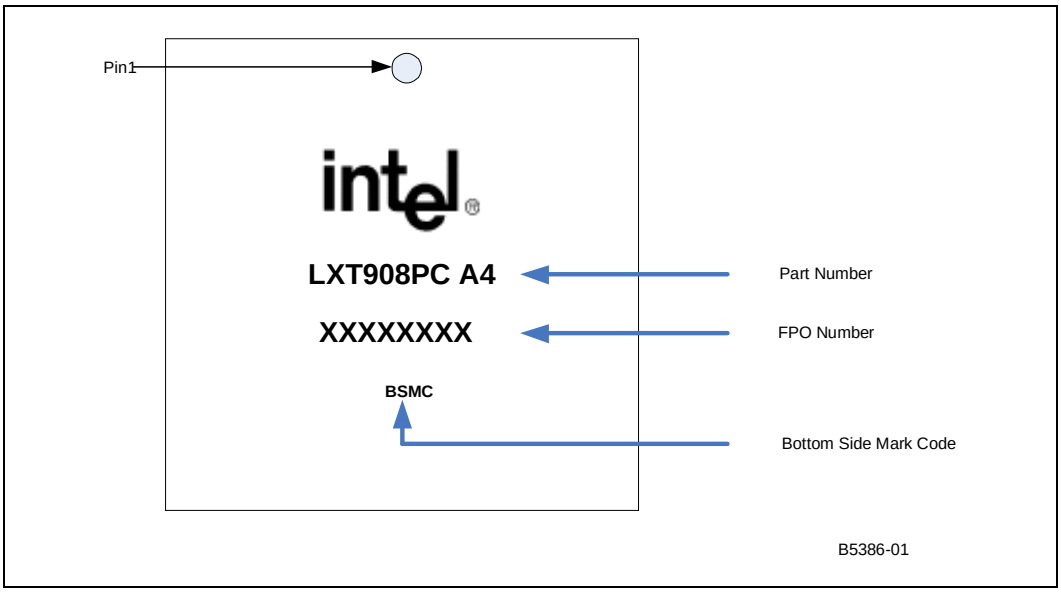
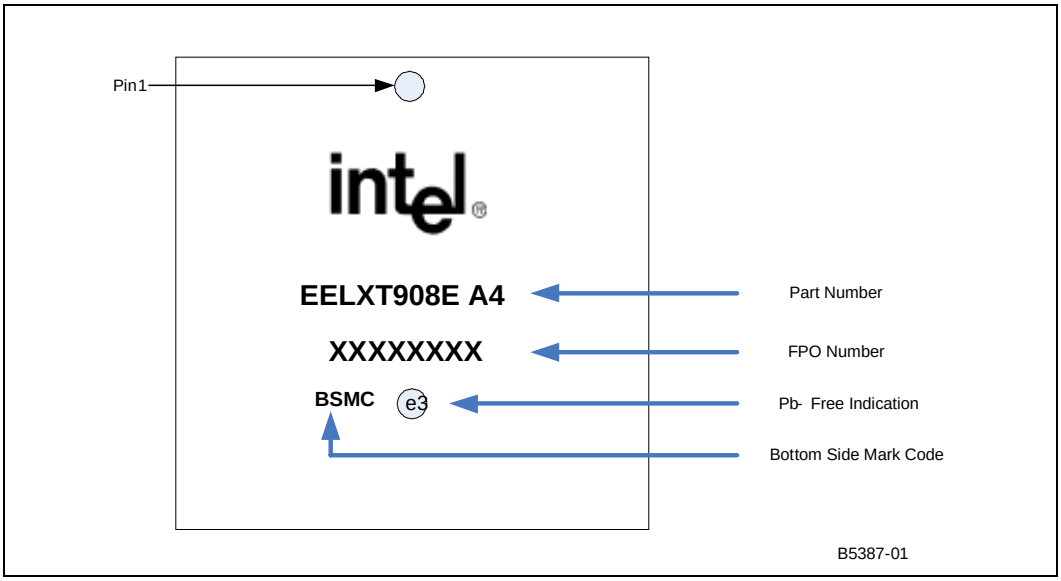


Figure 51 shows a sample Pb-Free (RoHS-compliant) PLCC package for the LXT908 Transceiver.

Figure 51. Sample Pb-Free (RoHS-Compliant) PLCC Package - Intel® LXT908 Transceiver



6.0 Product Ordering Information

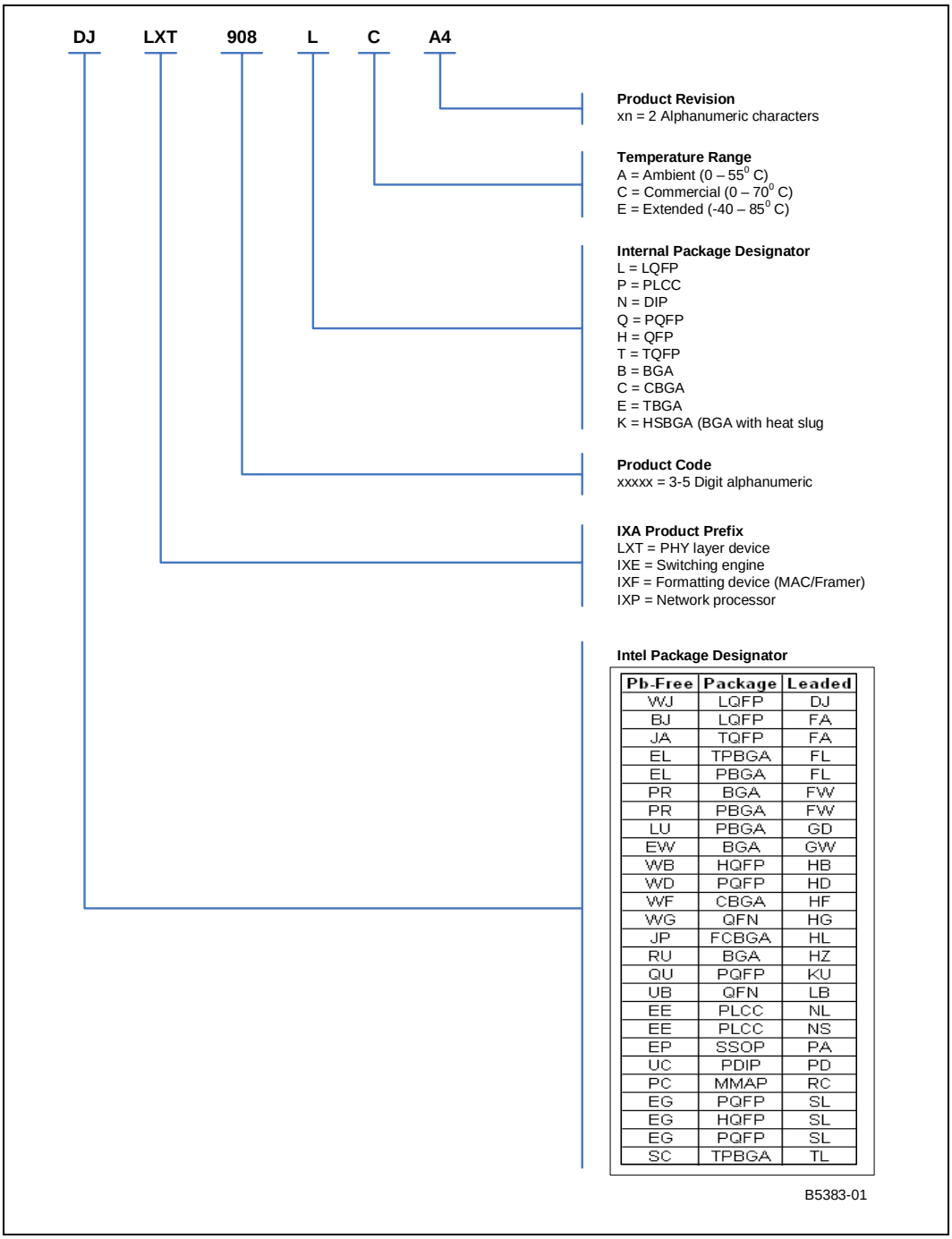
Table 14 lists product ordering information for the Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver.

Table 14. Product Information

Number	Revision	Package Type	Pin Count	RoHS Compliant
DJLXT908LC.A4	A4	LQFP	64	No
WJLXT908LC.A4	A4	LQFP	64	Yes
DJLXT908LE.A4	A4	LQFP	64	No
WJLXT908LE.A4	A4	LQFP	64	Yes
NLXT908PC.A4	A4	PLCC	44	No
EELXT908PC.A4	A4	PLCC	44	Yes
NLXT908PE.A4	A4	PLCC	44	No
EELXT908PE.A4	A4	PLCC	44	Yes

Figure 52 shows an order matrix with sample information for ordering an Intel® LXT908 Universal 3.3 V 10BASE-T and AUI Transceiver.

Figure 52. Ordering Information - Sample



Pb-Free	Package	Leaded
WJ	LQFP	DJ
BJ	LQFP	FA
JA	TQFP	FA
EL	TPBGA	FL
EL	PBGA	FL
PR	BGA	FW
PR	PBGA	FW
LU	PBGA	GD
EW	BGA	GW
WB	HQFP	HB
WD	PQFP	HD
WF	CBGA	HF
WG	QFN	HG
JP	FCBGA	HL
RU	BGA	HZ
QU	PQFP	KU
UB	QFN	LB
EE	PLCC	NL
EE	PLCC	NS
EP	SSOP	PA
UC	PDIP	PD
PC	MMAP	RC
EG	PQFP	SL
EG	HQFP	SL
EG	PQFP	SL
SC	TPBGA	TL