MONOLITHIC QUADRUPLE FIXED DELAY LINE (SERIES 3D3324)

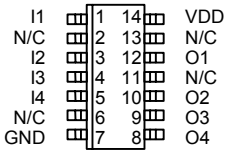
RoHS Compliant

data delay devices, inc.

FEATURES

- All-silicon, low-power CMOS technology
- Vapor phase, IR and wave solderable
- Low ground bounce noise
- Leading- and trailing-edge accuracy
- **Delay range:** 10 through 6000ns
- **Delay tolerance:** 2% or 1.0ns
- **Temperature stability:** ±3% typ (-40C to 85C)
- **Vdd stability:** ±1% typical (3.0V to 3.6V)
- **Minimum input pulse width:** 20% of total delay

PACKAGES



3D3324D-xx
SOIC (150 Mil)

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D3324 Quadruple Delay Line product family consists of fixed-delay CMOS integrated circuits. Each package contains four matched, independent delay lines. Delay values can range from 10ns through 6000ns. The input is reproduced at the output without inversion, shifted in time as per the user-specified dash number. The 3D3324 is CMOS-compatible and features both rising- and falling-edge accuracy.

The all-CMOS 3D3324 integrated circuit has been designed as a reliable, economic alternative to hybrid fixed delay lines. It is offered in a space saving surface mount 14-pin SOIC.

PIN DESCRIPTIONS

I1	Delay Line 1 Input
I2	Delay Line 2 Input
I3	Delay Line 3 Input
I4	Delay Line 4 Input
O1	Delay Line 1 Output
O2	Delay Line 2 Output
O3	Delay Line 3 Output
O4	Delay Line 4 Output
VDD	+3.3 Volts
GND	Ground
N/C	No Connection

TABLE 1: PART NUMBER SPECIFICATIONS

PART NUMBER	DELAY PER LINE (ns)	INPUT RESTRICTIONS			
		Max Operating Frequency	Absolute Max Oper. Freq.	Min Operating Pulse Width	Absolute Min Oper. P.W.
3D3324D-10	10 ± 1.0	33.3 MHz	100.0 MHz	15.0 ns	5.0 ns
3D3324D -15	15 ± 1.0	22.2 MHz	100.0 MHz	22.5 ns	5.0 ns
3D3324D -20	20 ± 1.0	16.7 MHz	100.0 MHz	30.0 ns	5.0 ns
3D3324D -25	25 ± 1.0	13.3 MHz	83.3 MHz	37.5 ns	6.0 ns
3D3324D -30	30 ± 1.0	11.1 MHz	71.4 MHz	45.0 ns	7.0 ns
3D3324D -40	40 ± 1.0	8.33 MHz	62.5 MHz	60.0 ns	8.0 ns
3D3324D -50	50 ± 1.0	6.67 MHz	50.0 MHz	75.0 ns	10.0 ns
3D3324D -100	100 ± 2.0	3.33 MHz	25.0 MHz	150.0 ns	20.0 ns
3D3324D -200	200 ± 4.0	1.67 MHz	12.5 MHz	300.0 ns	40.0 ns
3D3324D -500	500 ± 10	0.67 MHz	5.00 MHz	750.0 ns	100.0 ns
3D3324D -1000	1000 ± 20	0.33 MHz	2.50 MHz	1500.0 ns	200.0 ns
3D3324D -2000	2000 ± 40	0.17 MHz	1.25 MHz	3000.0 ns	400.0 ns
3D3324D -5000	5000 ± 100	0.07 MHz	0.50 MHz	7500.0 ns	1000.0 ns
3D3324D -6000	6000 ± 120	0.05 MHz	0.42 MHz	9000.0 ns	1200.0 ns

NOTES: Any delay between 10 and 6000 ns not shown is also available.

APPLICATION NOTES

OPERATIONAL DESCRIPTION

The 3D3324 quadruple delay line architecture is shown in Figure 1. The individual delay lines are composed of a number of delay cells connected in series. Each delay line produces at its output a replica of the signal present at its input, shifted in time. The delay lines are matched and share the same compensation signals, which minimizes line-to-line delay deviations over temperature and supply voltage variations.

INPUT SIGNAL CHARACTERISTICS

The Frequency and/or Pulse Width (high or low) of operation may adversely impact the specified delay accuracy of the particular device. The reasons for the dependency of the output delay accuracy on the input signal characteristics are varied and complex. Therefore a **Maximum** and an **Absolute Maximum** operating input frequency and a **Minimum** and an **Absolute Minimum** operating pulse width have been specified.

OPERATING FREQUENCY

The **Absolute Maximum Operating Frequency** specification, tabulated in **Table 1**, determines the highest frequency of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable duty cycle distortion.

The **Maximum Operating Frequency** specification determines the highest frequency of the delay line input signal for which the output delay accuracy is guaranteed.

To guarantee the **Table 1** delay accuracy for input frequencies higher than the **Maximum Operating Frequency**, the 3D3324 must be tested at the user operating frequency. Therefore, to facilitate production and device identification, **the part number will include a custom reference designator** identifying the intended frequency of operation. The programmed delay accuracy of the device is guaranteed, therefore, only at the user specified input frequency. Small input frequency variation about the selected frequency will only marginally impact the programmed delay accuracy, if at all. **Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.**

OPERATING PULSE WIDTH

The **Absolute Minimum Operating Pulse Width** (high or low) specification, tabulated in **Table 1**, determines the smallest Pulse Width of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable pulse width distortion.

The **Minimum Operating Pulse Width** (high or low) specification determines the smallest Pulse Width of the delay line input signal for which the output delay accuracy tabulated in **Table 1** is guaranteed.

To guarantee the **Table 1** delay accuracy for input pulse width smaller than the **Minimum Operating Pulse Width**, the 3D3324 must be tested at the user operating pulse width. Therefore, to facilitate production and device identification, the **part number will include a**

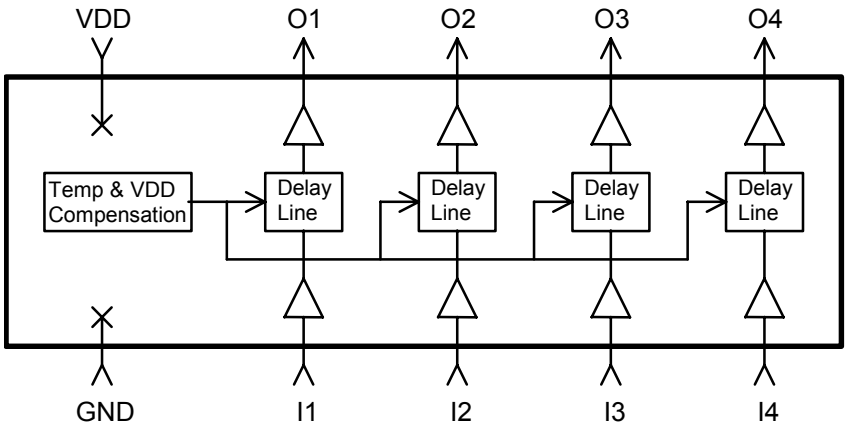


Figure 1: 3D3324 Functional Diagram

APPLICATION NOTES (CONT'D)

custom reference designator identifying the intended frequency and duty cycle of operation. The programmed delay accuracy of the device is guaranteed, therefore, only for the user specified input characteristics. Small input pulse width variation about the selected pulse width will only marginally impact the programmed delay accuracy, if at all. **Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.**

POWER SUPPLY AND TEMPERATURE CONSIDERATIONS

The delay of CMOS integrated circuits is strongly dependent on power supply and temperature. The monolithic 3D3324 programmable delay line utilizes novel and innovative compensation circuitry to minimize the delay variations induced by fluctuations in power supply and/or temperature.

The **thermal coefficient** is reduced to **300 PPM/C**, which is equivalent to a variation , over the -40C to 85C operating range, of **±3%** from the room-temperature delay settings and/or **1.0ns**, whichever is greater. The **power supply coefficient** is reduced, over the 3.0V to 3.6V operating range, to **±1%** of the delay settings at the nominal 3.3VDC power supply and/or **2.0ns**, whichever is greater. **It is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred.**

DEVICE SPECIFICATIONS

TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-1.0	1.0	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 3: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		5	mA	
High Level Input Voltage	V_{IH}	2.0		V	
Low Level Input Voltage	V_{IL}		0.8	V	
High Level Input Current	I_{IH}	-1	1	µA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}	-1	1	µA	V_{IL} = 0V
High Level Output Current	I_{OH}		-4.0	mA	V_{DD} = 4.75V V_{OH} = 2.4V
Low Level Output Current	I_{OL}	4.0		mA	V_{DD} = 4.75V V_{OL} = 0.4V
Output Rise & Fall Time	T_R & T_F		2	ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = 4 * C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/line (pf)
F = Input frequency (GHz)

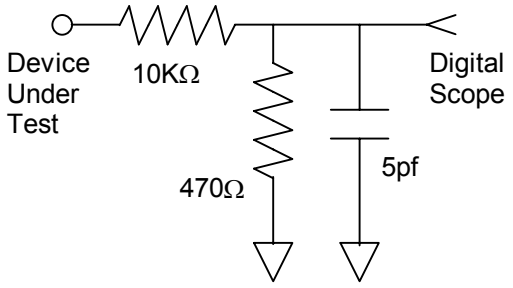
Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): 3.3V ± 0.1V
Input Pulse: High = 3.0V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width: PW_{IN} = 1.25 x Total Delay
Period: PER_{IN} = 2.5 x Total Delay

OUTPUT:
R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

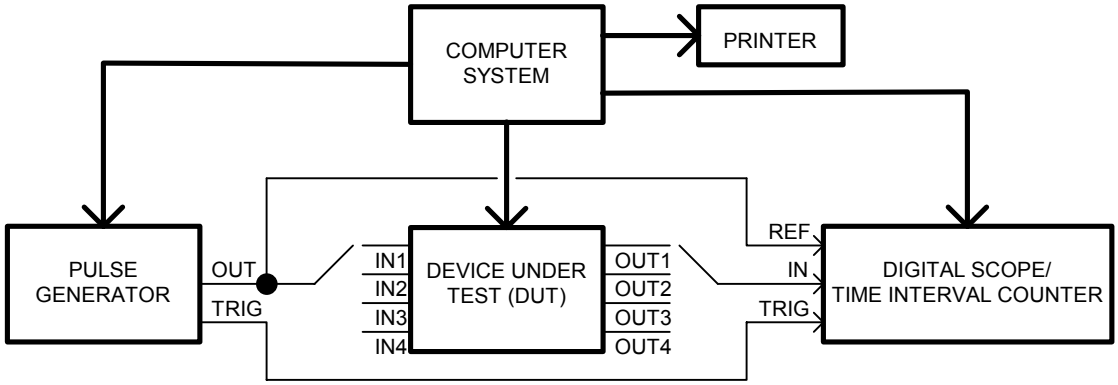


Figure 2: Test Setup

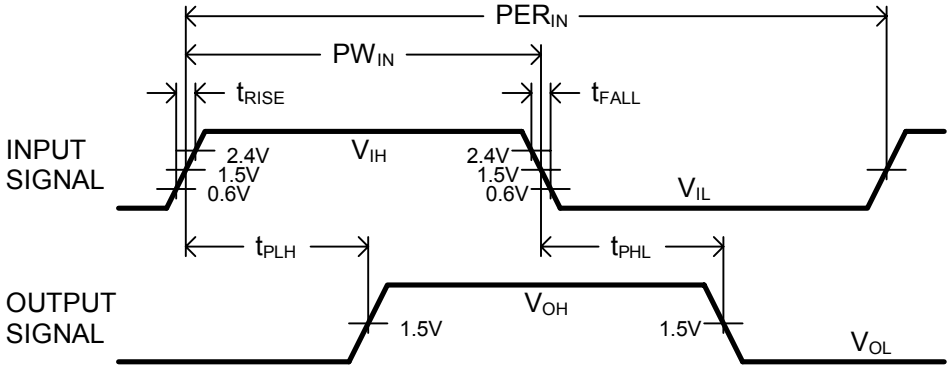


Figure 3: Timing Diagram