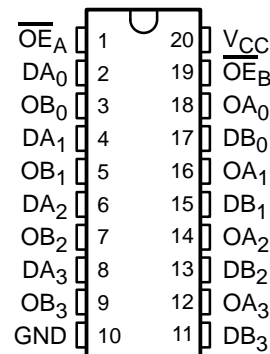# CY54FCT244T, CY74FCT244T
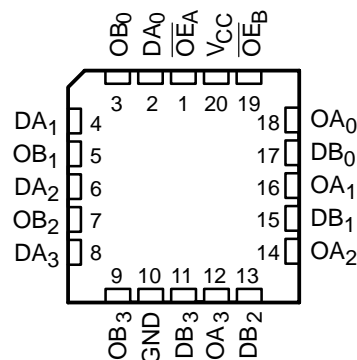# 8-BIT BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS

SCCS071 – OCTOBER 2001

- **Function, Pinout, and Drive Compatible With FCT and F Logic**
- **Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **CY54FCT244T**
  - **48-mA Output Sink Current**
    12-mA Output Source Current
- **CY74FCT244T**
  - **64-mA Output Sink Current**
    32-mA Output Source Current
- **3-State Outputs**

CY54FCT244T . . . D PACKAGE
CY74FCT244T . . . P, Q, OR SO PACKAGE
(TOP VIEW)

$\overline{OE}_A$	1	20	V_{CC}
DA_0	2	19	$\overline{OE}_B$
OB_0	3	18	OA_0
DA_1	4	17	DB_0
OB_1	5	16	OA_1
DA_2	6	15	DB_1
OB_2	7	14	OA_2
DA_3	8	13	DB_2
OB_3	9	12	OA_3
GND	10	11	DB_3

CY54FCT244T . . . L PACKAGE
(TOP VIEW)

Top pins: OB_0, DA_0, $\overline{OE}_A$, V_{CC}, $\overline{OE}_B$ (3, 2, 1, 20, 19)

DA_1	4	18	OA_0
OB_1	5	17	DB_0
DA_2	6	16	OA_1
OB_2	7	15	DB_1
DA_3	8	14	OA_2

Bottom pins: OB_3, GND, DB_3, OA_3, DB_2 (9, 10, 11, 12, 13)

description

The 'FCT244T devices are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts, while reducing power consumption. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

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ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QSOP – Q	Tape and reel	3.6	CY74FCT244DTQCT	FCT244D
	SOIC – SO	Tube	3.6	CY74FCT244DTSOC	FCT244D
		Tape and reel	3.6	CY74FCT244DTSOCT	
−40°C to 85°C	SOIC – SO	Tube	4.1	CY74FCT244CTSOC	FCT244C
		Tape and reel	4.1	CY74FCT244CTSOCT	
	QSOP – Q	Tape and reel	4.1	CY74FCT244CTQCT	FCT244C
	DIP – P	Tube	4.6	CY74FCT244ATPC	CY74FCT244ATPC
	SOIC – SO	Tube	4.6	CY74FCT244ATSOC	FCT244A
		Tape and reel	4.6	CY74FCT244ATSOCT	
	QSOP – Q	Tape and reel	4.6	CY74FCT244ATQCT	FCT244A
	SOIC – SO	Tube	6.5	CY74FCT244TSOC	FCT244
		Tape and reel	6.5	CY74FCT244TSOCT	
	QSOP – Q	Tape and reel	6.5	CY74FCT244TQCT	FCT244
−55°C to 125°C	CDIP – D	Tube	4.6	CY54FCT244CTDMB	
	LCC – L	Tube	4.6	CY54FCT244CTLMB	
	CDIP – D	Tube	5.1	CY54FCT244ATDMB	
	LCC – L	Tube	5.1	CY54FCT244ATLMB	
	CDIP – D	Tube	7	CY54FCT244TDMB	
	LCC – L	Tube	7	CY54FCT244TLMB	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
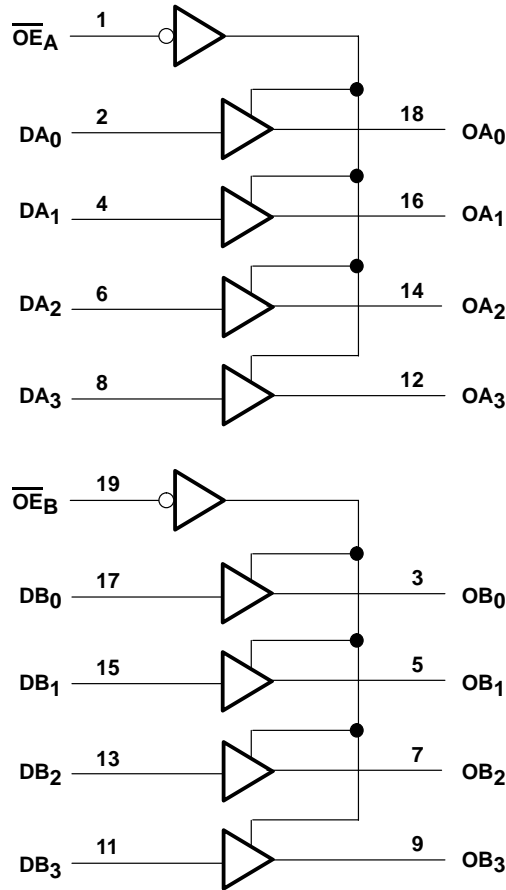
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_A$	$\overline{OE}_B$	D	O
L	L	L	L
L	L	H	H
H	H	X	Z

H = High logic level, L = Low logic level,
X = Don't care, Z = High-impedance state

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logic diagram (positive logic)

Pin	Signal		Pin	Signal
1	$\overline{OE}_A$			
2	DA_0		18	OA_0
4	DA_1		16	OA_1
6	DA_2		14	OA_2
8	DA_3		12	OA_3
19	$\overline{OE}_B$			
17	DB_0		3	OB_0
15	DB_1		5	OB_1
13	DB_2		7	OB_2
11	DB_3		9	OB_3

absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential . . . . −0.5 V to 7 V
DC input voltage range . . . . −0.5 V to 7 V
DC output voltage range . . . . −0.5 V to 7 V
DC output current (maximum sink current/pin) . . . . 120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package . . . . 69°C/W
                                                        Q package . . . . 68°C/W
                                                        SO package . . . . 58°C/W
Ambient temperature range with power applied, T_A . . . . −65°C to 135°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.
  Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 2)

		CY54FCT244T			CY74FCT244DT			CY74FCT244T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			2			V
V_{IL}	Low-level input voltage			0.8			0.8			0.8	V
I_{OH}	High-level output current			−12			−32			−32	mA
I_{OL}	Low-level output current			48			64			64	mA
T_A	Operating free-air temperature	−55		125	0		70	−40		85	°C

NOTE 2:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		CY54FCT244T			CY74FCT244T			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{IN} = −18 mA		−0.7	−1.2				V
	V_{CC} = 4.75 V,	I_{IN} = −18 mA					−0.7	−1.2	
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.3					V
	V_{CC} = 4.75 V	I_{OH} = −32 mA				2			
		I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA					0.3	0.55	
V_{hys}	All inputs			0.2			0.2		V
I_I	V_{CC} = 5.5 V,	V_{IN} = V_{CC}			5				µA
	V_{CC} = 5.25 V,	V_{IN} = V_{CC}						5	
I_{IH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V						±1	
I_{IL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V						±1	
I_{OZH}	V_{CC} = 5.5 V,	V_{OUT} = 2.7 V			10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V						10	
I_{OZL}	V_{CC} = 5.5 V,	V_{OUT} = 0.5 V			−10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V						−10	
I_{OS}‡	V_{CC} = 5.5 V,	V_{OUT} = 0 V	−60	−120	−225				mA
	V_{CC} = 5.25 V,	V_{OUT} = 0 V				−60	−120	−225	
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V			±1			±1	µA
I_{CC}	V_{CC} = 5.5 V, $V_{IN} \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V			0.1	0.2				mA
	V_{CC} = 5.25 V, $V_{IN} \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V						0.1	0.2	
ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open			0.5	2				mA
	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open						0.5	2	
I_{CCD}¶	V_{CC} = 5.5 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B$ = GND, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V			0.06	0.12				mA/ MHz
	V_{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B$ = GND, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V						0.06	0.12	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT244T			CY74FCT244T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_C#	V_{CC} = 5.5 V, Outputs open, $\overline{OE}_A = \overline{OE}_B$ = GND	One bit switching at f_1 = 10 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V		0.7	1.4				mA
			V_{IN} = 3.4 V or GND		1	2.4				
		Eight bits switching at f_1 = 2.5 MHz at 50% duty cycle	V_{IN} = 0.2 V or $V_{IN} \geq V_{CC} - 0.2$ V		1.3	2.6‖				
			V_{IN} = 3.4 V or GND		3.3	10.6‖				
	V_{CC} = 5.25 V, Outputs open, $\overline{OE}_A = \overline{OE}_B$ = GND	One bit switching at f_1 = 10 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V					0.7	1.4	
			V_{IN} = 3.4 V or GND					1	2.4	
		Eight bits switching at f_1 = 2.5 MHz at 50% duty cycle	V_{IN} = 0.2 V or $V_{IN} \geq V_{CC} - 0.2$ V					1.3	2.6‖	
			V_{IN} = 3.4 V or GND					3.3	10.6‖	
C_i					5	10		5	10	pF
C_O					9	12		9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

\# I_C = I_{CC} + $\Delta I_{CC} \times D_H \times N_T$ + I_{CCD} (f_0/2 + $f_1 \times N_1$)

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

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switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT244T		CY54FCT244AT		CY54FCT244CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	O	1.5	7	1.5	5.1	1.5	4.6	ns
t_{PHL}			1.5	7	1.5	5.1	1.5	4.6	
t_{PZH}	$\overline{OE}$	O	1.5	8.5	1.5	6.5	1.5	6.5	ns
t_{PZL}			1.5	8.5	1.5	6.5	1.5	6.5	
t_{PHZ}	$\overline{OE}$	O	1.5	7.5	1.5	5.9	1.5	5.7	ns
t_{PLZ}			1.5	7.5	1.5	5.9	1.5	5.7	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT244T		CY74FCT244AT		CY74FCT244CT		CY74FCT244DT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	O	1.5	6.5	1.5	4.6	1.5	4.1	1.5	3.6	ns
t_{PHL}			1.5	6.5	1.5	4.6	1.5	4.1	1.5	3.6	
t_{PZH}	$\overline{OE}$	O	1.5	8	1.5	6.2	1.5	5.8	1.5	4.8	ns
t_{PZL}			1.5	8	1.5	6.2	1.5	5.8	1.5	4.8	
t_{PHZ}	$\overline{OE}$	O	1.5	7	1.5	5.6	1.5	5.2	1.5	4	ns
t_{PLZ}			1.5	7	1.5	5.6	1.5	5.2	1.5	4	

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
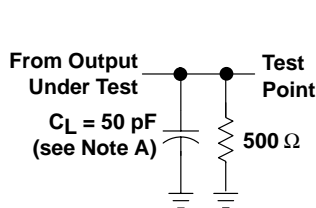
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS
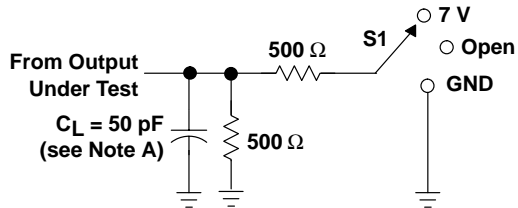
LOAD CIRCUIT FOR 3-STATE OUTPUTS
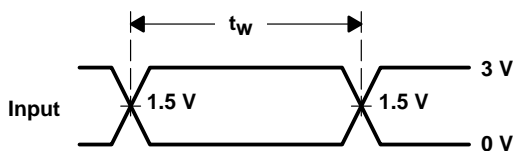
VOLTAGE WAVEFORMS PULSE DURATION
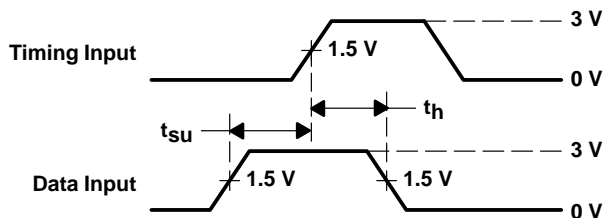
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES
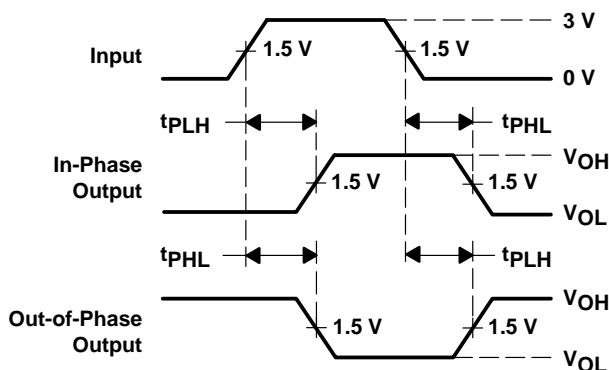
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS
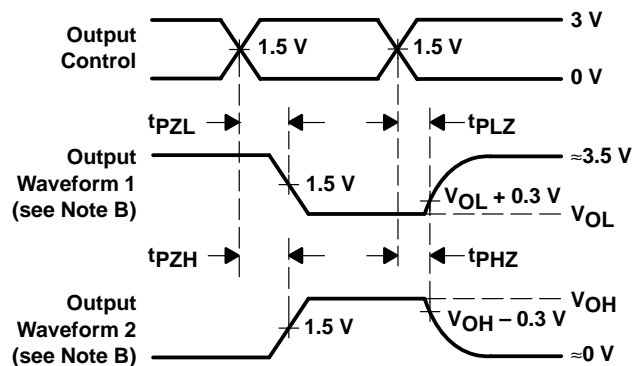
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9220301M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9220301MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-9220301MSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
5962-9220302M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9220302MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-9220302MSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
5962-9220303M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9220303MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-9220303MSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
CY54FCT244ATDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
CY54FCT244ATLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
CY54FCT244ATW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
CY54FCT244CTDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
CY54FCT244CTW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
CY54FCT244TDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
CY54FCT244TLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
CY54FCT244TW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
CY74FCT244ATPC	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT244ATPCE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT244ATQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT244ATQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT244ATQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT244ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244ATSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244ATSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244ATSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244ATSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244ATSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244CTQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT244CTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT244CTQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT244CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						no Sb/Br)		
CY74FCT244CTSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244CTSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244CTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244CTSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244DTQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT244DTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT244DTQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT244DTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244DTSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244DTSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244DTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244DTSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244DTSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244TQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT244TQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT244TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244TSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244TSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244TSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244TSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT244TSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check

http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT244ATQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT244CTQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244CTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT244DTQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244DTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT244TQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT244ATQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT244ATSOCT	SOIC	DW	20	2000	346.0	346.0	41.0
CY74FCT244CTQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT244CTSOCT	SOIC	DW	20	2000	346.0	346.0	41.0
CY74FCT244DTQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT244DTSOCT	SOIC	DW	20	2000	346.0	346.0	41.0
CY74FCT244TQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT244TSOCT	SOIC	DW	20	2000	346.0	346.0	41.0

J (R−GDIP−T**)   CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN
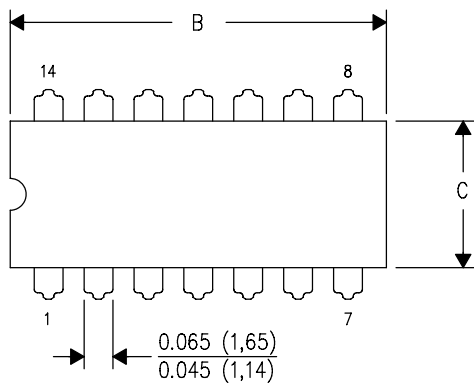
DIM / PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)
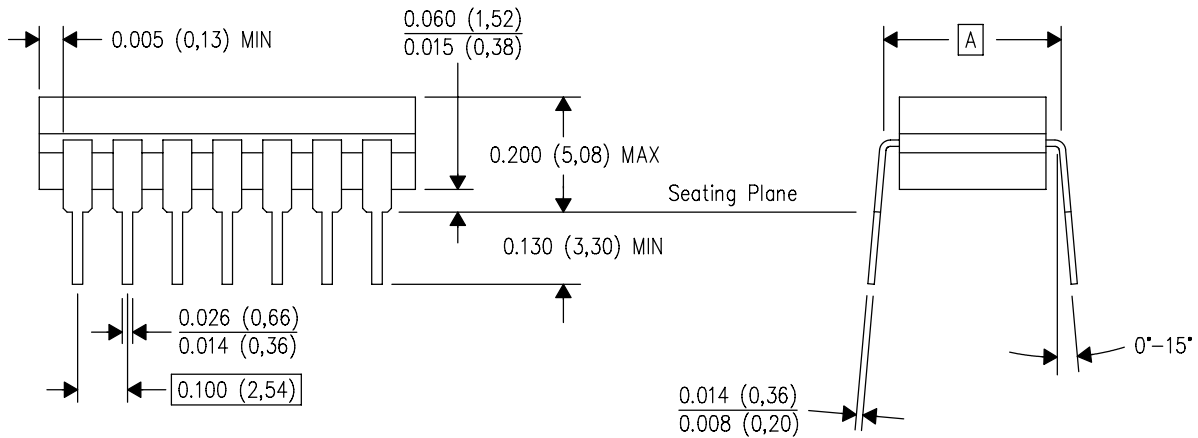
4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package is hermetically sealed with a ceramic lid using glass frit.
          D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E.   Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R–GDFP–F20)   CERAMIC DUAL FLATPACK

Base and Seating Plane

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.300\ (7,62)}{0.245\ (6,22)}$

$\dfrac{0.100\ (2,45)}{0.045\ (1,14)}$

$\dfrac{0.009\ (0,23)}{0.004\ (0,10)}$

0.320 (8,13) MAX

1   20

$\dfrac{0.022\ (0,56)}{0.015\ (0,38)}$

0.540 (13,72) MAX

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

$\dfrac{0.370\ (9,40)}{0.250\ (6,35)}$

$\dfrac{0.370\ (9,40)}{0.250\ (6,35)}$

4040180–4/D 07/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within Mil–Std 1835 GDFP2–F20

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MECHANICAL DATA

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER
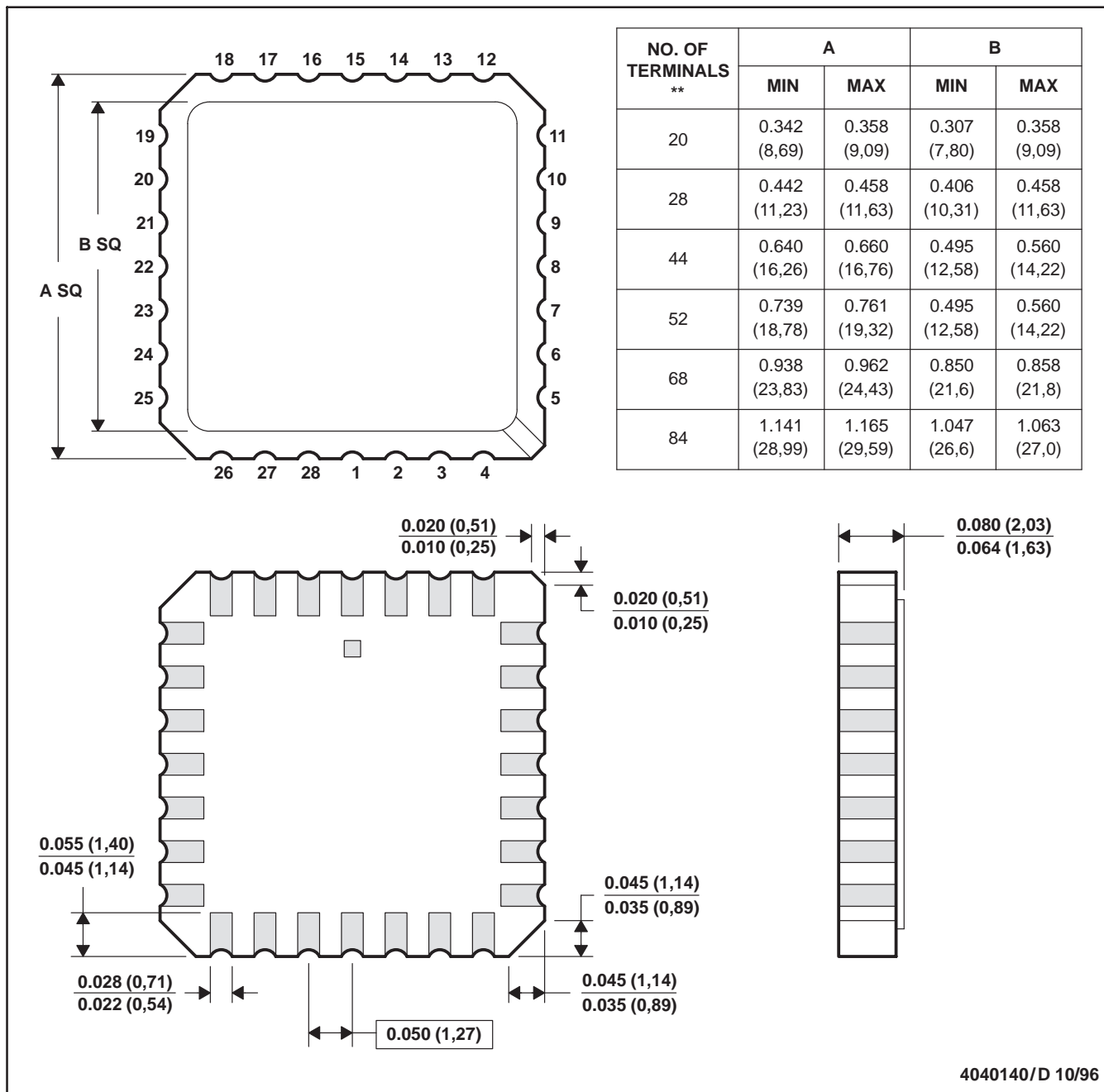
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51)
0.010 (0,25)

0.020 (0,51)
0.010 (0,25)

0.080 (2,03)
0.064 (1,63)

0.055 (1,40)
0.045 (1,14)

0.045 (1,14)
0.035 (0,89)

0.028 (0,71)
0.022 (0,54)

0.045 (1,14)
0.035 (0,89)

0.050 (1,27)

4040140/D 10/96

NOTES: A.   All linear dimensions are in inches (millimeters).
　　　　　B.   This drawing is subject to change without notice.
　　　　　C.   This package can be hermetically sealed with a metal lid.
　　　　　D.   The terminals are gold plated.
　　　　　E.   Falls within JEDEC MS-004

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POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

DIM / PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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DW (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.512 (13,00)
─────────────
0.496 (12,60)

20   11

0.419 (10,63)
─────────────
0.393 (9,97)

0.299 (7,60)
────────────
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
────────────
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
────────────
0.004 (0,10)

0.013 (0,33)
────────────
0.008 (0,20)

△ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
────────────
0.016 (0,40)
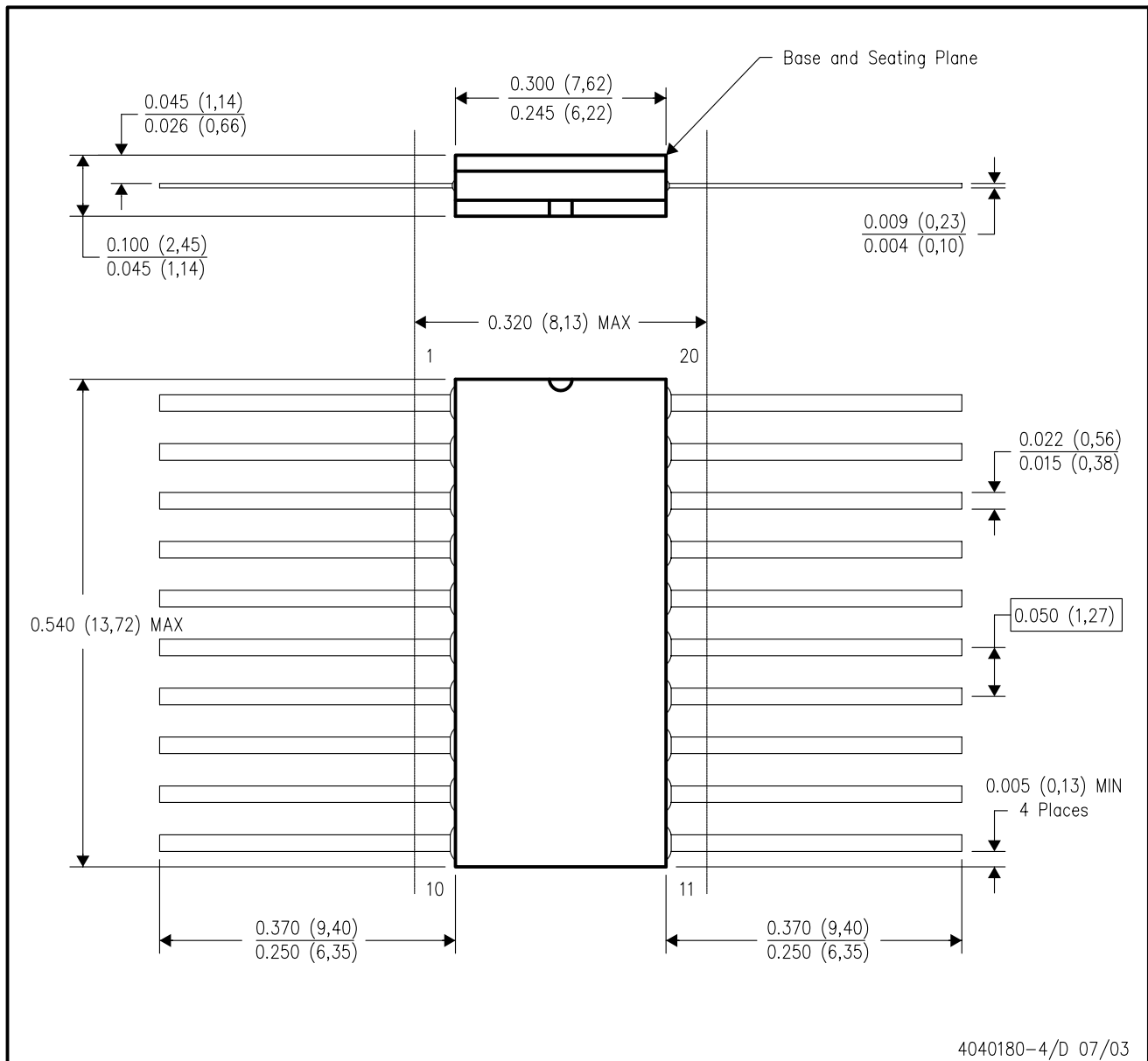
4040000−4/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AC.

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DW (R−PDSO−G20)

Example Board Layout
(Note C)

Stencil Openings
(Note D)

20x0,5   18x1,27

20x0,5   18x1,27

2,2

9,2

9,2

Non Solder Mask Define Pad

0,5

2,2

Solder Mask Opening
(Note E)

Pad Geometry
(Note C)

0,07
All Around
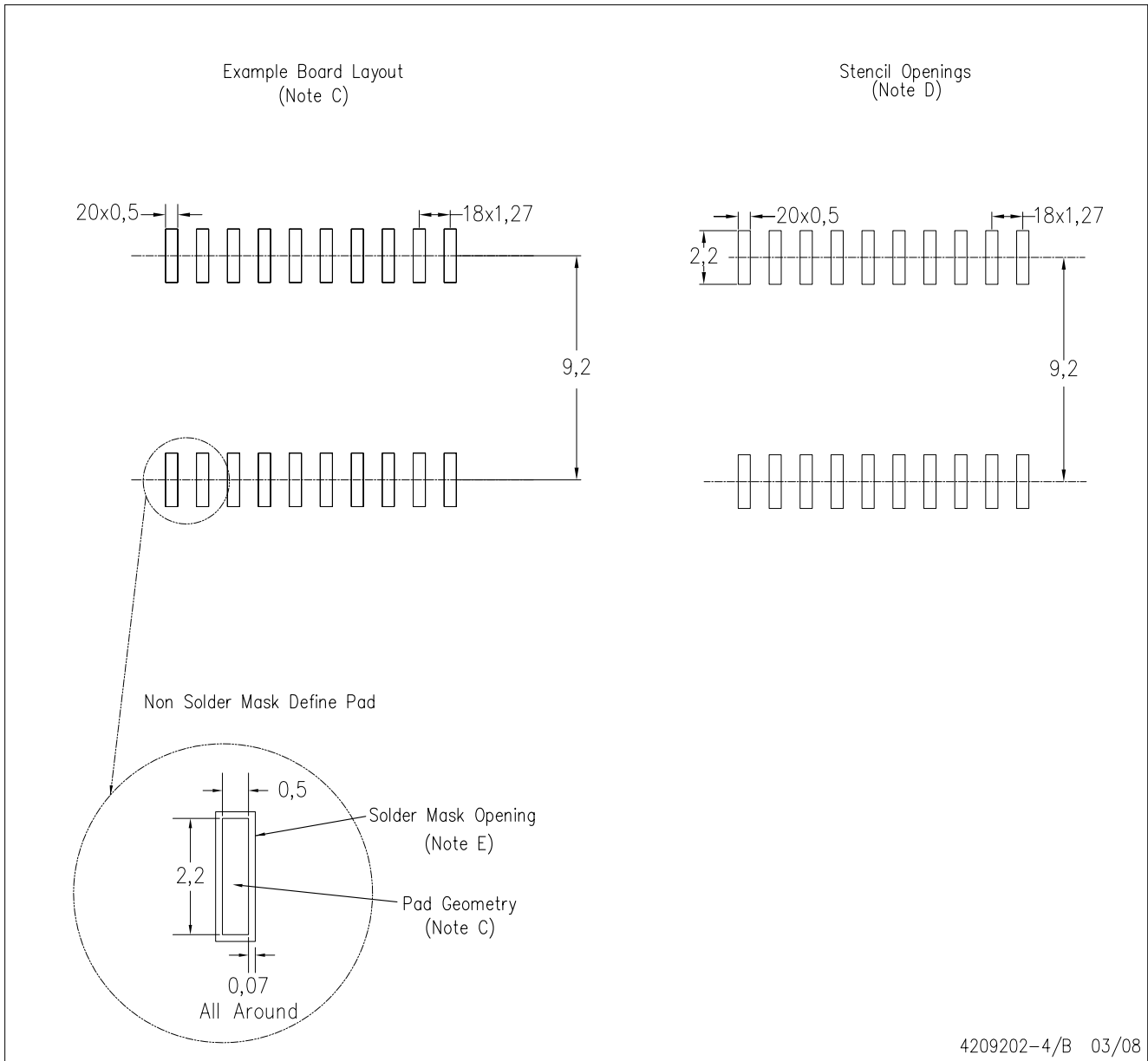
4209202−4/B   03/08

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DBQ (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

20   11

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

Pin 1
Index Area

1   10

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

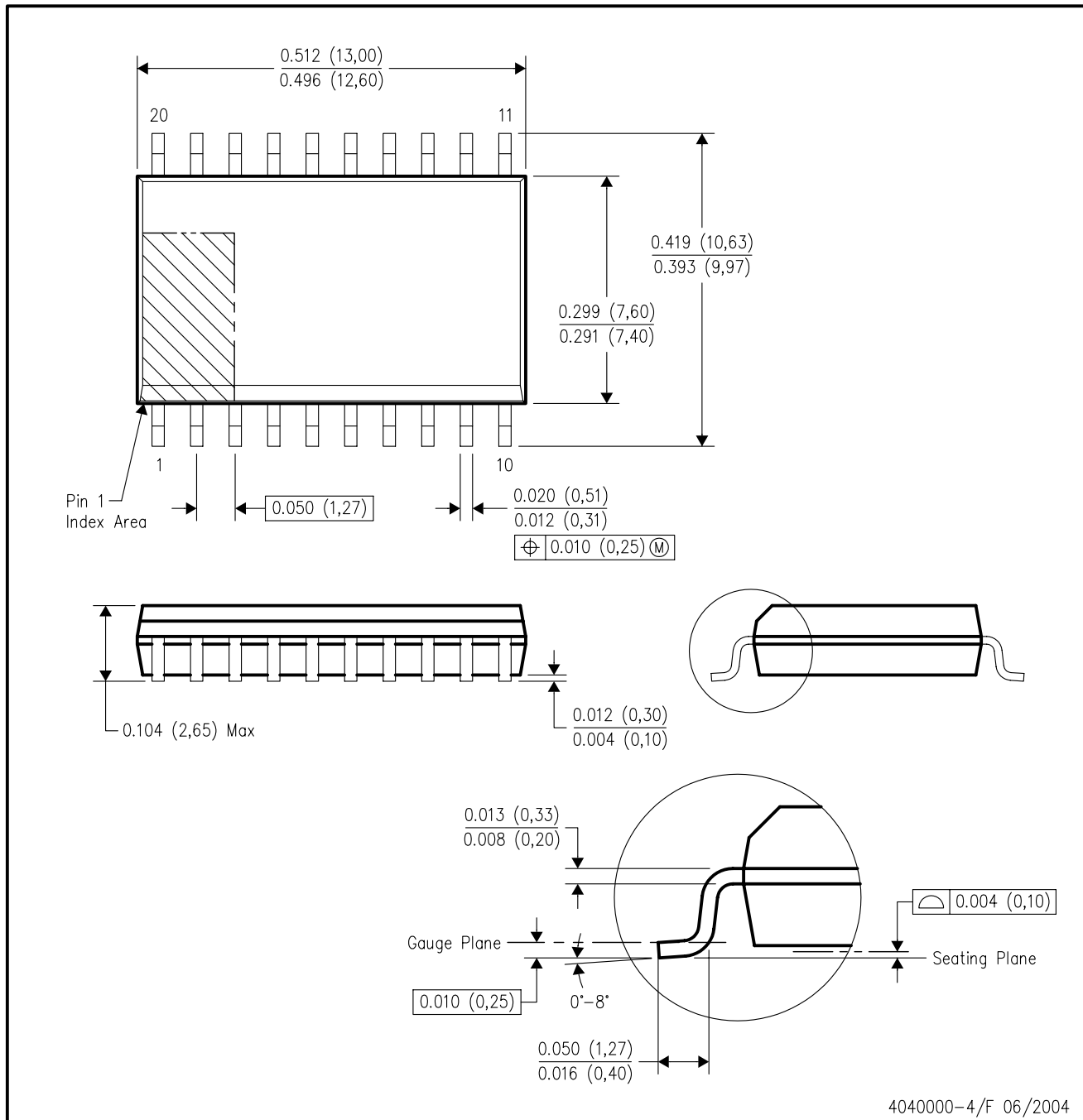0.010 (0,25)

0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−3/H   10/2008

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
         D.   Falls within JEDEC MO−137 variation AD.

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DBQ (R-PDSO-G20)   PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

20x0,35 —| |← |←—18x0,635

5,2

20x0,3 —| |← |←—18x0,635

20x1,75

5,2

0,35

Solder Mask Opening

1,90   1,8

Pad Geometry

0,05

0,40

4210335-3/B 06/10

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
          D.   Publication IPC-7351 is recommended for alternate designs.
          E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
                contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
                metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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