Device Features

BlueCore™4-External

- Fully Qualified Bluetooth v2.0+EDR
- Enhanced Data Rate (EDR) compliant with v2.0.E.2 of specification for both 2Mbps and 3Mbps modulation modes
- Full Speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- 1.8V core, 1.8 to 3.6V I/O
- Low Power 1.8V operation
- 8 x 8mm 96-ball TFBGA and 6 x 6mm 96-ball VFBGA Package options
- Minimum External Components
- Integrated 1.8V Regulator
- USB and Dual UART Ports
- Support for 802.11 Co-Existence
- Support for 8Mbit External Flash
- RoHS Compliant

Single Chip Bluetooth®

v2.0+EDR System

Production Information Data Sheet For

BC417143B-IQN-E4

BC417143B-IRN-E4

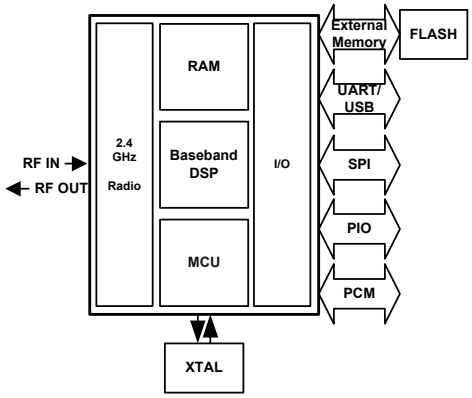
July 2005

BlueCore™4-External Product Data Sheet

General Description

BlueCore™4-External is a single chip radio and baseband IC for Bluetooth 2.4GHz systems including enhanced data rates (EDR) to 3Mbps.

BC417143B interfaces to 8Mbit of external Flash memory. When used with the CSR Bluetooth software stack, it provides a fully compliant Bluetooth system to v2.0 of the specification for data and voice communications..



System Architecture

Applications

- PCs
- Personal Digital Assistants (PDAs)
- Computer Accessories (compact Flash Cards, PCMCIA Cards, SD Cards and USB Dongles)
- Access Points
- Digital Cameras

BlueCore4-External has been designed to reduce the number of external components required which ensures production costs are minimised. The device incorporates auto-calibration and built in self test (BIST) routines to simplify development, type approval and production test.

All hardware and device firmware is fully compliant with the Bluetooth v2.0 + EDR specification (all mandatory and optional features). To improve the performance of both Bluetooth and 802.11b/g co-located systems a wide range of co-existence features are available including two types of hardware signalling: basic activity signalling and Intel WCS activity and channel signalling.

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1 Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Life Support Policy and Use in Safety-Critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

RoHS Compliance

BlueCore4-External devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

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CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

2 Key Features

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time. No external trimming is required in production
- Full RF reference designs available
- Bluetooth v2.0 + EDR Specification compliant

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch
- Supports π/4 DQPSK (2Mbps) and 8DPSK (3Mbps) modulation

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range
- Supports π/4 DQPSK and 8DPSK modulation
- Channel classification

Synthesiser

- Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz) or an external clock
- Accepts 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low Park/Sniff/Hold mode
- Clock request output to control external clock
- On-chip linear regulator; 1.8V output from a 2.2 4.2V input

Auxiliary Features (Continued)

- Can run in low power mode from external 32kHz clock signal
- 8-bit ADC and DAC available to application
- Auto baud rate setting for different TCXO frequencies
- Power-on-reset cell detects low supply voltage
- Arbitrary power supply sequencing permitted
- 8-bit ADC available to applications

Baseband and Software

- External 8Mbit Flash for complete system solution
- Internal 48Kbyte RAM, allows full speed data transfer, mixed voice and data, and full piconet operation, including all medium rate preset types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Supports all Bluetooth v2.0 + EDR features including eSCO and AFH
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbaud for system debugging
- UART interface with programmable baud rate up to 3Mbaud with an optional bypass mode
- Full speed USB v1.1 interface supports OHCI and UHCI host interfaces. Compliant with USB v2.0
- Synchronous bi-directional serial programmable audio interface
- Optional I²C™ compatible interface
- Optional co-existence interfaces

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on-chip in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded to RFCOMM
- Customised builds with embedded application code

Package Options

- 96-ball TFBGA, 8 x 8 x 1.2mm, 0.65mm pitch
- 96-ball VFBGA, 6 x 6 x 1mm, 0.5mm pitch

3 Package Information

3.1 8 x 8mm TFBGA Package Information

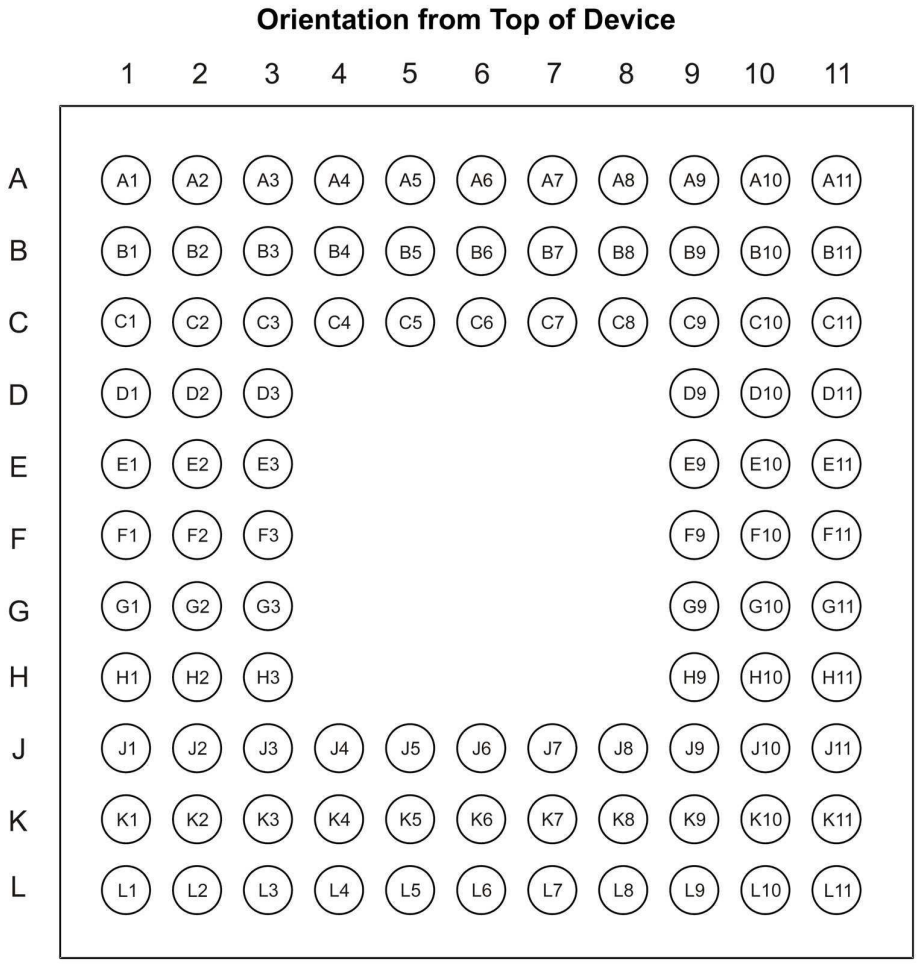


Figure 3.1: BlueCore4-External 8 x 8mm Device Pinout (BC417143B-IQN-E4)

3.2 BC417143B-IQN-E4 Device Terminal Functions

Radio	Ball	Pad Type	Description
PIO[0]/RXEN	B1	Bi-directional with programmable strength internal pull-up/down	Control output for external LNA (if fitted)
PIO[1]/TXEN	B2	Bi-directional with programmable strength internal pull-up/down	Control output for external PA (If fitted)
RX_IN	D1	Analogue	Single ended receiver input
RF_A	F1	Analogue	Transmitter output/switched receiver input
RF_B	E1	Analogue	Complement of RF_A

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L1	Analogue	For crystal or external clock input
XTAL_OUT	L2	Analogue	Drive for crystal

USB and UART	Ball	Pad Type	Description
UART_TX	G9	CMOS output, tri-state, with weak internal pull-up	UART data output
UART_RX	H10	CMOS input with weak internal pull-down	UART data input
UART_RTS	H9	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
UART_CTS	J11	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	K10	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	K11	Bi-directional	USB data minus

PCM Interface	Ball	Pad Type	Description
PCM_OUT	F9	CMOS output, tri-state, with weak internal pull-down	Synchronous data output
PCM_IN	H11	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G11	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	G10	Bi-directional with weak internal pull-down	Synchronous data clock

PIO Port	Ball	Pad Type	Description
PIO[11]	G3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	F3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	E3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	D3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	F10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]/WLAN_Active/ Ch_Data	F11	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or Optionally WLAN_Active/Ch_Data input for co-existence signalling
PIO[5]/BT_Active	E9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or Optionally BT_Active output for co-existence signalling
PIO[4]/ BT_Priority/Ch_Clk	E10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or Optionally BT_Priority/Ch_Clk output for co-existence signalling
PIO[3]	J3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[2]	H3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	K1	Bi-directional	Programmable input/output line
AIO[1]	J2	Bi-directional	Programmable input/output line
AIO[2]	K2	Bi-directional	Programmable input/output line

Test and Debug	Ball	Pad Type	Description
RESETB	B10	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	C11	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	C10	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	D10	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	C9	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	C8	CMOS input with strong internal pull-down	For test purposes only(leave unconnected)

External Memory Address Interface	Ball	Pad Type	Description
A[18]	L7	CMOS output, tri-state	Address line
A[17]	K7	CMOS output, tri-state	Address line
A[16]	A10	CMOS output, tri-state	Address line
A[15]	L10	CMOS output, tri-state	Address line
A[14]	K9	CMOS output, tri-state	Address line
A[13]	J9	CMOS output, tri-state	Address line
A[12]	L9	CMOS output, tri-state	Address line
A[11]	J8	CMOS output, tri-state	Address line
A[10]	K8	CMOS output, tri-state	Address line
A[9]	L8	CMOS output, tri-state	Address line
A[8]	J7	CMOS output, tri-state	Address line
A[7]	J5	CMOS output, tri-state	Address line
A[6]	L6	CMOS output, tri-state	Address line
A[5]	K6	CMOS output, tri-state	Address line
A[4]	K5	CMOS output, tri-state	Address line
A[3]	L5	CMOS output, tri-state	Address line
A[2]	J4	CMOS output, tri-state	Address line
A[1]	K4	CMOS output, tri-state	Address line
A[0]	A3	CMOS output, tri-state	Address line

External Memory Data Interface	Ball	Pad Type	Description
D[15]	B9	Bi-directional with weak internal pull-down	Data line
D[14]	B8	Bi-directional with weak internal pull-down	Data line
D[13]	C7	Bi-directional with weak internal pull-down	Data line
D[12]	A7	Bi-directional with weak internal pull-down	Data line
D[11]	B6	Bi-directional with weak internal pull-down	Data line
D[10]	C5	Bi-directional with weak internal pull-down	Data line
D[9]	A5	Bi-directional with weak internal pull-down	Data line
D[8]	B4	Bi-directional with weak internal pull-down	Data line
D[7]	A9	Bi-directional with weak internal pull-down	Data line
D[6]	A8	Bi-directional with weak internal pull-down	Data line
D[5]	B7	Bi-directional with weak internal pull-down	Data line
D[4]	C6	Bi-directional with weak internal pull-down	Data line
D[3]	A6	Bi-directional with weak internal pull-down	Data line
D[2]	B5	Bi-directional with weak internal pull-down	Data line
D[1]	C4	Bi-directional with weak internal pull-down	Data line
D[0]	A4	Bi-directional with weak internal pull-down	Data line

External Memory Interface	Ball	Pad Type	Description
REB	C3	CMOS output, tri-state with internal weak pull-up	Read enable for external memory. Active low.
WEB	J6	CMOS output, tri-state with internal weak pull-up	Write enable for external memory. Active low.
CSB	B3	CMOS output, tri-state with internal weak pull-up	Chip select for external memory. Active low.

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	L4	VDD/Regulator input	Linear regulator input
VREG_EN	H2	CMOS input	High or not connected to enable regulator. VSS to disable regulator
VDD_USB	L11	VDD	Positive supply for UART/USB ports
VDD_PIO	A2	VDD	Positive supply for PIO[a]
VDD_PADS	D11	VDD	Positive supply for all other digital Input/Output ports[b]
VDD_MEM	A11	VDD	Positive supply for external memory and AIO ports
VDD_CORE	E11	VDD	Positive supply for internal digital circuitry
VDD_RADIO	C1	VDD	Positive supply for RF circuitry
VDD_LO	J1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_ANA	L3	VDD/Regulator output	Positive supply for analogue circuitry and 1.8V regulated output. For performance, regulator decoupling and loads should be connected to ball adjacent to VREG_IN
VSS_DIG	A1, D9, J10	VSS	Ground connection for digital ports
VSS_RADIO	D2, E2, F2	VSS	Ground connections for RF circuitry
VSS_LO	H1	VSS	Ground connections for VCO and synthesiser
VSS_ANA	K3	VSS	Ground connections for analogue circuitry

(a) Positive supply for PIO[3:0] and PIO[11:8]
(b) Positive supply for SPI/PCM ports and PIO[7:4]

Unconnected Terminals	Ball	Description
N/C	B11, C2, G1, G2	Leave unconnected

3.3 6 x 6mm VFBGA Package Information

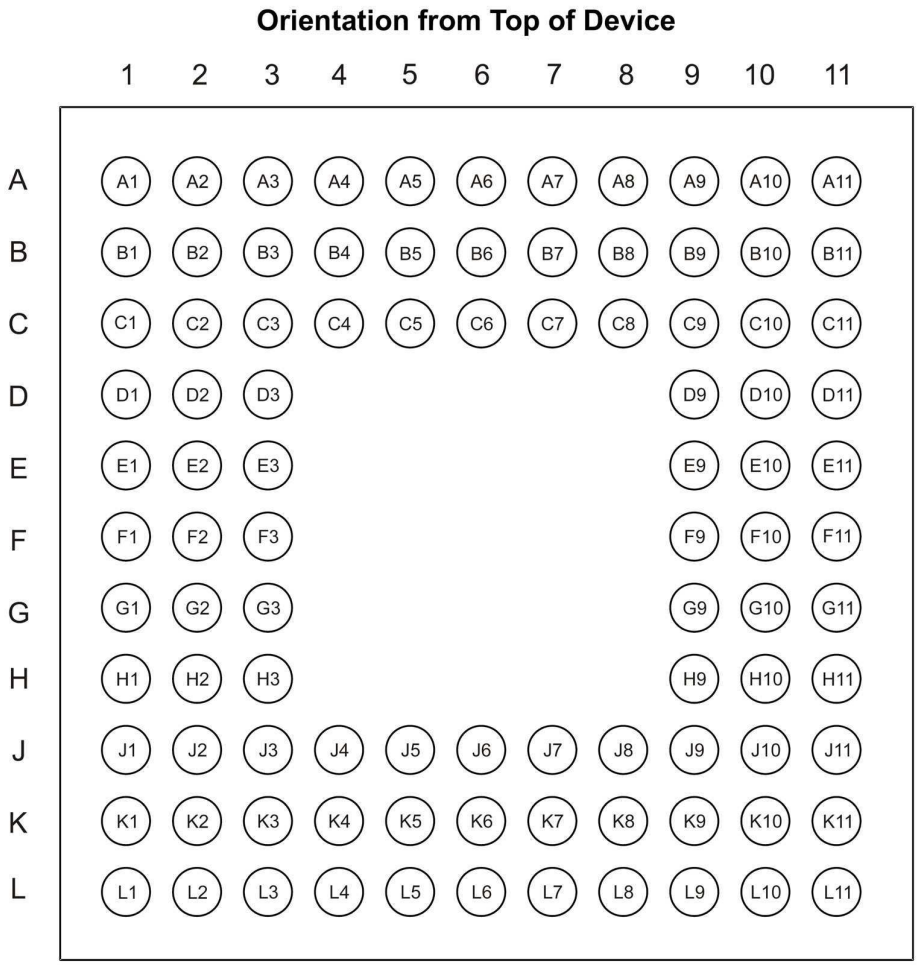


Figure 3.2: BlueCore4-External 6 x 6mm Device Pinout (BC417143B-IRN-E4)

3.4 BC417143B-IRN-E4 Device Terminal Functions

Radio	Ball	Pad Type	Description
PIO[0]/RXEN	C1	Bi-directional with programmable strength internal pull-up/down	Control output for external LNA (if fitted)
PIO[1]/TXEN	C2	Bi-directional with programmable strength internal pull-up/down	Control output for external PA (If fitted)
RX_IN	D1	Analogue	Single ended receiver input
RF_A	F1	Analogue	Transmitter output/switched receiver input
RF_B	E1	Analogue	Complement of RF_A

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L1	Analogue	For crystal or external clock input
XTAL_OUT	L2	Analogue	Drive for crystal

USB and UART	Ball	Pad Type	Description
UART_TX	G9	CMOS output, tri-state, with weak internal pull-up	UART data output
UART_RX	H10	CMOS input with weak internal pull-down	UART data input
UART_RTS	H9	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
UART_CTS	J11	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	K10	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	K11	Bi-directional	USB data minus

PCM Interface	Ball	Pad Type	Description
PCM_OUT	F9	CMOS output, tri-state, with weak internal pull-down	Synchronous data output
PCM_IN	H11	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G11	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	G10	Bi-directional with weak internal pull-down	Synchronous data clock

PIO Port	Ball	Pad Type	Description
PIO[11]	D2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	F3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	G3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	H3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	F10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]/WLAN_Active/ Ch_Data	F11	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or optional WLAN_Active/Ch_Data input for co-existence signalling
PIO[5]/BT_Active	E9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or optional BT_Active output for co-existence signalling
PIO[4]/ BT_Priority/Ch_Clk	E10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or optional BT_Priority/Ch_Clk output for co-existence signalling
PIO[3]	B2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[2]	J3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	L4	Bi-directional	Programmable input/output line
AIO[1]	K3	Bi-directional	Programmable input/output line
AIO[2]	K2	Bi-directional	Programmable input/output line

Test and Debug	Ball	Pad Type	Description
RESETB	D10	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	C11	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface. Active low.
SPI_CLK	B9	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	C10	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	C9	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	C8	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

External Memory Address Interface	Ball	Pad Type	Description
A[18]	L7	CMOS output, tri-state	Address line
A[17]	K7	CMOS output, tri-state	Address line
A[16]	A9	CMOS output, tri-state	Address line
A[15]	L10	CMOS output, tri-state	Address line
A[14]	K9	CMOS output, tri-state	Address line
A[13]	J9	CMOS output, tri-state	Address line
A[12]	L9	CMOS output, tri-state	Address line
A[11]	J8	CMOS output, tri-state	Address line
A[10]	K8	CMOS output, tri-state	Address line
A[9]	L8	CMOS output, tri-state	Address line
A[8]	J7	CMOS output, tri-state	Address line
A[7]	K6	CMOS output, tri-state	Address line
A[6]	L6	CMOS output, tri-state	Address line
A[5]	K5	CMOS output, tri-state	Address line
A[4]	J5	CMOS output, tri-state	Address line
A[3]	L5	CMOS output, tri-state	Address line
A[2]	J4	CMOS output, tri-state	Address line
A[1]	K4	CMOS output, tri-state	Address line
A[0]	A2	CMOS output, tri-state	Address line

External Memory Data Interface	Ball	Pad Type	Description
D[15]	B8	Bi-directional with weak internal pull-down	Data line
D[14]	B7	Bi-directional with weak internal pull-down	Data line
D[13]	C7	Bi-directional with weak internal pull-down	Data line
D[12]	A6	Bi-directional with weak internal pull-down	Data line
D[11]	B5	Bi-directional with weak internal pull-down	Data line
D[10]	C5	Bi-directional with weak internal pull-down	Data line
D[9]	A4	Bi-directional with weak internal pull-down	Data line
D[8]	B3	Bi-directional with weak internal pull-down	Data line
D[7]	A8	Bi-directional with weak internal pull-down	Data line
D[6]	A7	Bi-directional with weak internal pull-down	Data line
D[5]	B6	Bi-directional with weak internal pull-down	Data line
D[4]	C6	Bi-directional with weak internal pull-down	Data line
D[3]	A5	Bi-directional with weak internal pull-down	Data line
D[2]	B4	Bi-directional with weak internal pull-down	Data line
D[1]	C4	Bi-directional with weak internal pull-down	Data line
D[0]	A3	Bi-directional with weak internal pull-down	Data line

External Memory Interface	Ball	Pad Type	Description
REB	C3	CMOS output, tri-state with internal weak pull-up	Read enable for external memory. Active low.
WEB	J6	CMOS output, tri-state with internal weak pull-up	Write enable for external memory. Active low.
CSB	D3	CMOS output, tri-state with internal weak pull-up	Chip select for external memory. Active low.

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	K1	VDD/Regulator input	Linear regulator input
VREG_EN	H2	CMOS input	High or not connected to enable regulator. VSS to disable regulator
VDD_USB	L11	VDD	Positive supply for UART/USB ports
VDD_PIO	A1	VDD	Positive supply for PIO[a]
VDD_PADS	D11	VDD	Positive supply for all other digital Input/Output ports[b]
VDD_MEM	B10	VDD	Positive supply for external memory and AIO ports
VDD_CORE	E11	VDD	Positive supply for internal digital circuitry
VDD_RADIO	G1	VDD	Positive supply for RF circuitry
VDD_LO	J1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_ANA	L3	VDD/Regulator output	Positive supply for analogue circuitry and 1.8V regulated output. For performance, regulator decoupling and loads should be connected to ball adjacent to VREG_IN
VSS_DIG	B1, D9, J10	VSS	Ground connection for digital ports
VSS_RADIO	E2, F2, G2	VSS	Ground connections for RF circuitry
VSS_LO	H1	VSS	Ground connections for VCO and synthesiser
VSS_ANA	J2	VSS	Ground connections for analogue circuitry

(a) Positive supply for PIO[3:0] and PIO[11:8]
(b) Positive supply for SPI/PCM ports and PIO[7:4]

Unconnected Terminals	Ball	Description
N/C	A10, A11, B11, E3	Leave unconnected

4 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Min**	**Max**
Storage temperature	-40°C	+150°C
Supply voltage: VDD_RADIO, VDD_LO, VDD_ANA, and VDD_CORE	-0.4V	2.2V
Supply voltage: VDD_PADS, VDD_PIO and VDD_USB	-0.4V	3.7V
Supply voltage: VREG_IN	-0.4V	5.6V
Other terminal voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Min**	**Max**
Operating temperature range	-40°C	+105°C
Guaranteed RF performance range[a]	-40°C	+105°C
Supply voltage: VDD_RADIO, VDD_LO, VDD_ANA and VDD_CORE	1.7V	1.9V
Supply voltage: VDD_PADS, VDD_PIO and VDD_USB	1.7V	3.6V
Supply voltage: VREG_IN	2.2V	4.2V[b]

(a) Typical figures are given for RF performance between -40°C and +105°C.

(b) The device will operate without damage with VREG_IN as high as 5.6V. However the RF performance is not guaranteed above 4.2V.

Input/Output Terminal Characteristics (Supply)				
Linear Regulator	**Min**	**Typ**	**Max**	**Unit**
Normal Operation				
Output Voltage[a] (I_{load} = 70 mA)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	+250	ppm/°C
Output Noise[b] [c]	-	-	1	mV rms
Load Regulation (I_{load} < 100 mA)	-	-	50	mV/A
Settling Time[b] [d]	-	-	50	µs
Maximum Output Current	140	-	-	mA
Minimum Load Current	5	-	-	µA
Input Voltage	-	-	4.2[e]	V
Dropout Voltage (I_{load} = 70 mA)	-	-	350	mV
Quiescent Current (excluding load, I_{load} < 1mA)	25	35	50	µA
Low Power Mode[f]				
Quiescent Current (excluding load, I_{load} < 100µA)	4	7	10	µA
Disabled Mode[g]				
Quiescent Current	1.5	2.5	3.5	µA

(a) For optimum performance, the VDD_ANA ball adjacent to VREG_IN should be used for regulator output.

(b) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

(c) Frequency range is 100Hz to 100kHz.

(d) 1mA to 70mA pulsed load.

(e) Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore4-External, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.2V.

(f) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.

(g) Regulator is disabled when VREG_EN is pulled low. It is also disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA.

Input/Output Terminal Characteristics (Digital)					
Digital Terminals		**Min**	**Typ**	**Max**	**Unit**
Input Voltage Levels					
V_{IL} input logic level low	2.7V ≤ VDD ≤ 3.0V	-0.4	-	+0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	+0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, (I_o = 4.0mA), 2.7V ≤ VDD ≤ 3.0V		-	-	0.2	V
V_{OL} output logic level low, (I_o = 4.0mA), 1.7V ≤ VDD ≤ 1.9V		-	-	0.4	V
V_{OH} output logic level high, (I_o = -4.0mA), 2.7V ≤ VDD ≤ 3.0V		VDD-0.2	-	-	V
V_{OH} output logic level high, (I_o = -4.0mA), 1.7V ≤ VDD ≤ 1.9V		VDD-0.4	-	-	V
Input and Tri-state Current with:					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		+10	+40	+100	µA
Weak pull-up		-5.0	-1.0	-0.2	µA
Weak pull-down		+0.2	+1.0	+5.0	µA
I/O pad leakage current		-1	0	+1	µA
C_I Input Capacitance		1.0	-	5.0	pF

Input/Output Terminal Characteristics (USB)				
USB Terminals	**Min**	**Typ**	**Max**	**Unit**
VDD_USB for correct USB operation	3.1		3.6	V
Input Threshold				
V_{IL} input logic level low	-	-	0.3VDD_USB	V
V_{IH} input logic level high	0.7VDD_USB	-	-	V
Input Leakage Current				
VSS_PADS < VIN < VDD_USB[(a)]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

(a) Internal USB pull-up disabled

Input/Output Terminal Characteristics (Reset)				
Power-on Reset	**Min**	**Typ**	**Max**	**Unit**
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Input/Output Terminal Characteristics (Auxilliary ADC)					
Auxiliary ADC		**Min**	**Typ**	**Max**	**Unit**
Resolution		-	-	8	Bits
Input voltage range (LSB size = VDD_ANA/255)		0	-	VDD_ANA	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain Error		-0.8	-	0.8	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[a]		-	-	700	Samples/s

(a) ADC is accessed through the VM function. The sample rate given is achieved as part of this function.

Input/Output Terminal Characteristics (Clocks)				
Crystal Oscillator	**Min**	**Typ**	**Max**	**Unit**
Crystal frequency[a]	8.0	-	32.0	MHz
Digital trim range[b]	5.0	6.2	8.0	pF
Trim step size[b]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[c]	870	1500	2400	Ω
External Clock				
Input frequency[d]	7.5	-	40.0	MHz
Clock input level[e]	0.2	-	VDD_ANA	V pk-pk
Allowable Jitter	-	-	15	ps rms
XTAL_IN input impedance	-	-	-	kΩ
XTAL_IN input capacitance	-	7	-	pF

(a) Integer multiple of 250kHz

(b) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

(c) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF.

(d) Clock input can be any frequency between 8MHz and 40MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

(e) Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA. A DC blocking capacitor is required between the signal and XTAL_IN.

4.1 Power Consumption

Operation Mode	Connection Type	UART Rate (kbps)	Average	Unit
Page scan	-	115.2	0.42	mA
Inquiry and page scan	-	115.2	0.76	mA
ACL No traffic	Master	115.2	4.60	mA
ACL With file transfer	Master	115.2	10.3	mA
ACL No traffic	Slave	115.2	17.0	mA
ACL With file transfer	Slave	115.2	24.7	mA
ACL 40ms sniff	Master	38.4	2.40	mA
ACL 1.28s sniff	Master	38.4	0.37	mA
SCO HV1	Master	38.4	39.2	mA
SCO HV3	Master	38.4	20.3	mA
SCO HV3 30ms sniff	Master	38.4	19.8	mA
ACL 40ms sniff	Slave	38.4	2.11	mA
ACL 1.28s sniff	Slave	38.4	0.42	mA
Parked 1.28s beacon	Slave	38.4	0.20	mA
SCO HV1	Slave	38.4	39.1	mA
SCO HV3	Slave	38.4	24.8	mA
SCO HV3 30ms sniff	Slave	38.4	19.0	mA
Standby Host connection[a]	-	38.4	40	µA
Reset (RESETB low)[a]	-	-	34	µA

[a] Low power mode on the linear regulator is entered and exited automatically when the chip enters/leaves Deep Sleep mode. For more information about the electrical characteristics of the linear regulator, see section 4 in this document.

Typical Peak Current @ 20ºC	
Device Activity/State	**Current m(A)**
Peak current during cold boot	57.9
Peak TX current Master	51.5
Peak RX current Master	39.0
Peak TX current Slave	52.0
Peak RX current Slave	45.5
Conditions	
Firmware	HCI 19.2
VREG_IN, VDD_PIO, VDD_PADS	3.15V
Host Interface	UART
Baud rate	115200
Clock source	26MHz crystal
Output power	0dBm

5 Radio Characteristics - Basic Data Rate

Important Note:

BlueCore4-External meets the Bluetooth v2.0+EDR specification when used in a suitable application circuit between -40°C and +105°C. TX output is guaranteed unconditionally stable over guaranteed temperature range.

5.1 Temperature +20°C

5.1.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = +20°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a] [b]	-	5	-	-6 to +4[c]	dBm
RF power variation over temperature range with compensation enabled(±)[d]	-	1.5	-	-	dB
RF power variation over temperature range with compensation disabled(±)[d]	-	2	-	-	dB
RF power control range	25	35	-	≥16	dB
RF power range control resolution[e]	-	0.5	1.2	-	dB
20dB bandwidth for modulated carrier	-	790	1000	≤1000	kHz
Adjacent channel transmit power F = F_0 ± 2MHz[f] [g]	-	-35	-20	≤-20	dBm
Adjacent channel transmit power F = F_0 ± 3MHz[f] [g]	-	-45	-40	≤-40	dBm
Adjacent channel transmit power F = F_0 ± > 3MHz[f] [g]	-	-50	-40	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	140	163	175	140<$f1_{avg}$<175	kHz
$\Delta f2_{max}$ Minimum Modulation	115	154	-	115	kHz
$\Delta f1_{avg}/\Delta f2_{avg}$	0.80	0.98	-	≥0.80	-
Initial carrier frequency tolerance	-75	6	75	≤75	kHz
Drift Rate	-	7	20	≤20	kHz/50µs
Drift (single slot packet)	-	8	25	≤25	kHz
Drift (five slot packet)	-	9	40	≤40	kHz
2nd Harmonic Content	-	-60	-30	≤-30	dBm
3rd Harmonic Content	-	-45	-40	≤-30	dBm

(a) The BlueCore4-External firmware maintains the transmit power within Bluetooth v2.0+EDR specification limits

(b) Measurement using PSKEY_LC_MAX_TX_POWER setting corresponding to a PSKEY_LC_POWER_TABLE power table entry = 63

(c) Class 2 RF transmit power range, Bluetooth specification v2.0+EDR

(d) These parameters are dependent on matching circuit used, and its behaviour over temperature, therefore these parameters are not under CSR's direct control

(e) Resolution guaranteed over the range -5dB to -25dB relative to maximum power for Tx Level > 20

(f) Measured at F_0 = 2441MHz

(g) BlueCore4-External guaranteed to meet ACP performance in Bluetooth v2.0+EDR specification, three exceptions allowed.

Radio Characteristics	VDD = 1.8V	Temperature = +20°C				
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Cellular Band**	**Unit**
Emitted power in cellular bands measured at unbalanced port of the balun. Output power ≤6dBm	0.869 - 0.894[a]	-	-124	-	GSM 850	dBm / Hz
	0.869 - 0.894[b]	-	-128	-	CDMA 850	
	0.925 - 0.960[a]	-	-128	-	GSM 900	
	1.570 - 1.580[c]	-	-138	-	GPS	
	1.805 - 1.880[a]	-	-133	-	GSM 1800 / DCS 1800	
	1.930 - 1.990[d]	-	-135	-	PCS 1900	
	1.930 - 1.990[a]	-	-134	-	GSM 1900	
	1.930 - 1.990[b]	-	-134	-	CDMA 1900	
	2.110 - 2.170[b]	-	-136	-	W-CDMA 2000	
	2.110 - 2.170[e]	-	-139	-	W-CDMA 2000	

(a) Integrated in 200kHz bandwidth and then normalised to 1Hz bandwidth
(b) Integrated in 1.2MHz bandwidth and then normalised to 1Hz bandwidth
(c) Integrated in 1MHz bandwidth and then normalised to 1Hz bandwidth
(d) Integrated in 30kHz bandwidth and then normalised to 1Hz bandwidth
(e) Integrated in 5MHz bandwidth and then normalised to 1Hz bandwidth

5.1.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = +20°C		
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-85.0	-	≤-70	dBm
	2.441	-	-85.0	-		
	2.480	-	-87.0	-		
Maximum received signal at 0.1% BER		-20	10	-	≥-20	dBm
	Frequency (MHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Continuous power required to block Bluetooth reception (for input power of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	30-2000	-10	0	-	≥-10	dBm
	2000-2400	-27	0	-	≥-27	
	2500-3000	-27	0	-	≥-27	
C/I co-channel		-	6	11	≤11	dB
Adjacent channel selectivity C/I $F = F_0 + 1MHz$ [a] [b]		-	-5	0	≤0	dB
Adjacent channel selectivity C/I $F = F_0 - 1MHz$ [a] [b]		-	-4	0	≤0	dB
Adjacent channel selectivity C/I $F = F_0 + 2MHz$ [a] [b]		-	-44	-30	≤-30	dB
Adjacent channel selectivity C/I $F = F_0 - 2MHz$ [a] [b]		-	-23	-20	≤-20	dB
Adjacent channel selectivity C/I $F = F_0 + 3MHz$ [a] [b]		-	-45	-40	≤-40	dB
Adjacent channel selectivity C/I $F = F_0 - 5MHz$ [a] [b]		-	-45	-40	≤-40	dB
Adjacent channel selectivity C/I $F = F_{Image}$ [a] [b]		-	-22	-9	≤-9	dB
Maximum level of intermodulation interferers[c]		-39	-30	-	≥-39	dBm
Spurious output level[d]		-	-150	-	-	dBm/Hz

(a) Up to five exceptions are allowed in v2.0+EDR of the Bluetooth specification. BlueCore4-External is guaranteed to meet the C/I performance as specified by the Bluetooth specification v2.0+EDR.

(b) Measured at F = 2441MHz

(c) Measured at f1 - f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c., i.e., wanted signal at -64dBm.

(d) Measured at unbalanced port of the balun. Integrated in 100kHz bandwidth and normalised to 1Hz. Actual figure is typically below -150dBm/Hz except for peaks of -70dbm at 1600MHz, -60dBm inband at 2.4GHz and -70dBm at 3.2GHz.

Radio Characteristics	VDD = 1.8V	Temperature = +20°C				
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Cellular Band**	**Unit**
Continuous power in cellular bands required to block Bluetooth reception (for input power of -67dBm with 0.1% BER) measured at unbalanced port of the balun.	0.824 - 0.849	-	0	-	GSM 850	dBm
	0.824 - 0.849	-	-10	-	CDMA 850	
	0.880 - 0.915	-	-5	-	GSM 900	
	1.710 - 1.785	-	0	-	GSM 1800 / DCS 1800	
	1.850 - 1.910	-	0	-	GSM 1900 / PCS 1900	
	1.850 - 1.910	-	-7	-	CDMA 1900	
	1.920 - 1.980	-	-10	-	W-CDMA 2000	
Continuous power in cellular bands required to block Bluetooth reception (for input power of -72dBm with 0.1% BER) measured at unbalanced port of the balun.	0.824 - 0.849	-	-2	-	GSM 850	dBm
	0.824 - 0.849	-	-12	-	CDMA 850	
	0.880 - 0.915	-	-7	-	GSM 900	
	1.710 - 1.785	-	0	-	GSM 1800 / DCS 1800	
	1.850 - 1.910	-	0	-	GSM 1900 / PCS 1900	
	1.850 - 1.910	-	-12	-	CDMA 1900	
	1.920 - 1.980	-	-14	-	W-CDMA 2000	

5.2 Temperature -40°C

5.2.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = -40°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]	-	6	-	-6 to +4[b]	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	1000	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[c] [d]	-	-35	-20	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$[c] [d]	-	-45	-40	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	140	163	175	$140<\Delta f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	115	152	-	115	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	0.80	0.97	-	≥0.80	-
Initial carrier frequency tolerance	-75	6	75	≤75	kHz
Drift Rate	-	7	20	≤20	kHz/50µs
Drift (single slot packet)	-	8	25	≤25	kHz
Drift (five slot packet)	-	9	40	≤40	kHz

(a) BlueCore4-External firmware maintains the transmit power to be within the Bluetooth v2.0+EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measured at F_0 = 2441MHz
(d) Three exceptions are allowed in Bluetooth v2.0+EDR specification

5.2.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = -40°C		
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-87.0	-	≤-70	dBm
	2.441	-	-87.0	-		
	2.480	-	-89.0	-		
Maximum received signal at 0.1% BER		-20	10	-	≥-20	dBm

5.3 Temperature -25°C

5.3.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = -25°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]	-	5.8	-	-6 to +4[b]	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	1000	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[c] [d]	-	-35	-20	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$[c] [d]	-	-45	-40	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	140	163	175	$140<\Delta f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	115	154	-	115	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	0.80	0.98	-	≥0.80	-
Initial carrier frequency tolerance	-75	6	75	≤75	kHz
Drift Rate	-	7	20	≤20	kHz/50µs
Drift (single slot packet)	-	8	25	≤25	kHz
Drift (five slot packet)	-	9	40	≤40	kHz

(a) BlueCore4-External firmware maintains the transmit power to be within the Bluetooth v2.0+EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measured at F_0 = 2441MHz
(d) Three exceptions are allowed in Bluetooth v2.0+EDR specification.

5.3.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = -25°C		
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-86.5	-	≤-70	dBm
	2.441	-	-86.5	-		
	2.480	-	-88.0	-		
Maximum received signal at 0.1% BER		-20	10	-	≥-20	dBm

5.4 Temperature +85°C

5.4.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = +85°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]	-	3	-	-6 to +4[b]	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	1000	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[c] [d]	-	-40	-20	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$[c] [d]	-	-45	-40	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	140	163	175	$140<\Delta f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	115	150	-	115	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	0.80	0.97	-	≥0.80	-
Initial carrier frequency tolerance	-75	6	75	≤75	kHz
Drift Rate	-	7	20	≤20	kHz/50µs
Drift (single slot packet)	-	8	25	≤25	kHz
Drift (five slot packet)	-	9	40	≤40	kHz

(a) BlueCore4-External firmware maintains the transmit power to be within the Bluetooth v2.0+EDR specification limits.
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measured at F_0 = 2441MHz
(d) Three exceptions are allowed in Bluetooth v2.0+EDR specification

5.4.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = +85°C		
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-82.5	-	≤-70	dBm
	2.441	-	-82.0	-		
	2.480	-	-84.0	-		
Maximum received signal at 0.1% BER		-20	10	-	≥-20	dBm

5.5 Temperature +105°C

5.5.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = +105°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]	-	1.5	-	-6 to +4[b]	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	1000	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[c] [d]	-	-40	-20	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$[c] [d]	-	-45	-40	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	140	163	175	$140<\Delta f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	115	148	-	115	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	0.80	0.97	-	≥0.80	-
Initial carrier frequency tolerance	-75	12	75	≤75	kHz
Drift Rate	-	7	20	≤20	kHz/50µs
Drift (single slot packet)	-	8	25	≤25	kHz
Drift (five slot packet)	-	9	40	≤40	kHz

(a) BlueCore4-External firmware maintains the transmit power to be within the Bluetooth v2.0+EDR specification limits.
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measured at F_0 = 2441MHz
(d) Three exceptions are allowed in the Bluetooth v2.0+EDR specification

5.5.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = +105°C		
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-81.5	-	≤-70	dBm
	2.441	-	-81.0	-		
	2.480	-	-83.0	-		
Maximum received signal at 0.1% BER		-20	10	-	≥-20	dBm

6 Radio Characteristics - Enhanced Data Rate

Important Note:

Results shown are referenced to the unbalanced port of the balun.

6.1 Temperature +20°C

6.1.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +20°C						
		Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power[a]		-	1.5	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1.2	-	-4 to +1	dB
π/4 DQPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] w_i		-	6	-	≤±75 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] $\lvert w_0 + w_i \rvert$		-	8	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_i		-	6	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] $\lvert w_0 + w_i \rvert$		-	8	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy[c] [d]	RMS DEVM	-	7	-	≤20	%
	99% DEVM	-	13	-	≤30	%
	Peak DEVM	-	19	-	≤35	%
8DPSK Modulation Accuracy[c] [d]	RMS DEVM	-	7	-	≤13	%
	99% DEVM	-	13	-	≤20	%
	Peak DEVM	-	17	-	≤25	%
In-band spurious emissions[e]	$F>F_0$ +3MHz	-	<-50	-	≤-40	dBm
	$F<F_0$ -3MHz	-	<-50	-	≤-40	dBm
	$F=F_0$ -3MHz	-	-46	-	≤-40	dBm
	$F=F_0$ -2MHz	-	-34	-	≤-20	dBm
	$F=F_0$ -1MHz	-	-35	-	≤-26	dB
	$F=F_0$ +1MHz	-	-35	-	≤-26	dB
	$F=F_0$ +2MHz	-	-31	-	≤-20	dBm
	$F=F_0$ +3MHz[e]	-	-33	-	≤-40	dBm
EDR Differential Phase Encoding		99	No Errors	-	≥99	%

(a) BlueCore4-External firmware maintains transmit power within Bluetooth v2.0+EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measurements methods are in accordance with the EDR RF Test Specification v2.0.e.2
(d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the frequency drift.
(e) Bluetooth specification values are for 8DPSK. Three exceptions are allowed in Bluetooth v2.0+EDR specification.

6.1.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = +20°C				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER[a]	π/4 DQPSK	-	-87		≤-70	dBm
	8DPSK	-	-78		≤-70	dBm
Maximum received signal at 0.1% BER[a]	π/4 DQPSK	-	-8	-	≥-20	dBm
	8DPSK	-	-10	-	≥-20	dBm
C/I co-channel at 0.1% BER[a]	π/4 DQPSK	-	10	-	≤+13	dB
	8DPSK	-	19	-	≤+21	dB
Adjacent channel selectivity C/I $F=F_0+1MHz$[a] [b] [c]	π/4 DQPSK	-	-10	-	≤0	dB
	8DPSK	-	-5	-	≤+5	dB
Adjacent channel selectivity C/I $F=F_0-1MHz$ [a] [b] [c]	π/4 DQPSK	-	-11	-	≤0	dB
	8DPSK	-	-5	-	≤+5	dB
Adjacent channel selectivity C/I $F=F_0+2MHz$[a] [b] [c]	π/4 DQPSK	-	-40	-	≤-30	dB
	8DPSK	-	-40	-	≤-25	dB
Adjacent channel selectivity C/I $F=F_0-2MHz$[a] [b] [c]	π/4 DQPSK	-	-23	-	≤-20	dB
	8DPSK	-	-20	-	≤-13	dB
Adjacent channel selectivity C/I $F\geq F_0+3MHz$[a] [b] [c]	π/4 DQPSK	-	-45	-	≤-40	dB
	8DPSK	-	-45	-	≤-33	dB
Adjacent channel selectivity C/I $F\leq F_0-5MHz$[a] [b] [c]	π/4 DQPSK	-	-45	-	≤-40	dB
	8DPSK	-	-45	-	≤-33	dB
Adjacent channel selectivity C/I $F=F_{Image}$[a] [b] [c]	π/4 DQPSK	-	-20	-	≤-7	dB
	8DPSK	-	-15	-	≤0	dB

(a) Measurements methods are in accordance with the EDR RF Test Specification v2.0.e.2

(b) Up to five exceptions are allowed in EDR RF Test Specification v2.0.e.2. BlueCore4-External is guaranteed to meet the C/I performance as specified by the EDR RF Test Specification v2.0.e.2.

(c) Measured at F0 = 2405MHz, 2441MHz, 2477MHz

6.2 Temperature -40°C

6.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]		-	4	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1.2	-	-4 to +1	dB
π/4 DQPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] $\| w_0+w_i \|$		-	8	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_0		-	3	-	≤±10 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] $\| w_0+ w_i \|$		-	9	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy[c] [d]	RMS DEVM	-	7	-	≤20	%
	99% DEVM	-	14	-	≤30	%
	Peak DEVM	-	19	-	≤35	%
8DPSK Modulation Accuracy[c] [d]	RMS DEVM	-	6	-	≤13	%
	99% DEVM	-	12	-	≤20	%
	Peak DEVM	-	18	-	≤25	%
In-band spurious emissions[e]	$F>F_0+3MHz$	-	<-50	-	≤-40	dBm
	$F<F_0-3MHz$	-	<-50	-	≤-40	dBm
	$F=F_0-3MHz$	-	-42	-	≤-40	dBm
	$F=F_0-2MHz$	-	-25	-	≤-20	dBm
	$F=F_0-1MHz$	-	-32	-	≤-26	dB
	$F=F_0+1MHz$	-	-33	-	≤-26	dB
	$F=F_0+2MHz$	-	-25	-	≤-20	dBm
	$F=F_0+3MHz$[e]	-	-30	-	≤-40	dBm
EDR Differential Phase Encoding		99	No Errors	-	≥99	%

(a) BlueCore4-External firmware maintains transmit power within Bluetooth v2.0+EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measurements methods are in accordance with the EDR RF Test Specification v2.0.e.2
(d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the frequency drift.
(e) The Bluetooth specification values are for 8DPSK. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification.

6.2.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = -40°C				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER(a)	π/4 DQPSK	-	-85	-	≤-70	dBm
	8DPSK	-	-78	-	≤-70	dBm
Maximum received signal at 0.1% BER(a)	π/4 DQPSK	-	-12	-	≤-20	dBm
	8DPSK	-	-15	-	≤-20	dBm

(a) Measurements methods are in accordance with the EDR RF Test Specification v2.0.e.2

6.3 Temperature -25°C

6.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]		-	3	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1.2	-	-4 to +1	dB
π/4 DQPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] w_i		-	6	-	≤±75 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] $\| w_0+w_i \|$		-	8	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_i		-	6	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] $\| w_0+ w_i \|$		-	8	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy[c] [d]	RMS DEVM	-	6	-	≤20	%
	99% DEVM	-	13	-	≤30	%
	Peak DEVM	-	16	-	≤35	%
8DPSK Modulation Accuracy[c] [d]	RMS DEVM	-	6	-	≤13	%
	99% DEVM	-	11	-	≤20	%
	Peak DEVM	-	16	-	≤25	%
In-band spurious emissions[e]	$F>F_0+3MHz$	-	<-50	-	≤-40	dBm
	$F<F_0-3MHz$	-	<-50	-	≤-40	dBm
	$F=F_0-3MHz$	-	-43	-	≤-40	dBm
	$F=F_0-2MHz$	-	-29	-	≤-20	dBm
	$F=F_0-1MHz$	-	-32	-	≤-26	dB
	$F=F_0+1MHz$	-	-33	-	≤-26	dB
	$F=F_0+2MHz$	-	-27	-	≤-20	dBm
	$F=F_0+3MHz$[e]	-	-31	-	≤-40	dBm
EDR Differential Phase Encoding		99	No Errors	-	≥99	%

(a) BlueCore4-External firmware maintains transmit power within Bluetooth v2.0+EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measurements methods are in accordance with the EDR RF Test Specification v2.0.e.2
(d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the frequency drift.
(e) The Bluetooth specification values are for 8DPSK. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification.

6.3.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = -25°C				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER(a)	π/4 DQPSK	-	-85	-	≤-70	dBm
	8DPSK	-	-78	-	≤-70	dBm
Maximum received signal at 0.1% BER(a)	π/4 DQPSK	-	-12	-	≤-20	dBm
	8DPSK	-	-15	-	≤20	dBm

(a) Measurements methods are in accordance with the EDR RF Test Specification v2.0.e.2

6.4 Temperature +85°C

6.4.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +85°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]		-	-2	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1.2	-	-4 to +1	dB
π/4 DQPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] $\| w_0+w_i \|$		-	9	-	≤±75 for all blocks	kHZ
8DPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHZ
8DPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHZ
8DPSK max carrier frequency stability[c] $\| w_0+ w_i \|$		-	9	-	≤±75 for all blocks	kHZ
π/4 DQPSK Modulation Accuracy[c] [d]	RMS DEVM	-	6	-	≤20	%
	99% DEVM	-	13	-	≤30	%
	Peak DEVM	-	16	-	≤35	%
8DPSK Modulation Accuracy[c] [d]	RMS DEVM	-	6	-	≤13	%
	99% DEVM	-	11	-	≤20	%
	Peak DEVM	-	16	-	≤25	%
In-band spurious emissions[e]	$F>F_0+3MHz$	-	<-50	-	≤-40	dBm
	$F<F_0-3MHz$	-	<-50	-	≤-40	dBm
	$F=F_0-3MHz$	-	-43	-	≤-40	dBm
	$F=F_0-2MHz$	-	-29	-	≤-20	dBm
	$F=F_0-1MHz$	-	-32	-	≤-26	dB
	$F=F_0+1MHz$	-	-33	-	≤-26	dB
	$F=F_0+2MHz$	-	-27	-	≤-20	dBm
	$F=F_0+3MHz$[e]	-	-31	-	≤-40	dBm
EDR Differential Phase Encoding		99	No Errors	-	≥99	%

(a) BlueCore4-External firmware maintains transmit power within Bluetooth v2.0+EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measurements methods are in accordance with the EDR RF Test Specification v2.0.e.2
(d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the frequency drift.
(e) The Bluetooth specification values are for 8DPSK. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification.

6.4.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = +85°C				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER(a)	π/4 DQPSK	-	-83	-	≤-70	dBm
	8DPSK	-	-75	-	≤-70	dBm
Maximum received signal at 0.1% BER(a)	π/4 DQPSK	-	-5	-	≤-20	dBm
	8DPSK	-	-5	-	≤-20	dBm

(a) Measurements methods are in accordance with the EDR RF Test Specification v2.0.e.2

6.5 Temperature +105°C

6.5.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +105°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]		-	-3	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1.3	-	-4 to +1	dB
π/4 DQPSK max carrier frequency stability[c] w_0		-	1	-	≤±10 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] $\| w_0+w_i \|$		-	8	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_0		-	1	-	≤±10 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] $\| w_0+ w_i \|$		-	8	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy[c] [d]	RMS DEVM	-	7	-	≤20	%
	99% DEVM	-	12	-	≤30	%
	Peak DEVM	-	16	-	≤35	%
8DPSK Modulation Accuracy[c] [d]	RMS DEVM	-	7	-	≤13	%
	99% DEVM	-	12	-	≤20	%
	Peak DEVM	-	15	-	≤25	%
In-band spurious emissions[e]	$F>F_0+3MHz$	-	<-50	-	≤-40	dBm
	$F<F_0-3MHz$	-	<-50	-	≤-40	dBm
	$F=F_0-3MHz$	-	-51	-	≤-40	dBm
	$F=F_0-2MHz$	-	-45	-	≤-20	dBm
	$F=F_0-1MHz$	-	-37	-	≤-26	dB
	$F=F_0+1MHz$	-	-32	-	≤-26	dB
	$F=F_0+2MHz$	-	-37	-	≤-20	dBm
	$F=F_0+3MHz$[e]	-	-38	-	≤-40	dBm
EDR Differential Phase Encoding		99	No Errors	-	≥99	%

(a) BlueCore4-External firmware maintains transmit power within Bluetooth v2.0+EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measurements methods are in accordance with the EDR RF Test Specification v2.0.e.2
(d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the frequency drift.
(e) The Bluetooth specification values are for 8DPSK. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification.

6.5.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = +105°C				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER(a)	π/4 DQPSK	-	-85	-	≤-70	dBm
	8DPSK	-	-73	-	≤-70	dBm
Maximum received signal at 0.1% BER(a)	π/4 DQPSK	-	-5	-	≤-20	dBm
	8DPSK	-	-5	-	≤-20	dBm

(a) Measurements methods are in accordance with the EDR RF Test Specification v2.0.e.2

7 Device Diagram

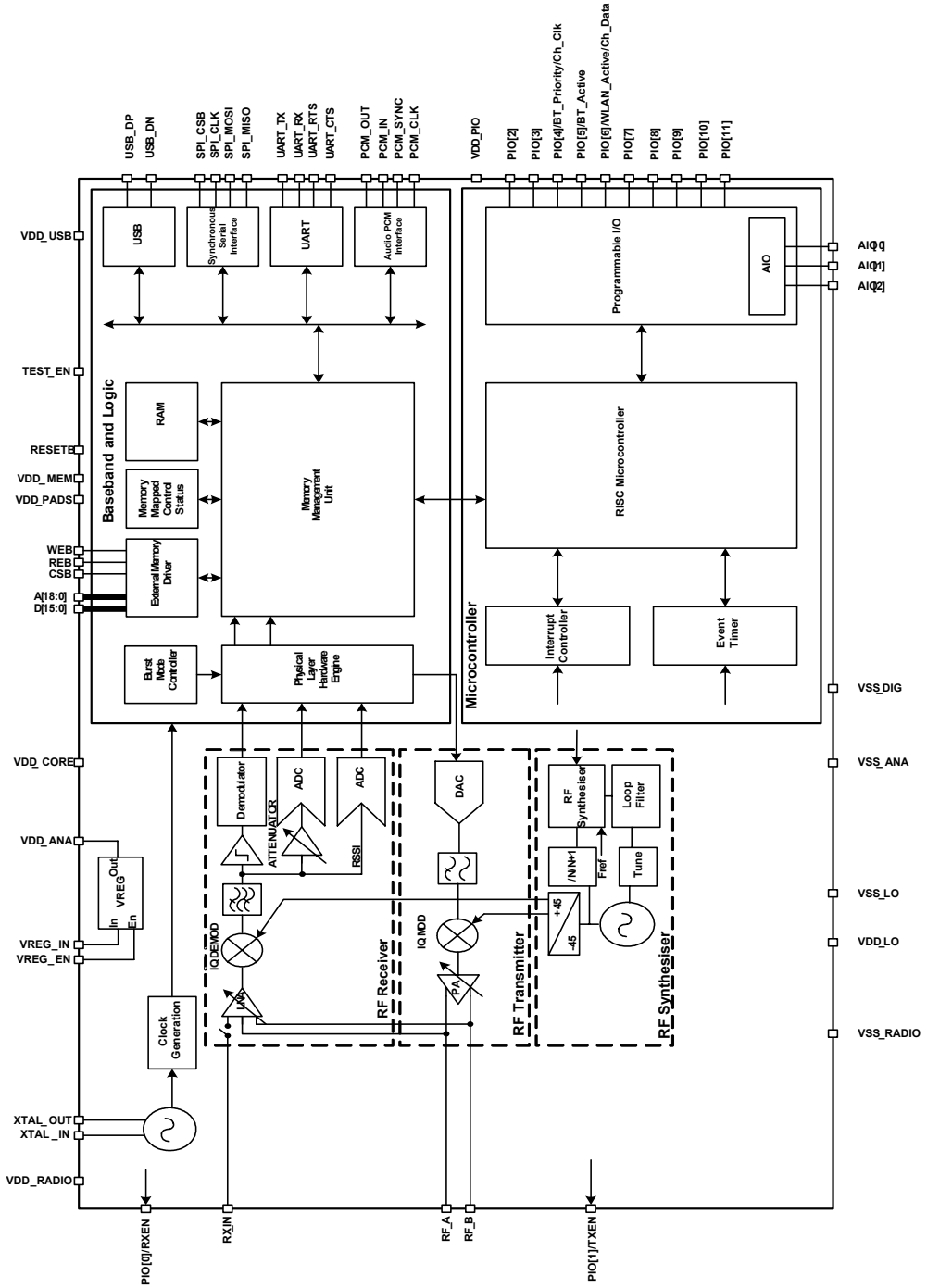


Figure 7.1: BlueCore4-External Device Diagram

8 Description of Functional Blocks

8.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore4-External to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, an ADC is used to digitise the IF received signal.

8.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation; differential mode is used for Class 2 operation.

8.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

8.2 RF Transmitter

8.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

8.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm. This allows BlueCore4-External to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

8.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.0 + EDR specification.

8.4 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8MHz and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

8.5 Baseband and Logic

8.5.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

8.5.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

8.5.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware suports all optional and mandatory features of Bluetooth v2.0 + EDR including AFH and eSCO.

8.5.4 RAM (48Kbytes)

48Kbytes of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

8.5.5 External Memory Driver

The External Memory Driver interface can be used to connect to the external Flash memory and also to the optional external RAM for memory intensive applications.

8.5.6 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore4-External acts as a USB peripheral, responding to requests from a master host controller such as a PC.

8.5.7 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory.

8.5.8 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

8.6 Microcontroller

The microcontroller (MCU), interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

8.6.1 Programmable I/O

BlueCore4-External has a total of 15 (12 digital and 3 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

8.6.2 802.11 Co-Existence Interface

Dedicated hardware is provided to implement a variety of co-existence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware. The details of some methods are proprietary (e.g., Intel WCS). Contact CSR for details.

9 CSR Bluetooth Software Stacks

BlueCore4-External is supplied with Bluetooth v2.0 + EDR compliant stack firmware, which runs on the internal RISC microcontroller.

The BlueCore4-External software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

9.1 BlueCore HCI Stack

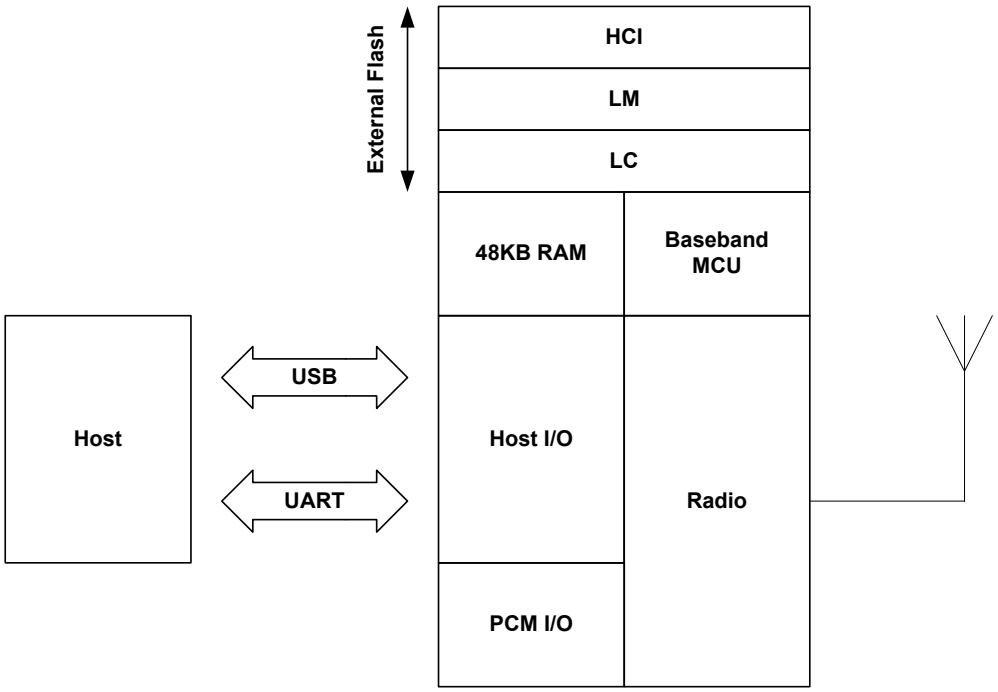


Figure 9.1: BlueCore HCI Stack

In the implementation shown in Figure 9.1 the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). The Host processor must provide all upper layers including the application.

9.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

Bluetooth v2.0 + EDR mandatory functionality:

- Adaptive frequency hopping (AFH), including classifier
- Faster connection - enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

Optional Bluetooth v2.0 + EDR functionality supported:

- Adaptive Frequency Hopping (AFH) as Master and Automatic Channel Classification
- Fast Connect - Interlaced Inquiry and Page Scan plus RSSI during Inquiry
- Extended SCO (eSCO), eV3 +CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.0 + EDR specification.

- Bluetooth components:
  - Baseband (including LC)
  - LM
  - HCI
- Standard USB v1.1 and UART HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps(1)
- Operation with up to seven active slaves(1)
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to three SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from www.csr.com.

(1) This is the maximum allowed by Bluetooth v2.0 + EDR specification.

(2) BlueCore4-External supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.0 + EDR specification.

9.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP), a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BlueCore Command (BCCMD), provides:
  - Access to the chip's general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code
- A block of BCCMD commands provides access to the chip's Persistent Store configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART break condition can be used in three ways:
  1. Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  2. Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
  3. With BCSP, the firmware can be configured to send a break to the host before sending data. (This is normally used to wake the host from a Deep Sleep state.)
- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules
- A modified version of the DFU protocol allows firmware upgrade via the chip's UART
- A block of radio test or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and RFCOMM builds (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LEDs via the chip's PIO port.
- Hardware low power modes: Shallow Sleep and Deep Sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the chip's single PCM port (at the same time as routing any remaining SCO channels over HCI).

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

9.2 BlueCore RFCOMM Stack

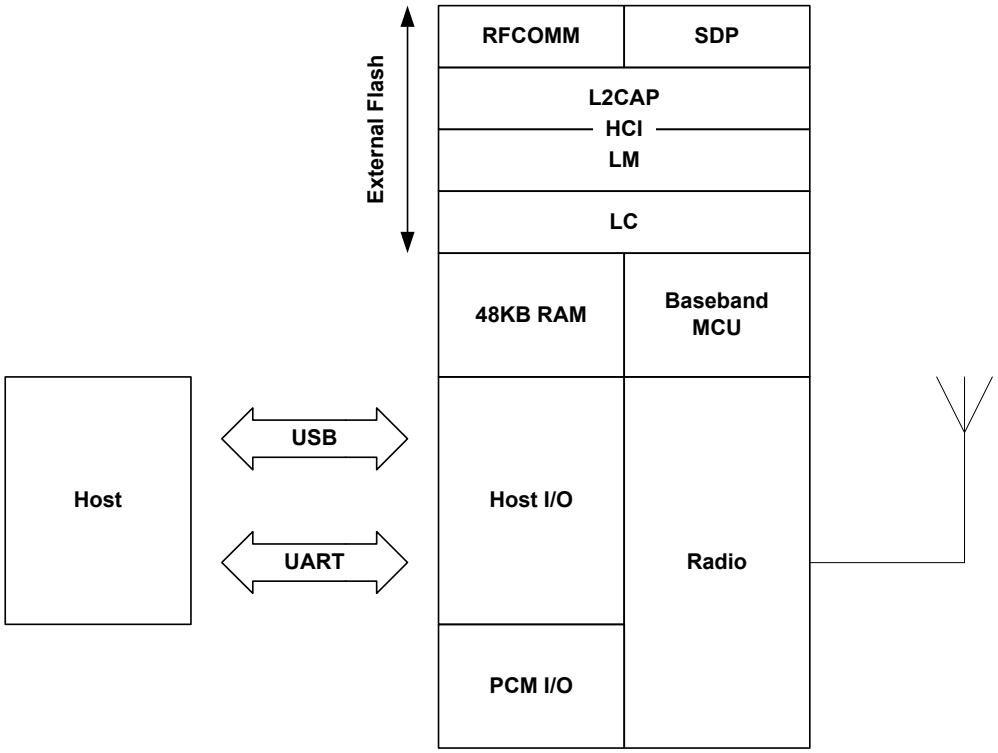


Figure 9.2: BlueCore RFCOMM Stack

In the version of the firmware, shown in Figure 9.2 the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

9.2.1 Key Features of the BlueCore4-External RFCOMM Stack

Interfaces to Host:

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity:

- Maximum number of active slaves: three
- Maximum number of simultaneous active ACL connections: three
- Maximum number of simultaneous active SCO connections: three
- Data Rate: up to 350kbps(1)

Security:

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving:

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity:

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimise interference to other radio devices using the ISM band.

(1) The data rate is with respect to BlueCore4-External with basic data rate packets.

9.3 BlueCore Virtual Machine Stack

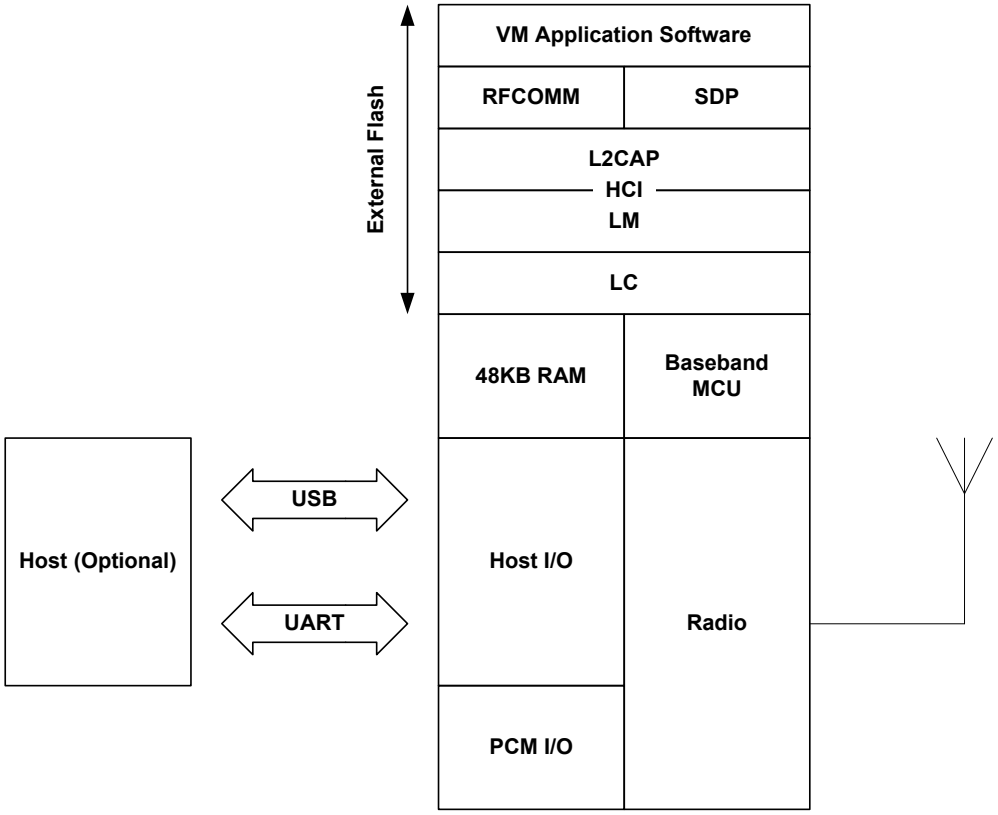


Figure 9.3: Virtual Machine

In Figure 9.3, this version of the stack firmware shown requires no host processor (but it can use a host processor for debugging, etc.). All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab SDK supplied with the BlueLab Multimedia and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless handsfree kit or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the handsfree profile.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

9.4 BlueCore HID Stack

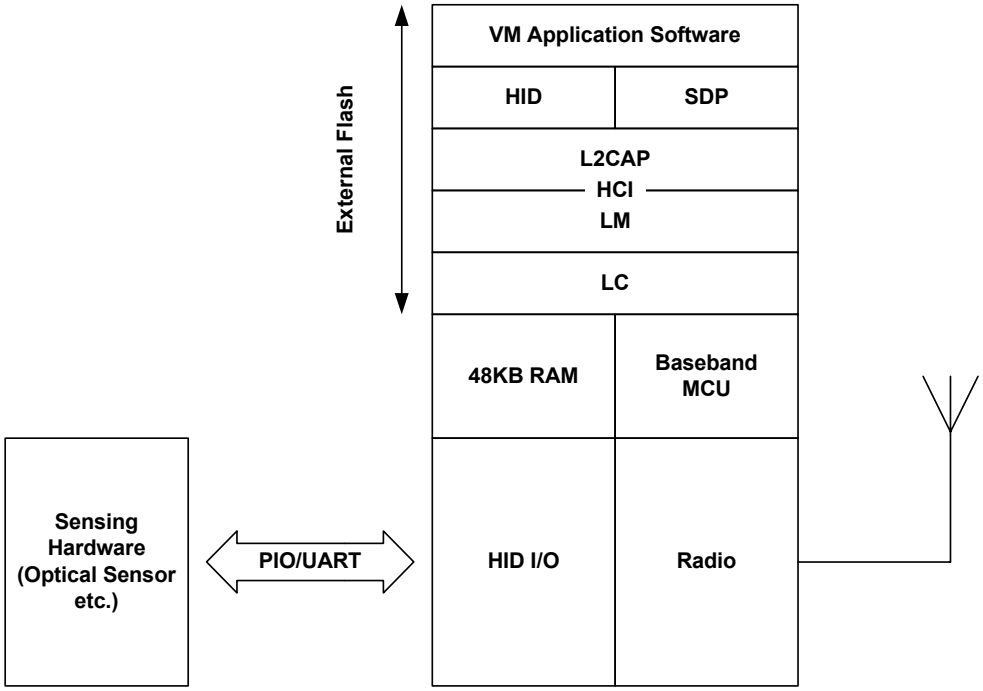


Figure 9.4: HID Stack

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC microcontroller in a protected user software execution environment known as a virtual machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab Professional SDK supplied with the BlueLab Professional and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab Professional SDK the user is able to develop Bluetooth HID devices such as an optical mouse or keyboard. The user is able to customise features such as power management and connect/reconnect behaviour.

The HID I/O component in the HID stack controls low latency data acquisition from external sensor hardware. With this component running in native code, it does not incur the overhead of the VM code interpreter. Supported external sensors include five mouse buttons, the Agilent ADNS-2030 optical sensor, quadrature scroll wheel, direct coupling to a keyboard matrix and a UART interface to custom hardware.

A reference schematic for implementing a three button, optical mouse with scroll wheel is available from CSR.

9.5 BCHS Software

BlueCore Embedded Host Software is designed to enable CSR customers to implement Bluetooth functionality into embedded products quickly, cheaply and with low risk.

BCHS is developed to work with CSR's family of BlueCore ICs. BCHS is intended for embedded products that have a host processor for running BCHS and the Bluetooth application, e.g., a mobile phone or a PDA. BCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP, RFCOMM and SDP) is a complete Bluetooth system solution from RF to profiles.

BCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.

The BlueCore Embedded Host Software contains three elements:

- Example Drivers (BCSP and proxies)
- Bluetooth Profile Managers
- Example Applications

The profiles are qualified which makes the qualification of the final product very easy. BCHS is delivered with source code (ANSI C). BCHS also comes with example applications in ANSI C, which makes the process of writing the application easier.

9.6 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore4-External, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery Protocol (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as C source or object code.

9.7 CSR Development Systems

CSR's BlueLab Multimedia and Casira development kits are available to allow the evaluation of the BlueCore4-External hardware and software, and as toolkits for developing on-chip and host software.

10 Enhanced Data Rate

EDR has been introduced to provide 2x and 3x[1] data rates with minimal disruption to higher layers of the Bluetooth stack. BlueCore4-External supports both of the new data rates and is compliant with the Bluetooth v2.0+EDR specification.

10.1 Enhanced Data Rate Baseband

At the baseband level EDR utilises both the same 1.6kHz slot rate and the 1MHz symbol rate as defined for the basic data rate. Where EDR differs is that each symbol in the payload portion of a packet represents 2 or 3-bits. This is achieved using two new distinct modulation schemes. These are summarised in Table 10.1 and in Figure 10.1. Link Establishment and management are unchanged and still use GFSK for both the header and payload portions of these packets.

Data Rate Scheme	Bits Per Symbol	Modulation
Basic Data Rate	1	GFSK
EDR	2	π/4 DQPSK
EDR	3	8DPSK (optional)

Table 10.1: Data Rate Schemes

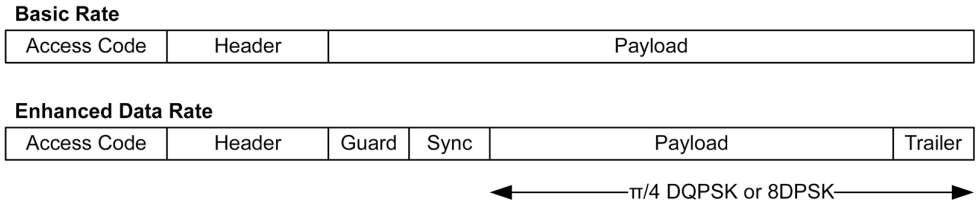


Figure 10.1: Basic Rate and Enhanced Data Rate Packet Structure

10.2 Enhanced Data Rate π/4 DQPSK

The 2x data rate for EDR utilises a π/4-DQPSK. Each symbol represents two bits of information. Figure 10.2 shows the constellation. It is described as having two planes, each having four points. Although it would appear that there are eight possible phase states, the encoding ensures that the trajectory of the modulation between symbols is restricted to the four states in the other plane.

For a given starting point, each phase change between symbols is restricted to +3π/4, +π/4, -π/4 or -3π/4 radians (+135°, +45°, -135° or -45°). For example, the arrows shown in Figure 10.2 represents trajectory to the four possible states in the other plane.Table 10.2 shows the phase shift encoding of symbols.

There are two primary advantages of utilising π/4-DQPSK modulation:

- The scheme avoids the crossing of the origin (a +π or -π phase shift) and therefore minimises amplitude variations in the envelope of the transmitted signal. This in turn allows the RF power amplifiers of the transmitter to be operated closer to their compression point without introducing spectral distortions. Consequently, the DC to RF efficiency is maximised.
- The differential encoding also allows for the demodulation without the knowledge of an absolute value for the phase of the RF carrier.

(1) The inclusion of 3x data rates is optional.

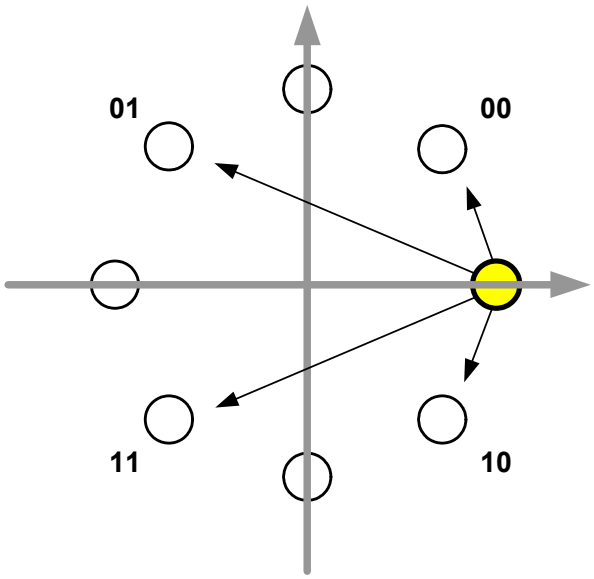


Figure 10.2: π/4 DQPSK Constellation Pattern

Bit Pattern	Phase Shift
00	π/4
01	3π/4
11	-3π/4
10	-π/4

Table 10.2: 2-Bits Determine Phase Shift Between Consecutive Symbols

10.3 Enhanced Data Rate 8DPSK

The 3x data rate modulation uses eight phase differential phase shift keying (8DPSK). Each symbol in the payload portion of the packet represents three baseband bits. Although it would appear that the 8DPSK is similar to π/4 DQPSK, the differential phase shifts between symbols are now permissible between any of the eight possible phase states. This reduces the separation between adjacent symbols on the constellation to π/4 (45°) and thereby reduces the noise and interference immunity of the modulation scheme. Nevertheless, since each symbol now represents 3 baseband bits, the actual throughput of the data is 3x when compared with the basic rate packet.

Figure 10.3 illustrates the 8DPSK constellation and Table 10.3 defines the phase encoding.

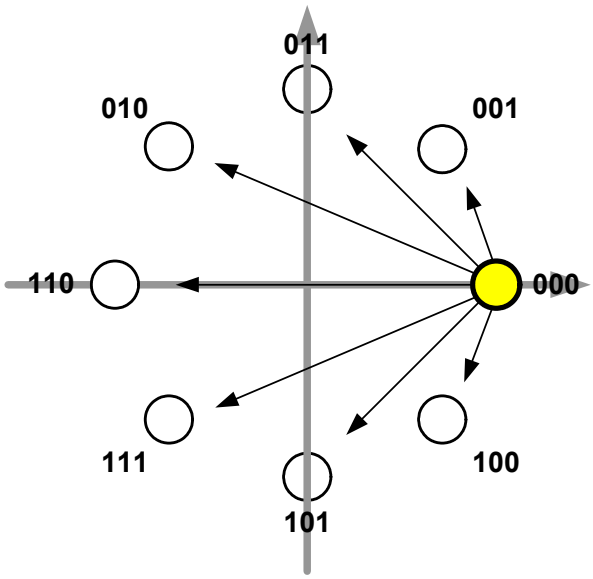


Figure 10.3: 8DPSK Constellation Pattern

Bit Pattern	Phase Shift
000	0
001	π/4
011	π/2
010	3π/4
110	π
111	-3π/4
101	-π/2
100	-π/4

Table 10.3: 3-Bits Determine Phase Shift Between Consecutive Symbols

11 Device Terminal Descriptions

11.1 RF Ports

The BlueCore4-External RF_IN terminal can be configured as either a single-ended or differential input. The operational mode is determined by setting the PS Key PSKEY_TXRX_PIO_CONTROL (0x20).

11.1.1 RF_A and RF_B

RF_A and RF_B form a complementary balanced pair. On transmit their outputs are combined using a balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally. Both terminals present similar complex impedances that require matching networks between them and the balun. Starting from the substrate (chip side), the outputs can each be modelled as an ideal current source in parallel with a lossy resistance and a capacitor. The bond wire can be represented as series inductance.

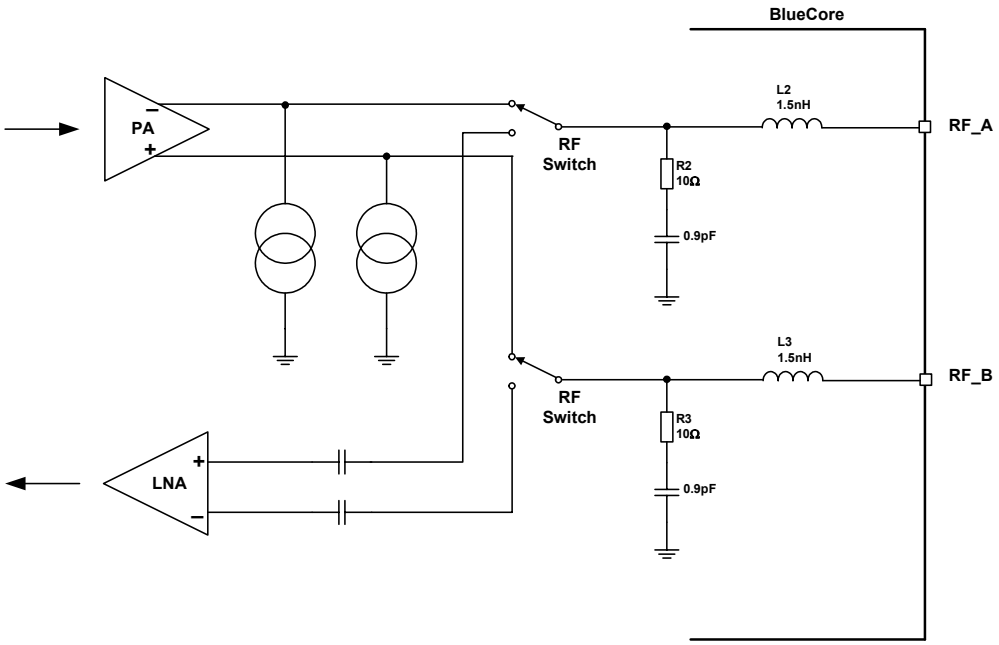


Figure 11.1: Circuit TX/RF_A and TX/RF_B

11.1.2 Single-Ended Input (RX_IN)

This is the single-ended RF input from the antenna. The input presents a complex impedance that requires a matching network between the terminal and the antenna. Starting from the substrate (chip) side, the input can be modelled as a lossy capacitor with the bond wire to the ball grid represented as a series inductance.

The terminal is DC blocked. The DC level must not exceed (VSS_RADIO -0.3V to VDD_RADIO + 0.3V).

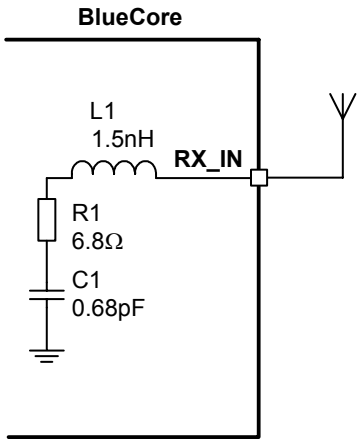


Figure 11.2: Circuit RX_IN

Note:

Both terminals must be externally DC biased to VDD_RADIO

11.1.3 Transmit RF Power Control for Class 1 Applications (TX_PWR)

An 8-bit voltage DAC (AUX_DAC) is used to control the amplification level of the external PA for Class 1 operation. The DAC output is derived from the on-chip band gap and is virtually independent of temperature and supply voltage. The output voltage is given by:

$$V_{DAC} = MIN\left(\left(3.3v \times \frac{CNTRL\_WORD}{255}\right), (VDD\_PIO - 0.3v)\right)$$

Equation 11.1: Output Voltage with Load Current ≤ 10mA

for a load current ≤10mA (sourced from the device).

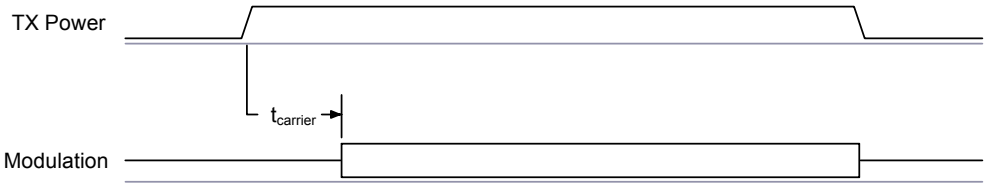
or

$$V_{DAC} = MIN\left(\left(3.3v \times \frac{CNTRL\_WORD}{255}\right), VDD\_PIO\right)$$

Equation 11.2: Output Voltage with No Load Current

for no load current.

BlueCore4-External enables the external PA only when transmitting. Before transmitting, the chip normally ramps up the power to the internal PA, then it ramps it down again afterwards. However, if a suitable external PA is used, it may be possible to ramp the power externally by driving the TX_PWR pin on the PA from AUX_DAC.



Equation 11.3: Internal Power Ramping

The Persistent Store Key (PS Key) PSKEY_TX_GAINRAMP (0x1d), is used to control the delay (in units of μs) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which gives the transmit circuitry time to fully settle to the correct frequency.

Bits[15:8] define a delay, tcarrier, (in units of μs) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which aids interoperability with some other vendor equipment which is not strictly Bluetooth compliant.

11.1.4 Control of External RF Components

A PS Key TXRX_PIO_CONTROL (0x209) is used to control external RF components such as a switch, an external PA or an external LNA. PIO[0], PIO[1] and the AUX_DAC can be used for this purpose, as Table 11.1 indicates.

TXRX_PIO_CONTROL Value	AUX_DAC Use
0	PIO[0], PIO[1], AUX_DAC not used to control RF. Power ramping is internal.
1	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC not used. Power ramping is internal.
2	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
3	PIO[0] is low during RX, PIO[1] is low during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
4	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is internal.

Table 11.1: TXRX_PIO_CONTROL Values

11.2 External Reference Clock Input (XTAL_IN)

The BlueCore4-External RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore4-External XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The crystal mode is described in section 11.3.

11.2.1 External Mode

BlueCore4-External can be configured to accept an external reference clock from another device (such as TCXO) at XTAL_IN by connecting XTAL_OUT to ground. The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (approximately 33pF) connected to XTAL_IN. A digital level reference clock gives superior noise immunity, as the high slew rate clock edges have lower voltage to phase conversion.

The external clock signal should meet the specifications in Table 11.2:

	Min	Typ	Max
Frequency[a]	7.5MHz	16MHz	40MHz
Duty cycle	20:80	50:50	80:20
Edge Jitter (At Zero Crossing)	-	-	15ps rms
Signal Level	400mV pk-pk	-	VDD_ANA[b] [c]

Table 11.2: External Clock Specifications

(a) The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

(b) VDD_ANA is 1.8V nominal

(c) If the external clock is driven through a DC blocking capacitor, then maximum allowable amplitude is reduced from VDD_ANA to 800mV pk-pk.

11.2.2 XTAL_IN Impedance in External Mode

The impedance of the XTAL_IN will not change significantly between operating modes, typically 10fF. When transitioning from Deep Sleep to an active state a spike of up to 1pC may be measured. For this reason it is recommended that a buffered clock input be used.

11.2.3 Clock Timing Accuracy

As Figure 11.3 indicates, the 250ppm timing accuracy on the external clock is required 7ms after the assertion of the system clock request line. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v2.0 + EDR specification. Radio activity may occur after 11ms, therefore, at this point the timing accuracy of the external clock source must be within 20ppm.

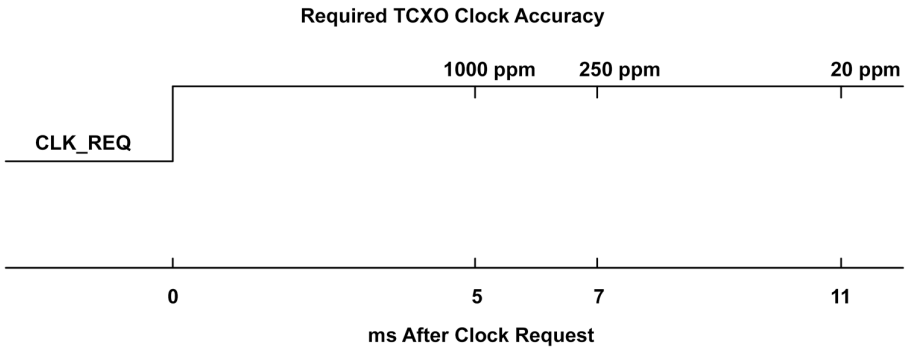


Figure 11.3: TCXO Clock Accuracy

11.2.4 Clock Start-Up Delay

BlueCore4-External hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore4-External firmware provides a software function which will extend the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 5-31ms.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore4-External as low as possible. BlueCore4-External will consume about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

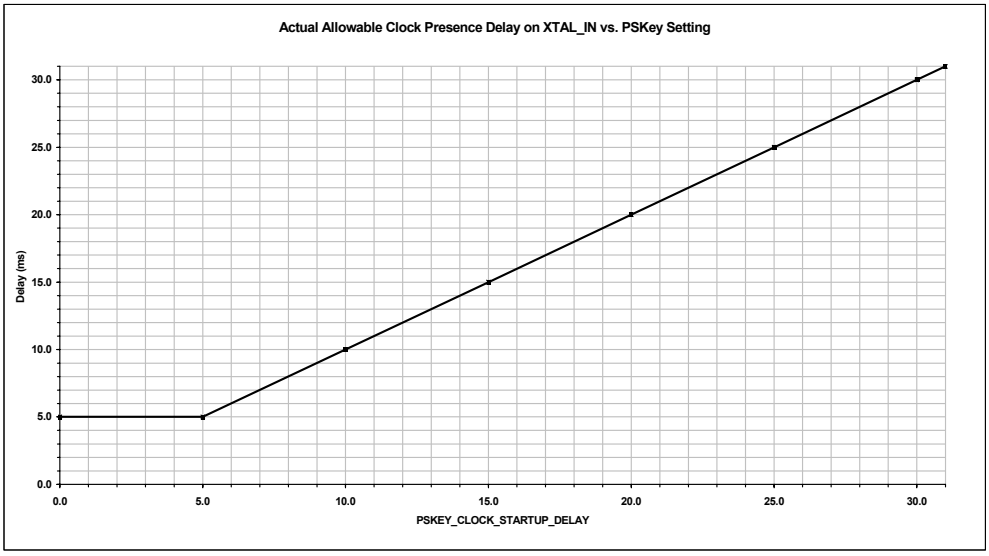


Figure 11.4: Actual Allowable Clock Presence Delay on XTAL_IN vs. PS Key Setting

11.2.5 Input Frequencies and PS Key Settings

BlueCore4-External should be configured to operate with the chosen reference frequency. This is accomplished by setting the PS Key PSKEY_ANA_FREQ (0x1fe) for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore4-External is 26MHz.

The following CDMA/3G TCXO frequencies are also catered for: 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (0x1fe) (Units of 1kHz)
7.68	7680
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 250kHz	-
+26.00 Default	26000

Table 11.3: PS Key Values for CDMA/3G Phone TCXO Frequencies

11.3 Crystal Oscillator (XTAL_IN, XTAL_OUT)

This section describes the crystal mode. See section 11.2 for the description of the external reference clock mode.

11.3.1 XTAL Mode

BlueCore4-External contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator.

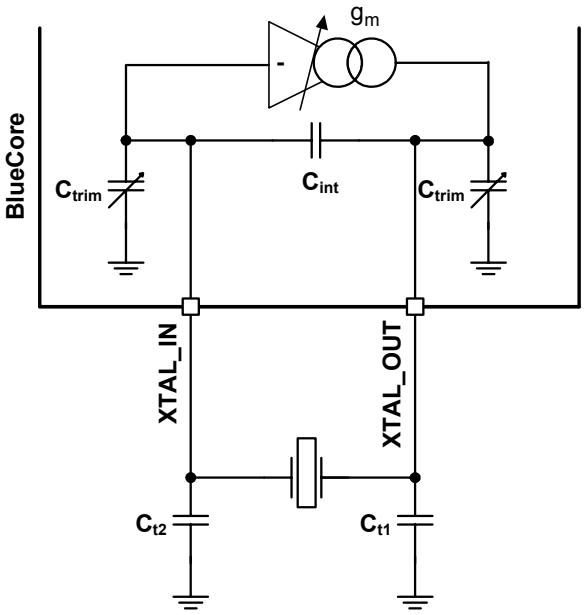


Figure 11.5: Crystal Driver Circuit

Figure 11.6 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

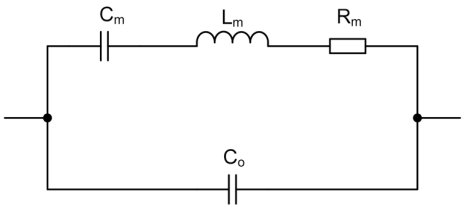


Figure 11.6: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore4-External contains variable internal capacitors to provide a fine trim.

	Min	Typ	Max
Frequency	8MHz	16MHz	32MHz
Initial Tolerance	-	±25ppm	-
Pullability	-	±20ppm/pF	-

Table 11.4: Crystal Specification

The BlueCore4-External driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

11.3.2 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore4-External provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence, slew rate at XTAL_IN (to which all on-chip clocks are referred). Crystal load capacitance, C_l is calculated with Equation 11.4:

$$C_l = C_{int} + \frac{C_{trim}}{2} + \frac{C_{t1} \bullet C_{t2}}{C_{t1} + C_{t2}}$$

Equation 11.4: Load Capacitance

Where:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

Note:

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

11.3.3 Frequency Trim

BlueCore4-External enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on-chip trim capacitors, C_{trim}. The value of C_{trim} is set by a 6-bit word in the PS Key PSKEY_ANA_FTRIM (0x1f6). Its value is calculated thus:

$$C_{trim} = 110fF \times PSKEY\_ANA\_FTRIM$$

Equation 11.5: Trim Capacitance

There are two C_{trim} capacitors, which are both connected to ground. When viewed from the crystal terminals, they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by Equation 11.6.

$$\frac{\Delta(F_X)}{F_X} = pullability \times 55 \times 10^{-3} (ppm/LSB)$$

Equation 11.6: Frequency Trim

Where Fx is the crystal frequency and pullability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 11.7.

$$\frac{\partial(F_X)}{\partial(F_X)} = F_X \bullet \frac{C_m}{4(C_l + C_0)^2}$$

Equation 11.7: Pullability

Where:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 11.6.

Note:

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

11.3.4 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore4-External uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 11.8:

$$g_m > \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{(2\pi F_X)^2 R_m((C_0+C_{int})(C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

Equation 11.8: Transconductance Required for Oscillation

BlueCore4-External guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance, by setting the PS Key PSKEY_XTAL_LVL (0x241).

11.3.5 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore4-External crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance may be calculated for it with the following formula in Equation 11.9:

$$R_{neg} > \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{g_m(2\pi F_X)^2(C_0+C_{int})((C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

Equation 11.9: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore4-External driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

11.3.6 Crystal PS Key Settings

See tables in section 11.2.5.

11.3.7 Crystal Oscillator Characteristics

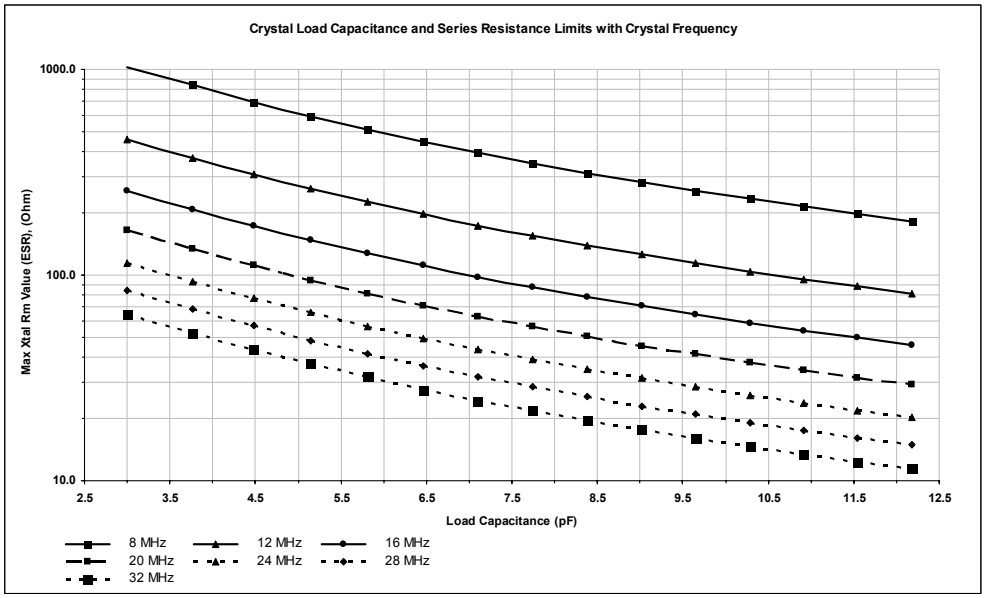


Figure 11.7: Crystal Load Capacitance and Series Resistance Limits with Crystal Frequency

Note:

Graph shows results for BlueCore4-External crystal driver at maximum drive level.

Conditions:

C_{trim} = 3.4pF centre value

Crystal C_o = 2pF

Transconductance setting = 2mA/V

Loop gain = 3

C_{t1}/C_{t2} = 3

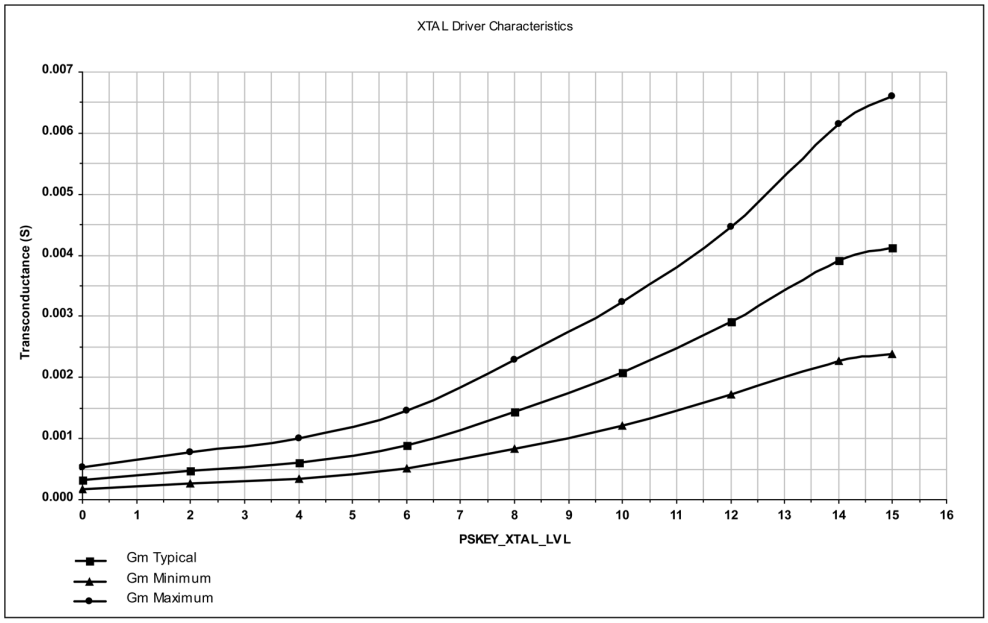


Figure 11.8: Crystal Driver Transconductance vs. Driver Level Register Setting

Note:

Drive level is set by PS Key PSKEY_XTAL_LVL (0x241).

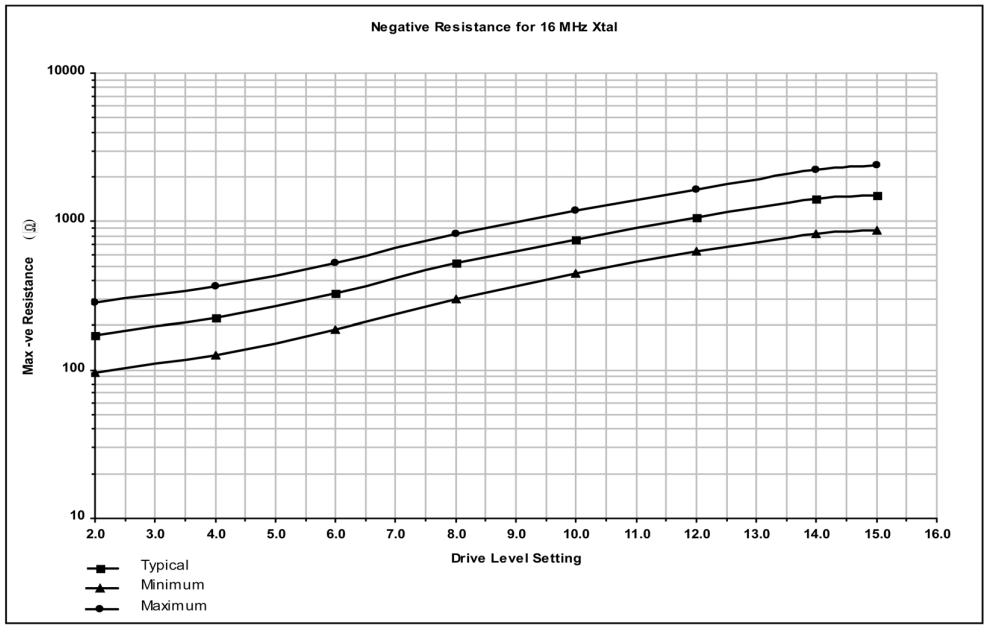


Figure 11.9: Crystal Driver Negative Resistance as a Function of Drive Level Setting

Crystal parameters:

Crystal frequency 16MHz (refer to your software build release note for supported frequencies).

Crystal C_0 = 0.75pF

Circuit parameters:

C_{trim} = 8pF, maximum value

C_{t1},C_{t2} = 5pF (3.9pF plus 1.1 pF stray)

(Crystal total load capacitance 8.5pF)

Note:

This is for a specific crystal and load capacitance.

11.4 Off-Chip Program Memory

The external memory port provides a facility to interface up to 8Mbits of 16 bit external memory. This off chip storage is used to store BlueCore4-External settings and program code. Flash is the storage mechanism typically used by BlueCore4-External modules, however external masked ROM may also be used if the host takes over responsibility for storing configuration data.

The external memory port consists of 16 bi-directional data lines, D[15:0]; 19 output address lines, A[18:0] and three active low output control signals (WEB, CEB, REB). WEB is asserted when data is written to external memory. REB is asserted when data is read from external memory and the chip select line. CSB is asserted when any data transfer (read or write) is required. All of the external memory port connections are implemented using CMOS technology and use standard 0V and VDD_MEM (1.8-3.6V) signalling levels.

Parameter	Value
Data width	16-bit
Minimum total capacity	4Mbit (256kWord)
Maximum access time	90ns @125°C 50pF load
	110ns @85°C 10pF load

Table 11.5: Flash Device Hardware Requirements

In addition to these hardware requirements, particular care should be taken to ensure that the sector organisation of the extended memory has the correct format. A sector is defined as an individually erasable area of external Flash.

It is important to make sure that external memory devices meet certain minimum specifications. In addition particular care should be taken to ensure that the sector organisation of the extended memory has the correct format.

11.4.1 Minimum Flash Specification

The flash device used with BlueCore4-External must meet the following criteria:

- Either standard or extended form of the JEDEC (AMD/Fujitsu/SST) or Intel command set.
- Access time must be ≤90ns @125°C 50pF load or ≤110ns @85°C 10pF load.
- Write strobe of 100ns.
- Accessible in word mode, i.e., via a 16-bit data bus.
- Support changing different bits within each word from 1 to 0 in at least two separate programming operations.
- Programming and erase times must have fixed upper limits.
- Must be bottom boot or uniform sector.
- Must have independently erasable sectors with at least the following boundaries. See Memory Map for more information.

Word Address	Size (kWords)
0x00000 - 0x01FFF	8
0x02000 - 0x02FFF	4
0x03000 - 0x03FFF	4
0x04000 - 0x07FFF	16
0x08000 - 0x0FFFF	32
0x10000 - 0x17FFF	32
0x18000 - ...	Don't care

Table 11.6: Flash Sector Boundaries

Important Note:

Satisfaction of these criteria is not sufficient for a particular device to be used; it must also support the Common Flash Interface described in section 11.4.2 or be supported in the BlueCore4-External firmware and host-side tools.

11.4.2 Common Flash Interface

The firmware can adapt automatically to work with some flash devices. If in addition to satisfying the minimum Flash specification described above, they meet the following criteria:

- The device must support the Common Flash Interface, as defined by JEDEC standard JESD68.
- The device must return one of the following codes for either the Primary or Alternative Algorithm Command Set (offset 0x13b or 0x17 of the Query Structure Output):

Code	Description
0x0001	Intel/Sharp Extended Command Set
0x0002	AMD/Fujitsu Standard Command Set
0x0003	Intel Standard Command Set
0x0701	AMD/Fujitsu Extended Command Set

Table 11.7: Common Flash Interface Algorithm Command Set Codes

- The device must return one of the following patterns of Erase Block Region Information (beginning at offset 0x2d of the Query Structure Output). If any of these criteria is not met, then the device will not work unless the device is supported by the BlueCore4-External firmware.

11.4.3 Memory Timing

Memory Write Cycle

Symbol	Parameter	Minimum[a]	Typical	Maximum[a]	Unit
t_{wc}	Write cycle time	300	-	-	ns
$t_{dat:su}$	Data set-up time	150	-	-	ns
$t_{dat:hd}$	Data hold time	150	-	-	ns
$t_{addr:su}$	Address set-up time	150	-	-	ns
$t_{we:low}$	WEB low	100	-	-	ns

Table 11.8: Memory Write Cycle

(a) Valid for temperatures between -40°C and +105°C

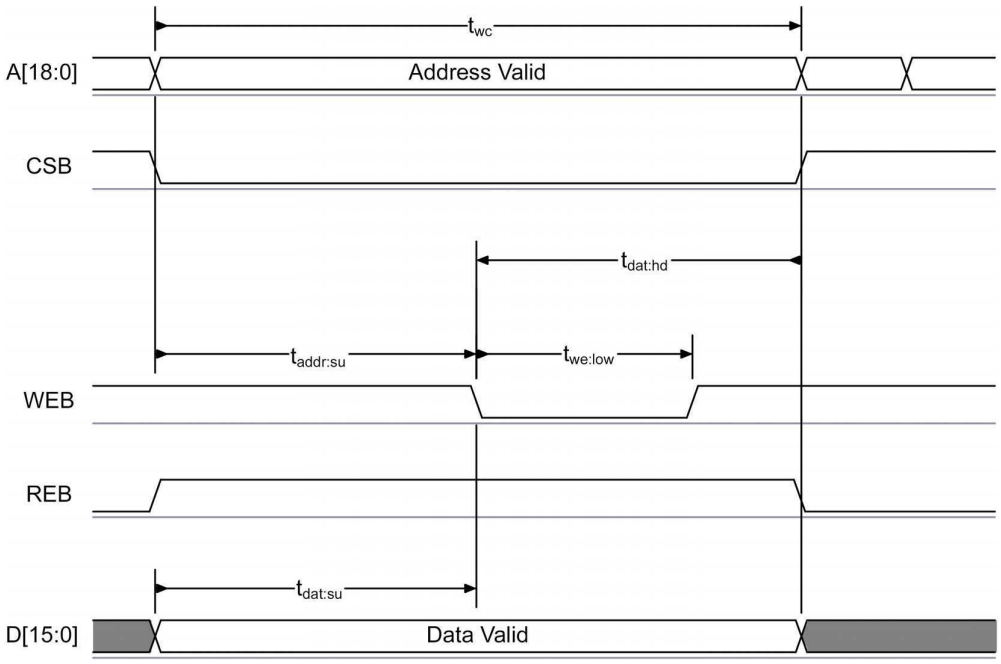


Figure 11.10: Memory Write Cycle

Memory Read Cycle

Symbol	Parameter	Minimum[a]	Typical	Maximum[a]	Unit
t_{rc}	Read cycle time	114	125	-	ns
t_{aa}	Address access time	-	-	110	ns
t_{re}	Read enable access time	-	-	110	ns
$t_{dat:hd}$	Data hold time from address line	0	-	-	ns

Table 11.9: Memory Read Cycle

(a) Valid for temperatures between -40°C and +105°C

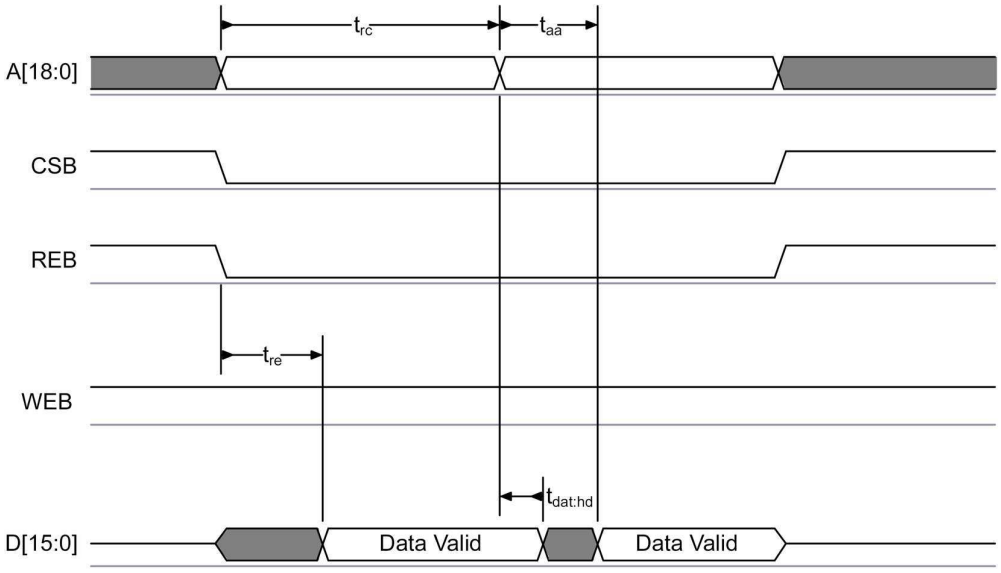


Figure 11.11: Memory Read Cycle

11.5 UART Interface

BlueCore4-External UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.(1)

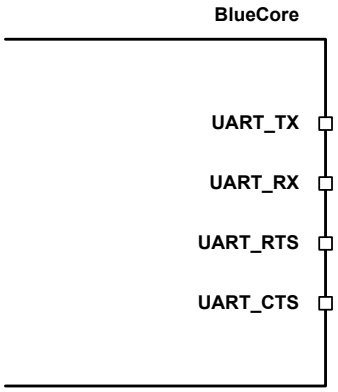


Figure 11.12: Universal Asynchronous Receiver

Four signals are used to implement the UART function, as shown in Figure 11.12. When BlueCore4-External is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_USB.

UART configuration parameters, such as baud rate and packet format, are set using BlueCore4-External software.

Note:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	3M baud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Channel		8

Table 11.10: Possible UART Settings

(1) Uses RS232 protocol, but voltage levels are 0V to VDD_USB (requires external RS232 transceiver chip).

The UART interface is capable of resetting BlueCore4-External upon reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 11.13. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialise the system to a known state. Also, BlueCore4-External can emit a break character that may be used to wake the host.

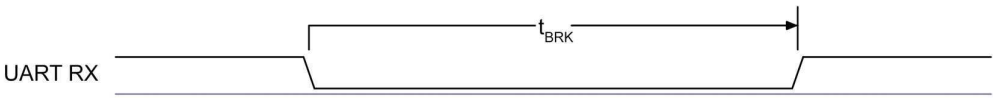


Figure 11.13: Break Signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 11.11 shows a list of commonly used baud rates and their associated values for the PS Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 11.10.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUD\_RATE}}{0.004096}$$

Equation 11.10: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%

Table 11.11: Standard Baud Rates

11.5.1 UART Bypass

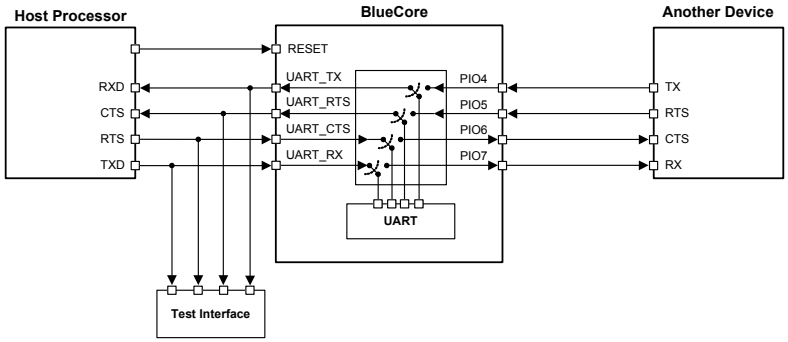


Figure 11.14: UART Bypass Architecture

11.5.2 UART Configuration While RESET is Active

The UART interface for BlueCore4-External while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore4-External reset is de-asserted and the firmware begins to run.

11.5.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore4-External can be used. The default state of BlueCore4-External after reset is de-asserted; this is for the host UART bus to be connected to the BlueCore4-External UART, thereby allowing communication to BlueCore4-External via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.(1)

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore4-External. Upon this issue, it will switch the bypass to PIO[7:4] as Figure 11.14 indicates. Once the bypass mode has been invoked, BlueCore4-External will enter the Deep Sleep state indefinitely.

In order to re-establish communication with BlueCore4-External, the chip must be reset so that the default configuration takes effect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore, it is not possible to have active Bluetooth links while operating the bypass mode.

11.5.4 Current Consumption in UART Bypass Mode

The current consumption for a device in UART bypass mode is equal to the values quoted for a device in standby mode.

(1) The range of the signalling level for the standard UART described in section 11.5 and the UART bypass may differ between CSR BlueCore devices, as the power supply configurations are chip dependent. For BlueCore4-External, the standard UART is supplied by VDD_USB, so has signalling levels of 0V and VDD_USB. Whereas in the UART bypass mode, the signals appear on PIO[4:7] which are supplied by VDD_PADS, therefore the signalling levels are 0V and VDD_PADS.

11.6 USB Interface

BlueCore4-External devices contain a full speed (12Mbits/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.0+EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

As USB is a master/slave oriented system (in common with other USB peripherals), BlueCore4-External only supports USB Slave operation.

11.6.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore4-External, therefore, have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP/USB_DN and the cable.

11.6.2 USB Pull-Up Resistor

BlueCore4-External features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore4-External is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD_PADS=3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

11.6.3 Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

11.6.4 Self-Powered Mode

In self-powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore4-External via a resistor network (R_{vb1} and R_{vb2}), so BlueCore4-External can detect when VBUS is powered up. BlueCore4-External will not pull USB_DP high when VBUS is off.

Self-powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5KΩ 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The internal pull-up in BlueCore is only suitable for bus-powered USB devices, e.g., dongles.

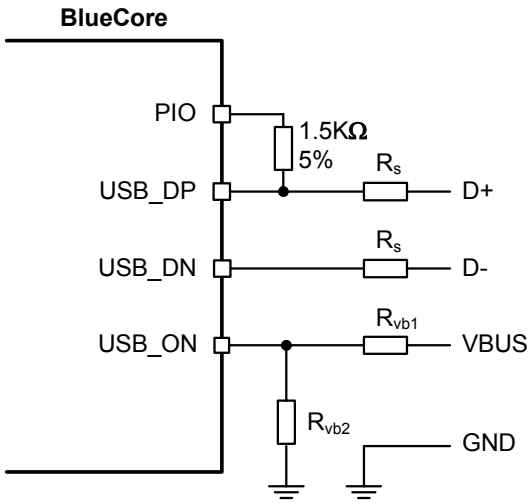


Figure 11.15: USB Connections for Self-Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

Note:

USB_ON is shared with BlueCore4-External PIO terminals.

Identifier	Value	Function
R_s	27Ω nominal	Impedance matching to USB cable
R_{vb1}	22kΩ 5%	VBUS ON sense divider
R_{vb2}	47kΩ 5%	VBUS ON sense divider

Table 11.12: USB Interface Component Values

11.6.5 Bus-Powered Mode

In bus-powered mode, the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore4-External negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus-powered mode, BlueCore4-External requests 100mA during enumeration.

For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting the PS Key PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification. See USB Specification v1.1, section 7.2.4.1. Some applications may require soft start circuitry to limit inrush current if more than 10µF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore4-External will result in reduced receive sensitivity and a distorted RF transmit signal.

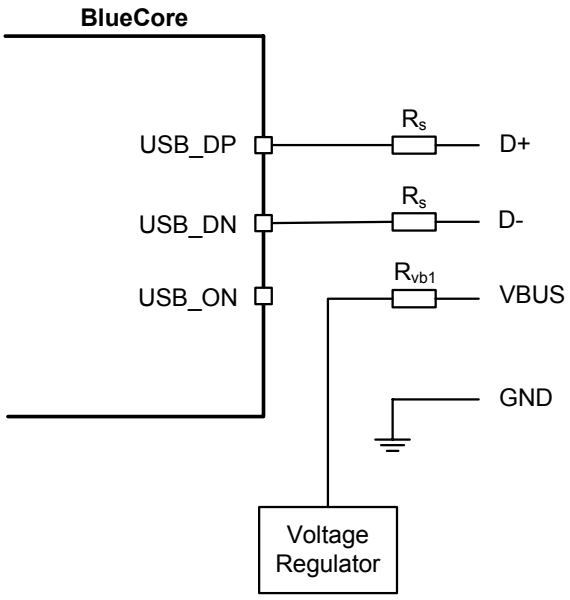


Figure 11.16: USB Connections for Bus-Powered Mode

11.6.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB suspend mode. While in USB Suspend, bus-powered devices must not draw more than 0.5mA from USB VBUS (self-powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus-powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100μA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore4-External. The entire circuit must be able to enter the suspend mode. Refer to separate CSR documentation for more details on USB Suspend.

11.6.7 Detach and Wake_Up Signalling

BlueCore4-External can provide out-of-band signalling to a host controller by using the control lines called USB_DETACH and USB_WAKE_UP. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore4-External into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore4-External to put USB_DN and USB_DP in a high impedance state and turns off the pull-up resistor on DP. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore4-External will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable) and cannot be sent while BlueCore4-External is effectively disconnected from the bus.

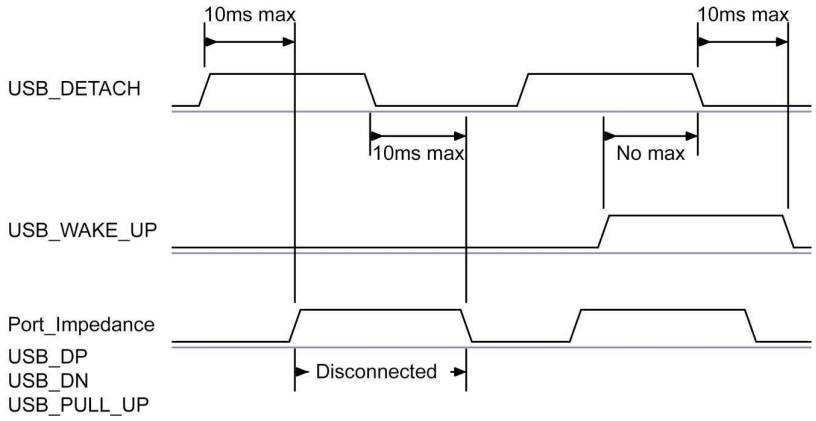


Figure 11.17: USB_DETACH and USB_WAKE_UP Signal

11.6.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore4-External and Bluetooth software running on the host computer. Suitable drivers are available from http://www.csrsupport.com.

11.6.9 USB 1.1 Compliance

BlueCore4-External is qualified to the USB Specification v1.1, details of which are available from www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore4-External meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification v2.0 (Chapter 7) electrical requirements.

11.6.10 USB 2.0 Compatibility

BlueCore4-External is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

11.7 Serial Peripheral Interface

BlueCore4-External uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore4-External via the four dedicated serial peripheral interface terminals. Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

11.7.1 Instruction Cycle

The BlueCore4-External is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 11.13 shows the instruction cycle for an SPI transaction.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8 bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

Table 11.13: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore4-External on the rising edge of the clock line SPI_CLK. When reading, BlueCore4-External will reply to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is teminated by taking SPI_CSB high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore4-External offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

11.7.2 Writing to BlueCore4-External

To write to BlueCore4-External, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

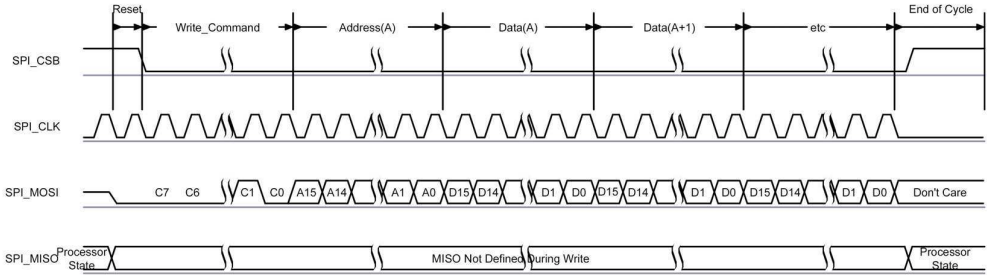


Figure 11.18: Write Operation

11.7.3 Reading from BlueCore4-External

Reading from BlueCore4-External is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore4-External then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

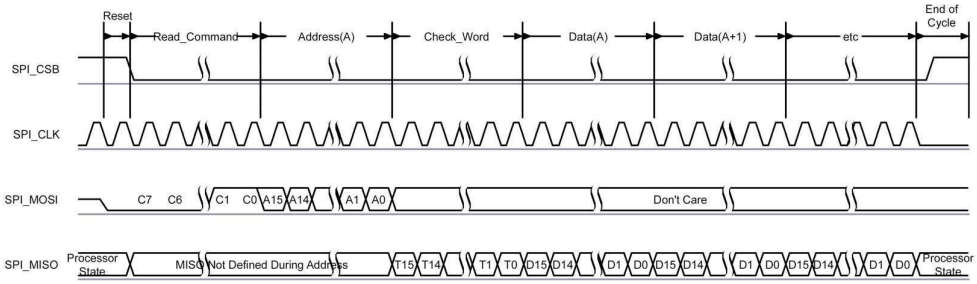


Figure 11.19: Read Operation

11.7.4 Multi-Slave Operation

BlueCore4-External should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore4-External is deselected (SPI_CSB = 1), the SPI_MISO line does not float. Instead, BlueCore4-External outputs 0 if the processor is running or 1 if it is stopped.

11.8 PCM CODEC Interface

Pulse Code Modulation (PCM) is a standard method used to digitise audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, BlueCore4-External has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore4-External offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore4-External allows the data to be sent to and received from a SCO connection. (1)

Up to three SCO connections can be supported by the PCM interface at any one time.

BlueCore4-External can operate as the PCM interface master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave, it can operate with an input clock up to 2048kHz. BlueCore4-External is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG32 (0x1b3).

BlueCore4-External interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore4-External is also compatible with the Motorola SSI™ interface

(1) Subject to firmware support. Contact CSR for current status.

11.8.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore4-External generates PCM_CLK and PCM_SYNC.

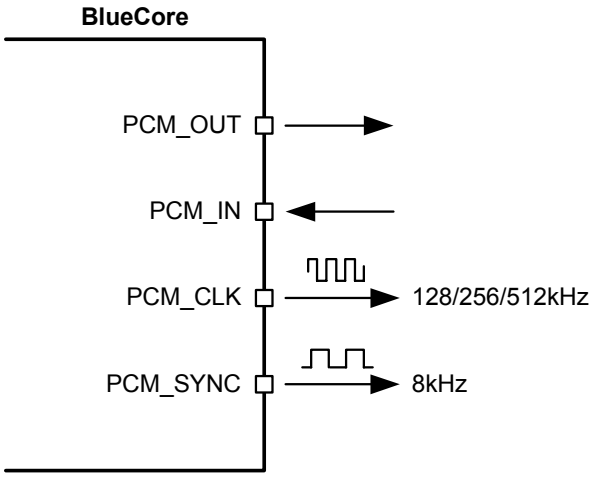


Figure 11.20: BlueCore4-External as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore4-External accepts PCM_CLK rates up to 2048kHz.

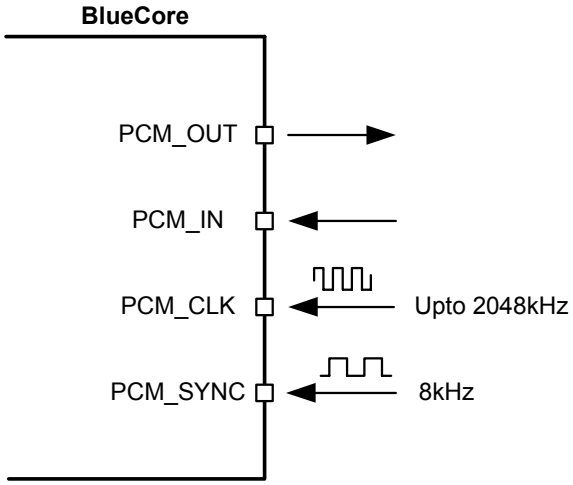


Figure 11.21: BlueCore4-External as PCM Interface Slave

11.8.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore4-External is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore4-External is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5µs long.

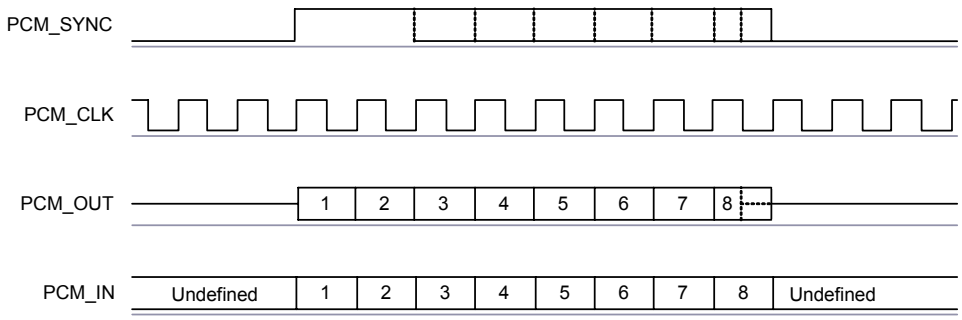


Figure 11.22: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore4-External samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

11.8.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

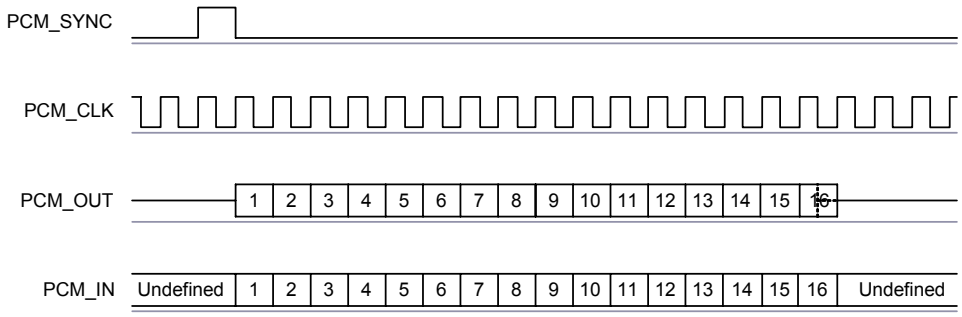


Figure 11.23: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore4-External samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

11.8.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

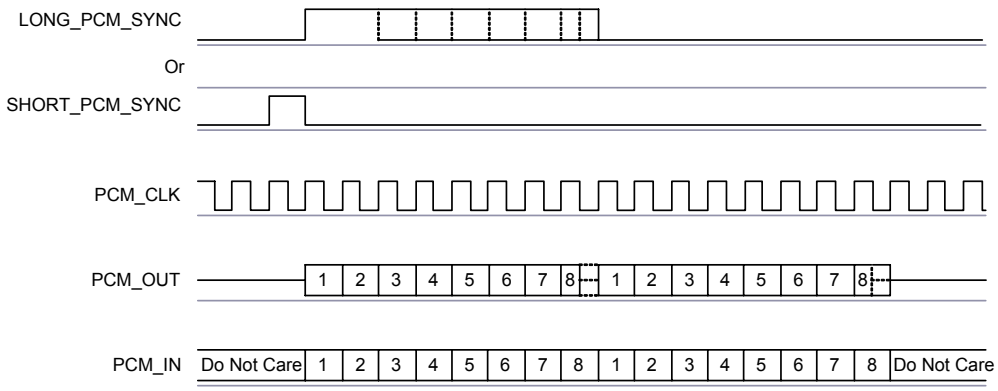


Figure 11.24: Multi-slot Operation with Two Slots and 8-bit Companded Samples

11.8.5 GCI Interface

BlueCore4-External is compatible with the General Circuit Interface (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

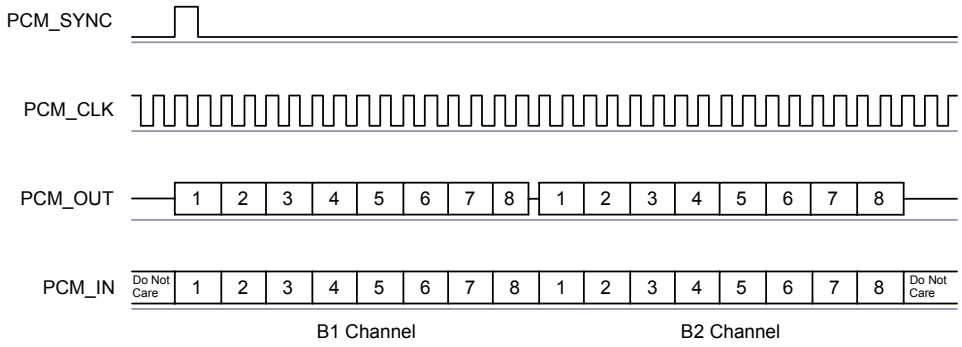


Figure 11.25: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore4-External in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

11.8.6 Slots and Sample Formats

BlueCore4-External can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore4-External supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

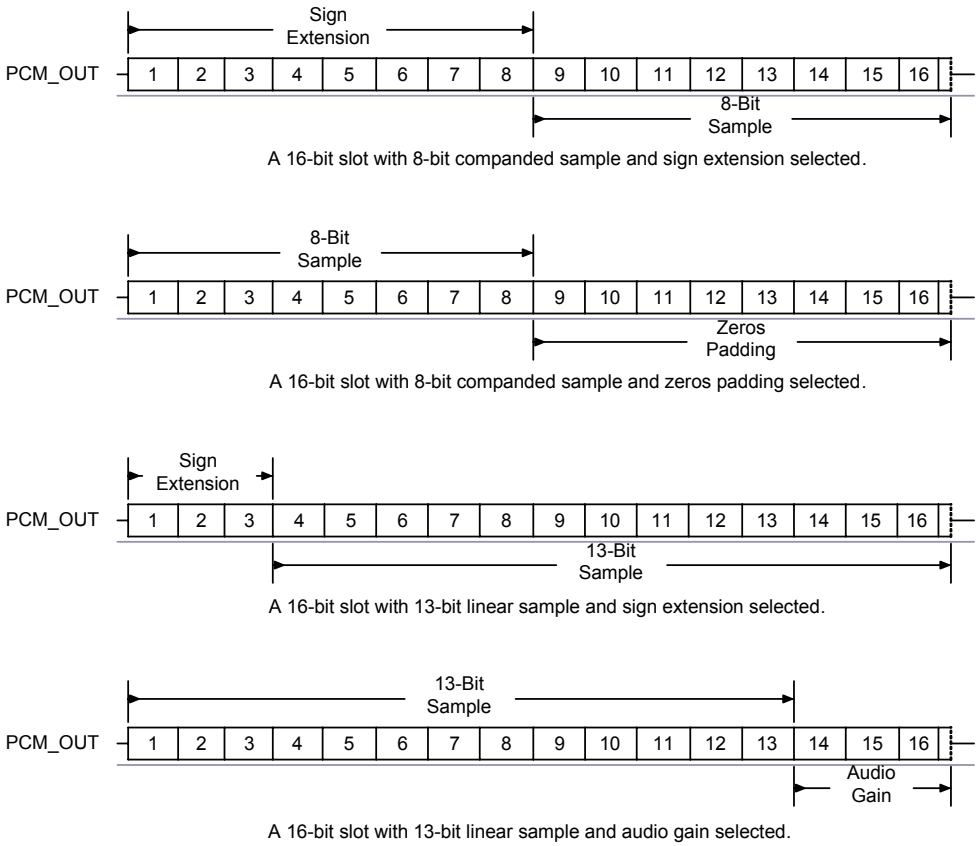


Figure 11.26: 16-Bit Slot Length and Sample Formats

11.8.7 Additional Features

BlueCore4-External has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

11.8.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table 11.16.	-	128 256 512	-	kHz
		48MHz DDS generation. Selection of frequency is programmable. See Table 11.17 and PCM_CLK and PCM_SYNC Generation on page 97.	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
t_{mclkh}[(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl}[(a)]	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation			21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 11.14: PCM Master Timing

(a) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

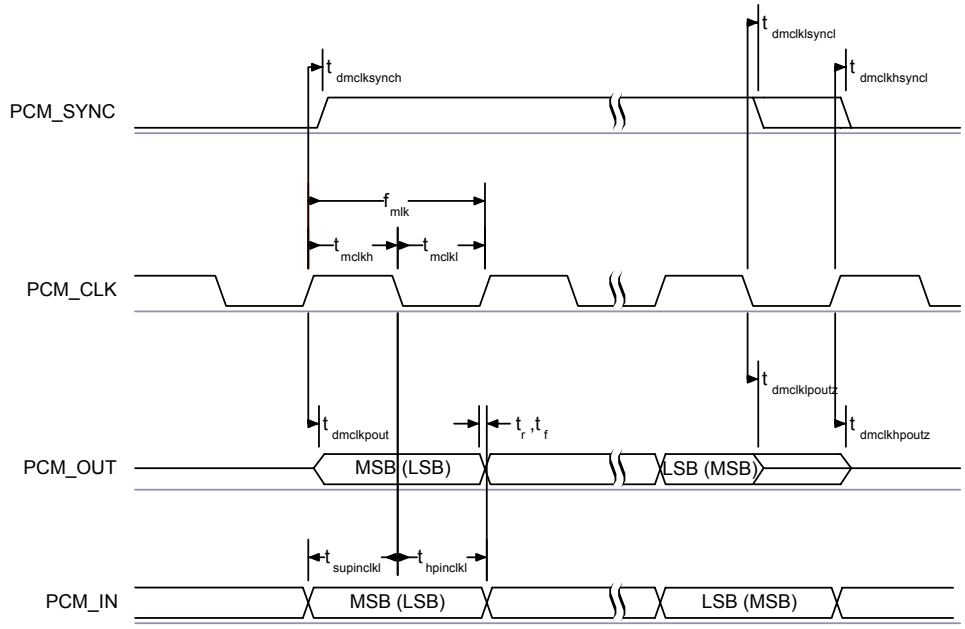


Figure 11.27: PCM Master Timing Long Frame Sync

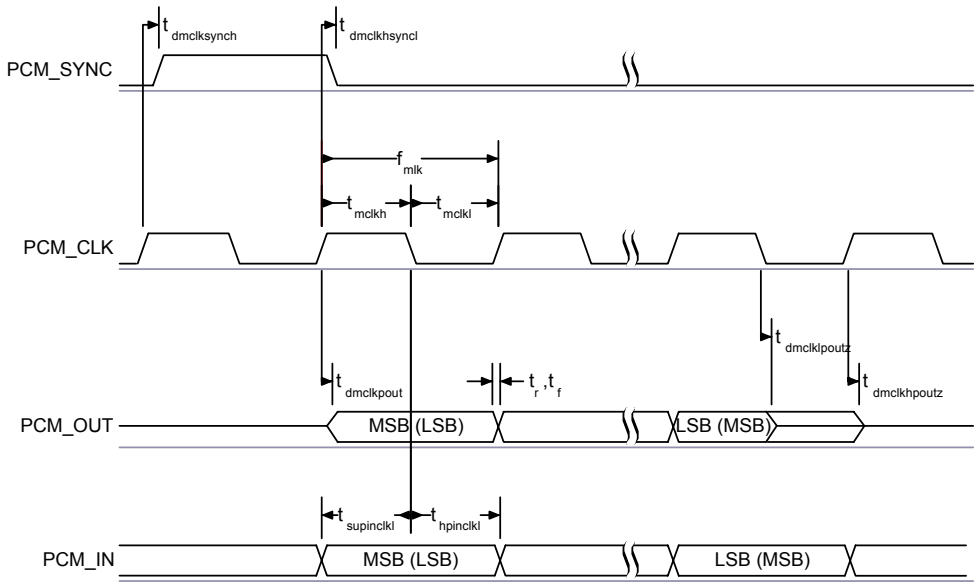


Figure 11.28: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 11.15: PCM Slave Timing

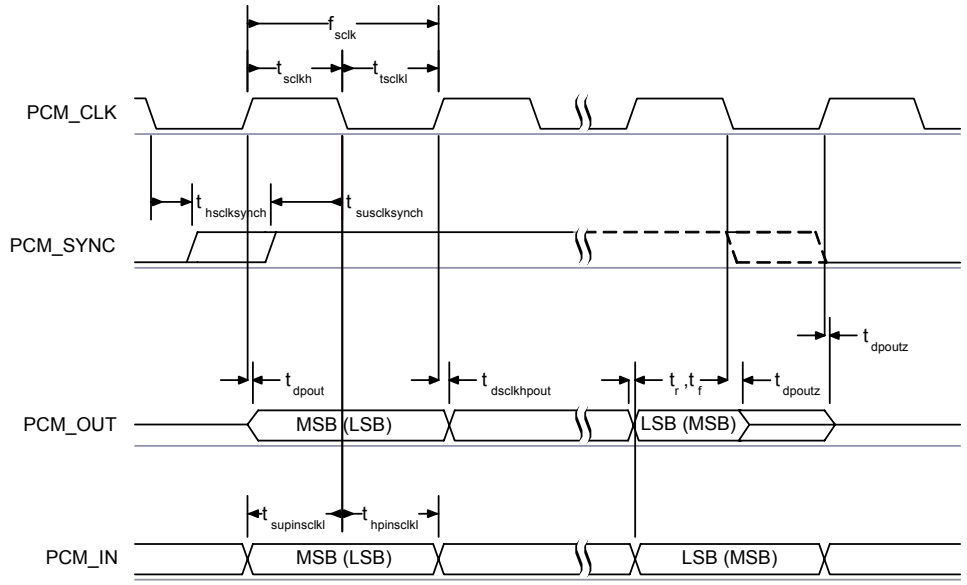


Figure 11.29: PCM Slave Timing Long Frame Sync

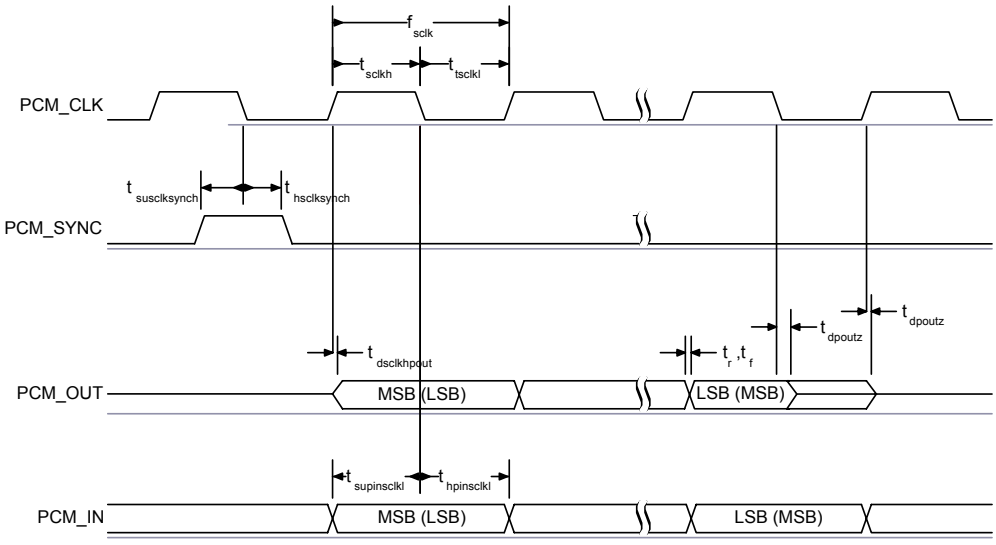


Figure 11.30: PCM Slave Timing Short Frame Sync

PCM_CLK and PCM_SYNC Generation

BlueCore4-External has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by Direct Digital Synthesis (DDS) from BlueCore4-External internal 4MHz clock (which is used in BlueCore2-External). Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This second method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

The Equation 11.11 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 11.11: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock

The frequency of PCM_SYNC relative to PCM_CLK can be set using Equation 11.12:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 11.12: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

11.8.9 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 detailed in Table 11.16 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 11.17. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT.

Name	Bit Position	Description
-	0	Set to 0
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tri-state PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode
MUTE_EN	10	1 = force PCM_OUT to 0
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000

Name	Bit Position	Description
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Table 11.16: PSKEY_PCM_CONFIG32 Description

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table 11.17: PSKEY_PCM_LOW_JITTER_CONFIG Description

11.9 I/O Parallel Ports

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

PIO[0] and PIO[1] are normally dedicated to RXEN and TXEN respectively, but they are available for general use.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO[2] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore4-External is provided from a system application specific integrated circuit (ASIC). Using PSKEY_CLOCK_REQUEST_ENABLE (0x246), this terminal can be configured to be low when BlueCore4-External is in Deep Sleep and high when a clock is required. The clock must be supplied within 4ms of the rising edge of PIO[6] or PIO[2] to avoid losing timing accuracy in certain Bluetooth operating modes.

BlueCore4-External has three general purpose analogue interface pins, AIO[0], AIO[1] and AIO[2]. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip band gap reference voltage, the other two may be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the band gap reference voltage and a variety of clock signals: 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals, the voltage range is constrained by the analogue supply voltage (1.8V). When configured to drive out digital level signals (e.g., clocks), the output voltage level is determined by VDD_MEM (1.8V).

11.9.1 PIO Defaults for BlueCore4-External

CSR cannot guarantee that these terminal functions remain the same. Refer to the software release note for the implementation of these PIO lines, as they are firmware build-specific.

11.10 I²C Interface

PIO[8:6] can be used to form a master I²C interface. The interface is formed using software to drive these lines. Therefore, it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD), keyboard scanner or EEPROM.

Notes:

PIO lines need to be pulled-up through 2.2kΩ resistors.

PIO[7:6] dual functions, UART bypass and EEPROM support, therefore, devices using an EEPROM cannot support UART bypass mode.

For connection to EEPROMs, refer to CSR documentation on I²C EEPROMS for use with BlueCore. This provides information on the type of devices currently supported.

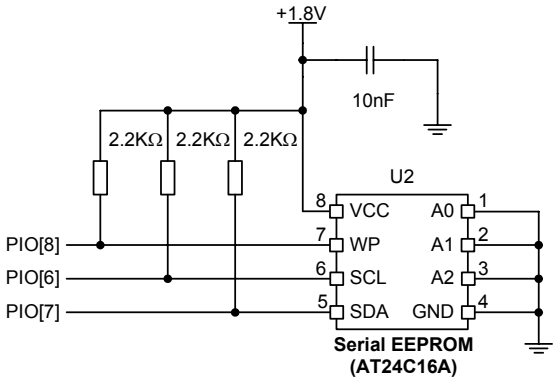


Figure 11.31: Example EEPROM Connection

11.11 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore4-External where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the host clock enables input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore4-External.

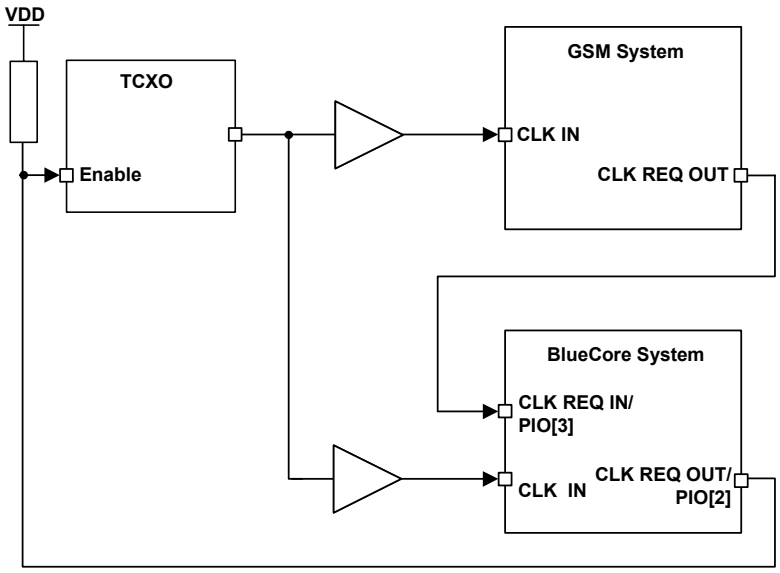


Figure 11.32: Example TXCO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tri-state. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

11.12 RESETB

BlueCore4-External may be reset from several sources: RESETB pin, power on reset, a UART break character or via a software configured watchdog timer.

The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-downs.

Following a reset, BlueCore4-External assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore4-External is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore4-External free runs, again at a safe frequency.

11.12.1 Pin States on Reset

Table 11.18 shows the pin states of BlueCore4-External on reset.

Pin Name	State: BlueCore4-External
PIO[11:0]	Input with weak pull-down
PCM_OUT	Tri-stated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	Input with weak pull-down
UART_TX	Output tri-stated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tri-stated with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Output tri-stated with weak pull-down
AIO[2:0]	Output, driving low
RESETB	Input with weak pull-up
TEST_EN	Input with strong pull-down
RF_A	High impedance
RF_B	High impedance
RF_IN	High impedance
XTAL_IN	High impedance, 250k to XTAL_OUT
XTAL_OUT	High impedance, 250k to XTAL_IN

Table 11.18: Pin States of BlueCore4-External on Reset

11.12.2 Status after Reset

The chip status after a reset is as follows:

- Warm Reset: Baud rate and RAM data remain available
- Cold Reset[1] : Baud rate and RAM data not available

[1] A Cold Reset is either Power cycle, system reset (firmware fault code) or Reset signal. See section 11.12.

11.13 Power Supply

11.13.1 Voltage Regulator

An on-chip linear voltage regulator can be used to power the 1.8V dependent supplies. It is advised that a smoothing circuit using a 2.2μF low ESR capacitor and 2.2Ω resistor be placed on the output VDD_ANA adjacent to VREG_IN.

The regulator is switched into a low power mode when the device is sent into Deep Sleep mode. When the on-chip regulator is not required VDD_ANA is a 1.8V input and VREG_IN must be either open circuit or tied to VDD_ANA.

11.13.2 Sequencing

It is recommended that VDD_CORE, VDD_RADIO, VDD_LO and VDD_ANA be powered at the same time. The order of powering supplies for VDD_CORE, VDD_PIO, VDD_PADS and VDD_USB is not important. However, if VDD_CORE is not present, all inputs have a weak pull-down irrespective of the reset state.

11.13.3 Sensitivity to Disturbances

CSR recommends if supplying BlueCore4-External from an external voltage source that VDD_LO, VDD_ANA and VDD_RADIO should have less than 10mV rms noise levels between 0 to 10MHz. In addition, avoid single tone frequencies. CSR recommends a simple RC filter for VDD_CORE, as this reduces transients put back onto the power supply rails.

The remaining supplies VDD_MEM, VDD_PIO, VDD_PADS and VDD_USB can be connected together with the VREG_IN to the 3.3V supply and simply decoupled as shown in Figure 12.1.

The transient response of the regulator is also important. At the start of a packet, power consumption will jump to high levels. See the average current consumption section. The regulator should have a response time of 20μs or less; it is essential that the power rail recovers quickly.

12 Application Schematic

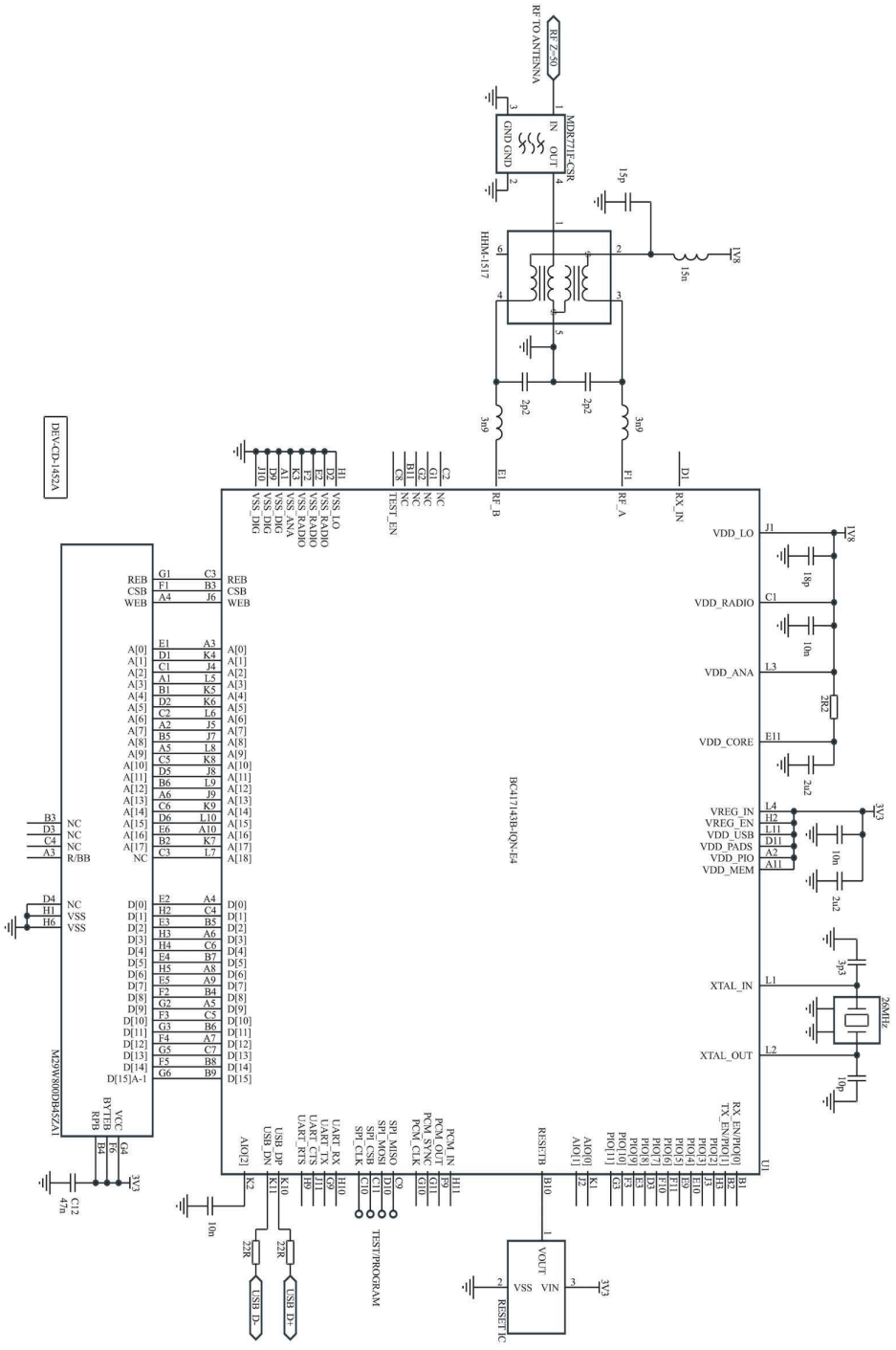
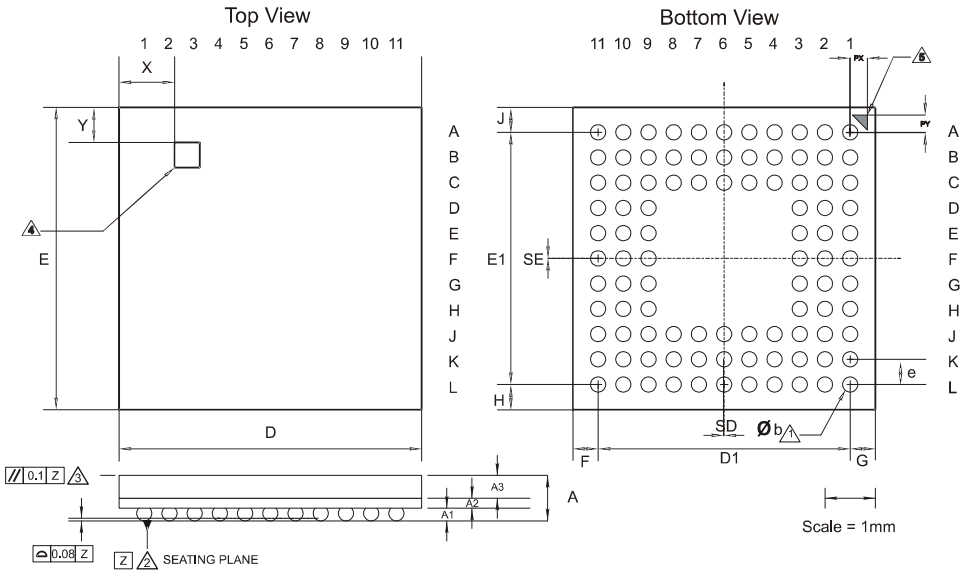


Figure 12.1: Application Circuit for Radio Characteristics Specification

13 Package Dimensions

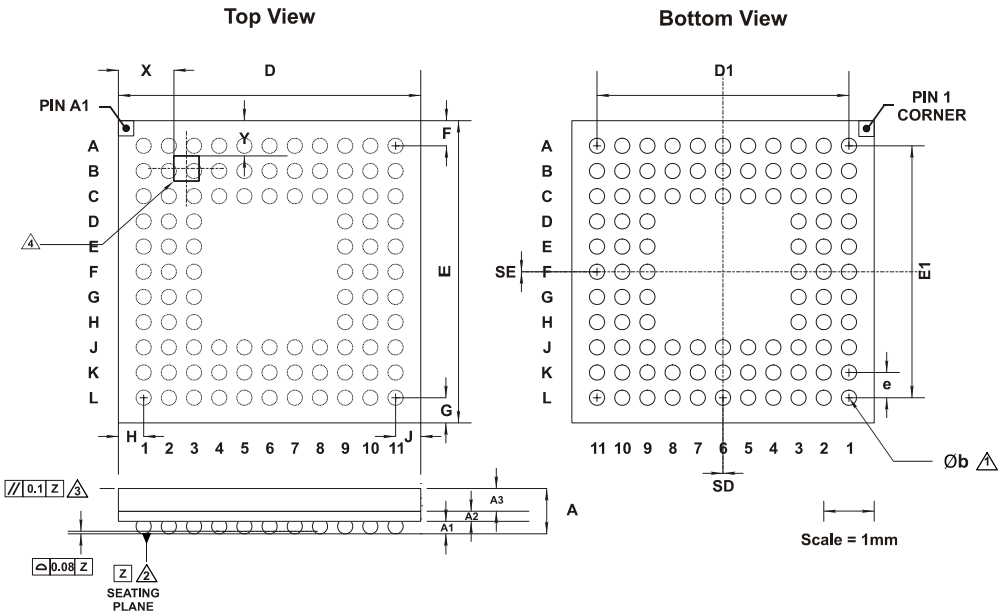
13.1 8 x 8mm TFBGA 96-Ball Package



Description	96-Ball Thin Fine-Pitch Ball Grid Array (TFBGA)			
Size	8 x 8 x 1.2mm			
Pitch	0.65mm			
Package Ball Land	Solder mask defined. Solder mask aperture 260µm Ø			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A			1.2	(1) Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1	0.18	0.23	0.26	
A2		0.21		
A3		0.70		(2) Datum Z is defined by the spherical crowns of the solder balls
b	0.27	0.32	0.37	
D	7.90	8.00	8.10	(3) Parallelism measurement shall exclude any effect of mark on top surface of package
E	7.90	8.00	8.10	
e		0.65		
D1		6.50		(4) Top-side polarity mark. The dimensions of the square polarity mark are 0.75 x 0.75mm.
E1		6.50		
F	0.70	0.75	0.80	(5) Bottom-side polarity mark. The dimensions of the triangular polarity mark are 3.0 x 3.0 x 4.2mm.
G	0.70	0.75	0.80	
H	0.70	0.75	0.80	
J	0.70	0.75	0.80	
PX		0.47		
PY		0.47		
SD		0		
SE		0		
X		1.35		
Y		0.85		
JEDEC	MO-195			
Unit	mm			

Figure 13.1: BlueCore4-External 96-Ball TFBGA Package Dimensions

13.2 6 x 6mm VFBGA 96-Ball Package



Description	96-Ball Very-Thin Fine-Pitch Ball Grid Array (VFBGA)			
Size	6 x 6 x 1mm			
Pitch	0.5mm			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A	0.8	0.9	1.0	(1) Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1	0.2	0.25	0.3	
A2		0.22		
A3		0.45		
b	0.25	0.30	0.35	(2) Datum Z is defined by the spherical crowns of the solder balls
D	5.90	6.00	6.10	
E	5.90	6.00	6.10	
e		0.50		(3) Parallelism measurement shall exclude any effect of mark on top surface of package
D1		5.00		
E1		5.00		
F	0.450	0.500	0.550	
G	0.450	0.500	0.550	(4) Polarity Mark. The dimensions of the polarity mark are 0.5 x 0.5mm.
H	0.450	0.500	0.550	
J	0.450	0.500	0.550	
PD		-		
PX		-		
PE		-		
PY		-		
SD		0		
SE		0		
X		1.10		
Y		0.70		
JEDEC	MO-225			
Unit	mm			

Figure 13.2: BlueCore4-External 96-Ball VFBGA Package Dimensions

14 Ordering Information

14.1 BlueCore4-External

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	96-Ball TFBGA (Pb free)	8 x 8 x 1.2mm	Tape and reel	BC417143B-IQN-E4
UART and USB	96-Ball VFBGA (Pb free)	6 x 6 x 1mm	Tape and reel	BC417143B-IRN-E4

Minimum Order Engineering Sample Quantity

2kpcs taped and reeled

Minimum Order Production Quantity

2kpcs taped and reeled

15 RoHS Statement with a List of Banned Materials

15.1 RoHS Statement

BlueCore4-External where explicitly stated in this Data Sheet meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

15.1.1 List of Banned Materials

The following banned substances are not present in BlueCore4-External which is compliant with RoHS:

- Cadmium
- Lead
- Mercury
- Hexavalent chromium
- PBB (Polybrominated Bi-Phenyl)
- PBDE (Polybrominated Diphenyl Ether)

In addition, BlueCore4-External is free from the following substances:

- PVC (Poly Vinyl Chloride)

16 Contact Information

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To contact a CSR representative, go to *www.csr.com/contacts.htm*

17 Document References

Document:	Reference, Date:
Specification of the Bluetooth System	v2.0 + EDR, 04 November 2004
Universal Serial Bus Specification	v2.0, 27 April 2000
Selection of I^2C EEPROMS for Use with BlueCore	bcore-an008Pb, 30 September 2003
EDR RF Test Specification v2.0.E.2	v2.0.E.20, D07r22, 16 March 2004
RF Prototyping Specification for Enhanced Data Rate IP	v.90, r29, 2004

18 Terms and Definitions

8DPSK	8 phase Differential Phase Shift Keying
π/4 DQPSK	pi/4 rotated Differential Quaternary Phase Shift Keying
BlueCore™	Group term for CSR's range of Bluetooth chips
Bluetooth™	Set of technologies providing audio and data transfer over short-range radio connections
ACL	Asynchronous Connection-Less. Bluetooth data packet
ADC	Analogue to Digital Converter
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
A-law	Audio encoding standard
ALU	Arithmetic Logic Unit
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BIST	Built-In Self-Test
BMC	Burst Mode Controller
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CQDDR	Channel Quality Driven Data Rate
CRC	Cyclic Redundancy Check
CSB	Chip Select (Active Low)
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DEVM	Differential Error Vector Magnitude
DFU	Device Firmware Upgrade
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quarternary Phase Shift Keying
ESR	Equivalent Series Resistance
FSK	Frequency Shift Keying
GSM	Global System for Mobile communications
HCI	Host Controller Interface

I²C™	Inter-Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response
INL	Integral Linearity Error
IQ Modulation	In-Phase and Quadrature Modulation
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksps	KiloSamples Per Second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LSB	Least-Significant Bit
μ-law	Audio Encoding Standard
MCU	MicroController Unit
MMU	Memory Management Unit
MISO	Master In Serial Out
MOSI	Master Out Slave In
Mbps	Mega bits per second
OHCI	Open Host Controller Interface
PA	Power Amplifier
PCM	Pulse Code Modulation. Refers to digital voice data
PIO	Parallel Input Output
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REB	Read enable (Active Low)
REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
RoHS	The Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver

SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SD	Secure Digital
SDK	Software Development Kit
SDP	Service Discovery Protocol
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
TBA	To Be Announced
TBD	To Be Defined
TCXO	Temperature Controlled crystal Oscillator
TFBGA	Thin Fine-Pitch Ball Grid Array
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UHCI	Upper Host Control Interface
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
WEB	Write Enable (Active Low)

19 Document History

Date	Revision	Reason for Change
03 JUN 04	a	Original publication of this document. (CSR reference: BC417143B-ds-001Pa)
15 JUN 04	b	Numbering changes made to AIO pins.
06 SEP 04	c	6 x 6mm package option added to data sheet and AUX DAC removed.
23 FEB 05	d	Radio Characteristics - Basic Data Rate section added. Radio Characteristics - Enhanced Data Rate section updated.
15 MAR 05	e	Package information updated, including Package Dimensions section.
10 MAY 05	f	Radio Characteristics - Basic Data Rate section updated. Radio Characteristics - Enhanced Data Rate section updated. Typical Radio Performance - Basic Data Rate section added. Typical Radio Performance - Enhanced Data Rate section added. Document moved to Production Information status.
27 JUL 05	g	Added following to Databook: ▪ Solder Profile Information ▪ PCB Design and Assembly Considerations ▪ Tape and Reel Information ▪ RoHS Information Corrected title typos in Typical Radio Performance - Enhanced Data Rate

BlueCore™4-External

Product Data Sheet

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