Programmable 1-PLL VCXO Clock Synthesizer With 1.8-V, 2.5-V, and 3.3-V Outputs

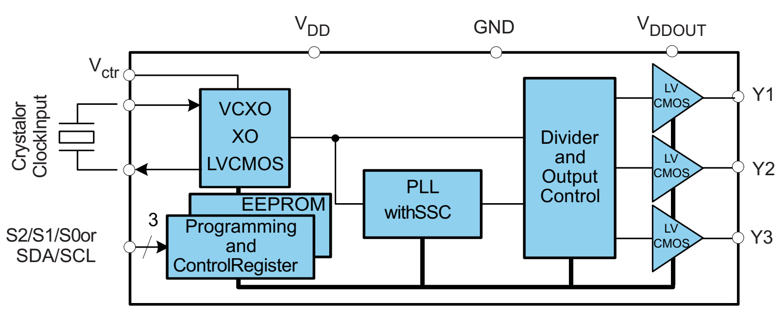
Check for Samples: CDCE913, CDCEL913

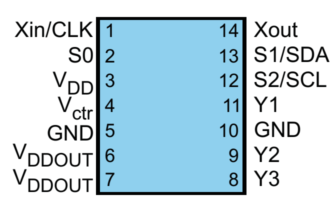
FEATURES

- **Member of Programmable Clock Generator Family**
  - ***CDCE913/CDCEL913: 1-PLL, 3 Outputs***
  - **CDCE925/CDCEL925: 2-PLL, 5 Outputs**
  - **CDCE937/CDCEL937: 3-PLL, 7 Outputs**
  - **CDCE949/CDCEL949: 4-PLL, 9 Outputs**
- **In-System Programmability and EEPROM**
  - **Serial Programmable Volatile Register**
  - **Nonvolatile EEPROM to Store Customer Setting**
- **Flexible Input Clocking Concept**
  - **External Crystal: 8 MHz to 32 MHz**
  - **On-Chip VCXO: Pull Range ±150 ppm**
  - **Single-Ended LVCMOS up to 160 MHz**
- **Free Selectable Output Frequency up to 230 MHz**
- **Low-Noise PLL Core**
  - **PLL Loop Filter Components Integrated**
  - **Low Period Jitter (Typical 50 ps)**
- **Separate Output Supply Pins**
  - **CDCE913: 3.3 V and 2.5 V**
  - **CDCEL913: 1.8 V**
- **Flexible Clock Driver**
  - **Three User-Definable Control Inputs [S0/S1/S2], for example., SSC Selection, Frequency Switching, Output Enable, or Power Down**
  - **Generates Highly Accurate Clocks for Video, Audio, USB, IEEE1394, RFID, Bluetooth™, WLAN, Ethernet™, and GPS**
  - **Generates Common Clock Frequencies Used With TI- DaVinci™, OMAP™, DSPs**
  - **Programmable SSC Modulation**
  - **Enables 0-PPM Clock Generation**
- **1.8-V Device Power Supply**
- **Wide Temperature Range –40° C to 85° C**
- **Packaged in TSSOP**
- **Development and Programming Kit for Easy PLL Design and Programming (TI Pro-Clock™)**

APPLICATIONS

- **D-TV, STB, IP-STB, DVD-Player, DVD-Recorder, Printer**





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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The CDCE913 and CDCEL913 are modular PLL-based low-cost, high-performance, programmable clock synthesizers, multipliers, and dividers. They generate up to 3 output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using the integrated configurable PLL.

The CDCx913 has separate output supply pins, V_{DDOUT}, which is 1.8 V for CDCEL913 and 2.5 V to 3.3 V for CDCE913.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 to 20 pF. Additionally, an on-chip VCXO is selectable which allows synchronization of the output frequency to an external control signal, that is, PWM signal.

The deep M/N divider ratio allows the generation of zero-ppm audio/video, networking (WLAN, BlueTooth, Ethernet, GPS) or interface (USB, IEEE1394, Memory Stick) clocks from e.g., a 27 MHz reference input frequency.

The PLL supports SSC (spread-spectrum clocking). SSC can be center-spread or down-spread clocking which is a common technique to reduce electro-magnetic interference (EMI).

Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability and optimized jitter transfer characteristic.

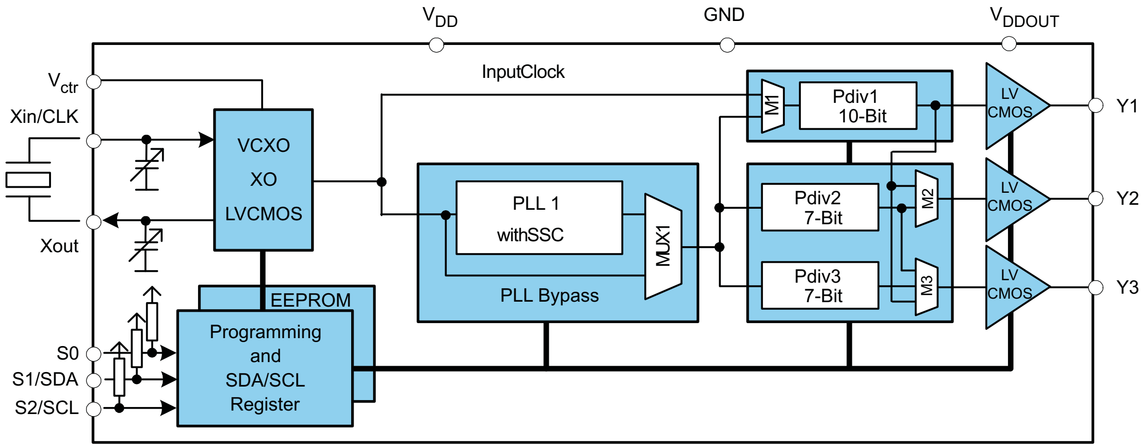
The device supports non-volatile EEPROM programming for ease customization of the device to the application. It is preset to a factory default configuration (see the DEFAULT DEVICE CONFIGURATION section). It can be re-programmed to a different application configuration before PCB assembly, or re-programmed by in-system programming. All device settings are programmable through SDA/SCL bus, a 2-wire serial interface.

Three programmable control inputs, S0, S1 and S2, can be used to select different frequencies, or change SSC setting for lowering EMI, or other control features like, outputs disable to low, outputs 3-state, power down, PLL bypass etc).

The CDCx913 operates in a 1.8 V environment. It operates in a temperature range of –40° C to 85° C.

Terminal Functions for CDCE913, CDCEL913

TERMINAL		I/O	DESCRIPTION
NAME	PIN TSSOP14		
Y1–Y3	11, 9, 8	O	LVCMOS outputs
Xin/CLK	1	I	Crystal oscillator input or LVCMOS clock Input (selectable via SDA/SCL bus)
Xout	14	O	Crystal oscillator output (leave open or pullup when not used)
V_{Ctrl}	4	I	VCXO control voltage (leave open or pullup when not used)
V_{DD}	3	Power	1.8-V power supply for the device
V_{DDOUT}	6, 7	Power	**CDCEL913**: 1.8-V supply for all outputs
			CDCE913: 3.3-V or 2.5-V supply for all outputs
GND	5, 10	Ground	Ground
S0	2	I	User-programmable control input S0; LVCMOS inputs; internal pullup 500k
SDA/S1	13	I/O or I	**SDA:** bidirectional serial data input/output (default configuration), LVCMOS internal pullup; or **S1:** user-programmable control input; LVCMOS inputs; internal pullup 500k
SCL/S2	12	I	**SCL:** serial clock input LVCMOS (default configuration), internal pullup 500k or **S2:** user-programmable control input; LVCMOS inputs; internal pullup 500k



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_{DD}	Supply voltage range	–0.5 to 2.5	V
V_I	Input voltage range(2) (3)	–0.5 to V_{DD} + 0.5	V
V_O	Output voltage range(2)	–0.5 to V_{DD} + 0.5	V
I_I	Input current (V_I < 0, V_I > V_{DD})	20	mA
I_O	Continuous output current	50	mA
T_{stg}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) SDA and SCL can go up to 3.6V as stated in the Recommended Operating Conditions table.

PACKAGE THERMAL RESISTANCE for TSSOP (PW) PACKAGE(1) (2)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		AIRFLOW (lfm)	TSSOP14 °C/W
T_{JA}	Thermal Resistance Junction to Ambient	0	106
		150	93
		200	92
		250	90
		500	85
T_{JC}	Thermal Resistance Junction to Case	—	43
T_{JB}	Thermal Resistance Junction to Board	—	66
$R_{\theta JT}$	Thermal Resistance Junction to Top	—	1.4
$R_{\theta JB}$	Thermal Resistance Junction to Bottom	—	62

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage	1.7	1.8	1.9	V
V_O	Output Yx supply voltage for CDCE913, V_{DDOUT}	2.3		3.6	V
	Output Yx supply voltage for CDCEL913, V_{DDOUT}	1.7		1.9	
V_{IL}	Low-level input voltage LVCMOS			0.3 V_{DD}	V
V_{IH}	High-level input voltage LVCMOS	0.7 V_{DD}			V
$V_{I\ (thresh)}$	Input voltage threshold LVCMOS		0.5 V_{DD}		V
$V_{I(S)}$	Input voltage range S0	0		1.9	V
	Input voltage range S1, S2, SDA, SCL; $V_{I(thresh)}$ = 0.5 V_{DD}	0		3.6	
$V_{I(CLK)}$	Input voltage range CLK	0		1.9	V
I_{OH} /I_{OL}	Output current (V_{DDOUT} = 3.3 V)			±12	mA
	Output current (V_{DDOUT} = 2.5 V)			±10	
	Output current (V_{DDOUT} = 1.8 V)			±8	
C_L	Output load LVCMOS			15	pF
T_A	Operating free-air temperature	–40		85	°C

RECOMMENDED CRYSTAL/VCXO SPECIFICATIONS(1)

		MIN	NOM	MAX	UNIT
f_{Xtal}	Crystal input frequency range (fundamental mode)	8	27	32	MHz
ESR	Effective series resistance			100	Ω
f_{PR}	Pulling range (0 V ≤ V_{Ctrl} ≤ 1.8 V)(2)	±120	±150		ppm
	Frequency control voltage, V_{Ctrl}	0		V_{DD}	V
C_0/C_1	Pullability ratio			220	
C_L	On-chip load capacitance at Xin and Xout	0		20	pF

(1) For more information about VCXO configuration, and crystal recommendation, see application report (SCAA085).
(2) Pulling range depends on crystal-type, on-chip crystal load capacitance and PCB stray capacitance; pulling range of min ±120 ppm applies for crystal listed in the application report (SCAA085).

EEPROM SPECIFICATION

		MIN	TYP	MAX	UNIT
EEcyc	Programming cycles of EEPROM	100	1000		cycles
EEret	Data retention	10			years

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load, and operating free-air temperature

			MIN	NOM	MAX	UNIT
CLK_IN REQUIREMENTS						
f_{CLK}	LVCMOS clock input frequency	PLL bypass mode	0		160	MHz
		PLL mode	8		160	
t_r / t_f	Rise and fall time CLK signal (20% to 80%)				3	ns
	Duty cycle CLK at V_{DD}/2		40%		60%	

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
SDA/SCL TIMING REQUIREMENTS (see Figure 12)						
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{su(START)}$	START setup time (SCL high before SDA low)	4.7		0.6		µs
$t_{h(START)}$	START hold time (SCL low after SDA low)	4		0.6		µs
$t_{w(SCLL)}$	SCL low-pulse duration	4.7		1.3		µs
$t_{w(SCLH)}$	SCL high-pulse duration	4		0.6		µs
$t_{h(SDA)}$	SDA hold time (SDA valid after SCL low)	0	3.45	0	0.9	µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
t_r	SCL/SDA input rise time		1000		300	ns
t_f	SCL/SDA input fall time		300		300	ns
$t_{su(STOP)}$	STOP setup time	4		0.6		µs
t_{BUS}	Bus free time between a STOP and START condition	4.7		1.3		µs

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
OVERALL PARAMETER							
I_{DD}	Supply current (see Figure 3)	All outputs off, f_{CLK} = 27 MHz, f_{VCO} = 135 MHz; f_{OUT} = 27 MHz	All PLLS on		11		mA
			Per PLL		9		
$I_{DD(OUT)}$	Supply current (see Figure 4 and Figure 5)	No load, all outputs on, f_{OUT} = 27 MHz	V_{DDOUT} = 3.3 V		1.3		mA
			V_{DDOUT} = 1.8 V		0.7		
$I_{DD(PD)}$	Power-down current. Every circuit powered down except SDA/SCL	f_{IN} = 0 MHz,	V_{DD} = 1.9 V		30		μA
$V_{(PUC)}$	Supply voltage V_{dd} threshold for power-up control circuit			0.85		1.45	V
f_{VCO}	VCO frequency range of PLL			80		230	MHz
f_{OUT}	LVCMOS output frequency	V_{DDOUT} = 3.3 V				230	MHz
		V_{DDOUT} = 1.8 V				230	
LVCMOS PARAMETER							
V_{IK}	LVCMOS input voltage	V_{DD} = 1.7 V; I_I = –18 mA				–1.2	V
I_I	LVCMOS Input current	V_I = 0 V or V_{DD}; V_{DD} = 1.9 V				±5	μA
I_{IH}	LVCMOS Input current for S0/S1/S2	V_I = V_{DD}; V_{DD} = 1.9 V				5	μA
I_{IL}	LVCMOS Input current for S0/S1/S2	V_I = 0 V; V_{DD} = 1.9 V				–4	μA
C_I	Input capacitance at Xin/Clk	V_{IClk} = 0 V or V_{DD}			6		pF
	Input capacitance at Xout	V_{IXout} = 0 V or V_{DD}			2		
	Input capacitance at S0/S1/S2	V_{IS} = 0 V or V_{DD}			3		
CDCE913 - LVCMOS PARAMETER FOR V_{DDOUT} = 3.3 V – MODE							
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 3 V, I_{OH} = –0.1 mA		2.9			V
		V_{DDOUT} = 3 V, I_{OH} = –8 mA		2.4			
		V_{DDOUT} = 3 V, I_{OH} = –12 mA		2.2			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 3 V, I_{OL} = 0.1 mA				0.1	V
		V_{DDOUT} = 3 V, I_{OL} = 8 mA				0.5	
		V_{DDOUT} = 3 V, I_{OL} = 12 mA				0.8	
t_{PLH}, t_{PHL}	Propagation delay	PLL bypass			3.2		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 3.3 V (20%–80%)			0.6		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(2) (3)	1 PLL switching, Y2-to-Y3			50	70	ps
$t_{jit(per)}$	Peak-to-peak period jitter(3)	1 PLL switching, Y2-to-Y3			60	100	ps
$t_{sk(o)}$	Output skew (4) , See Table 2	f_{OUT} = 50 MHz; Y1-to-Y3				60	ps
odc	Output duty cycle (5)	f_{VCO} = 100 MHz; Pdiv = 1		45%		55%	
CDCE913 – LVCMOS PARAMETER for V_{DDOUT} = 2.5 V – Mode							
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 2.3 V, I_{OH} = –0.1 mA		2.2			V
		V_{DDOUT} = 2.3 V, I_{OH} = –6 mA		1.7			
		V_{DDOUT} = 2.3 V, I_{OH} = –10 mA		1.6			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 2.3 V, I_{OL} = 0.1 mA				0.1	V
		V_{DDOUT} = 2.3 V, I_{OL} = 6 mA				0.5	
		V_{DDOUT} = 2.3 V, I_{OL} = 10 mA				0.7	
t_{PLH}, t_{PHL}	Propagation delay	PLL bypass			3.6		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 2.5 V (20%–80%)			0.8		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(2) (3)	1 PLL switching, Y2-to-Y3			50	70	ps
$t_{jit(per)}$	Peak-to-peak period jitter(3)	1 PLL switching, Y2-to-Y3			60	100	ps
$t_{sk(o)}$	Output skew(4) , See Table 2	f_{OUT} = 50 MHz; Y1-to-Y3				60	ps
odc	Output duty cycle(5)	f_{VCO} = 100 MHz; Pdiv = 1		45%		55%	

(1) All typical values are at respective nominal V_{DD}.
(2) 10000 cycles.
(3) Jitter depends on configuration. Jitter data is for input frequency = 27 MHz, f_{VCO} = 108 MHz, f_{OUT} = 27 MHz (measured at Y2).
(4) The tsk(o) specification is only valid for equal loading of each bank of outputs, and the outputs are generated from the same divider.
(5) odc depends on output rise and fall time (t_r/t_f); data sampled on rising edge (tr)

DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
CDCEL913 — LVCMOS PARAMETER for V_{DDOUT} = 1.8 V – Mode						
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 1.7 V, I_{OH} = –0.1 mA	1.6			V
		V_{DDOUT} = 1.7 V, I_{OH} = –4 mA	1.4			
		V_{DDOUT} = 1.7 V, I_{OH} = –8 mA	1.1			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 1.7 V, I_{OL} = 0.1 mA			0.1	V
		V_{DDOUT} = 1.7 V, I_{OL} = 4 mA			0.3	
		V_{DDOUT} = 1.7 V, I_{OL} = 8 mA			0.6	
t_{PLH}, t_{PHL}	Propagation delay	PLL bypass		2.6		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 1.8 V (20%–80%)		0.7		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter [(6)] [(7)]	1 PLL switching, Y2-to-Y3		80	110	ps
$t_{jit(per)}$	Peak-to-peak period jitter[(7)]	1 PLL switching, Y2-to-Y3		100	130	ps
$t_{sk(o)}$	Output skew[(8)] , See Table 2	f_{OUT} = 50 MHz; Y1-to-Y3			50	ps
odc	Output duty cycle[(9)]	f_{VCO} = 100 MHz; Pdiv = 1	45%		55%	
SDA/SCL PARAMETER						
V_{IK}	SCL and SDA input clamp voltage	V_{DD} = 1.7 V; I_I = –18 mA			–1.2	V
I_{IH}	SCL and SDA input current	V_I = V_{DD}; V_{DD} = 1.9 V			±10	μA
V_{IH}	SDA/SCL input high voltage[(10)]		0.7 V_{DD}			V
V_{IL}	SDA/SCL input low voltage[(10)]				0.3 V_{DD}	V
V_{OL}	SDA low-level output voltage	I_{OL} = 3 mA, V_{DD} = 1.7 V			0.2 V_{DD}	V
C_I	SCL/SDA Input capacitance	V_I = 0 V or V_{DD}		3	10	pF

(6) 10000 cycles.
(7) Jitter depends on configuration. Jitter data is for input frequency = 27 MHz, f_{VCO} = 108 MHz, f_{OUT} = 27 MHz (measured at Y2).
(8) The tsk(o) specification is only valid for equal loading of each bank of outputs, and the outputs are generated from the same divider.
(9) odc depends on output rise and fall time (t_r/t_f); data sampled on rising edge (tr)
(10) SDA and SCL pins are 3.3 V tolerant.

PARAMETER MEASUREMENT INFORMATION

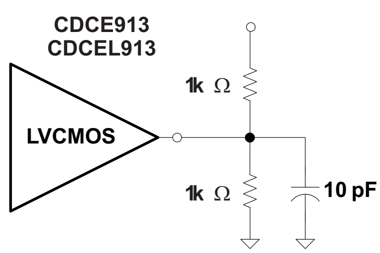


Figure 1. Test Load

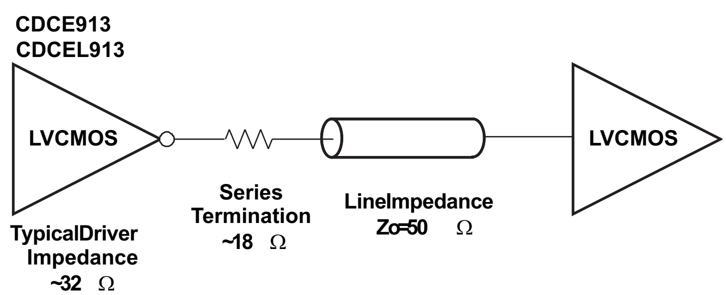


Figure 2. Test Load for 50-Ω Board Environment

TYPICAL CHARACTERISTICS

CDCE913, CDCEL913
SUPPLY CURRENT
vs
PLL FREQUENCY

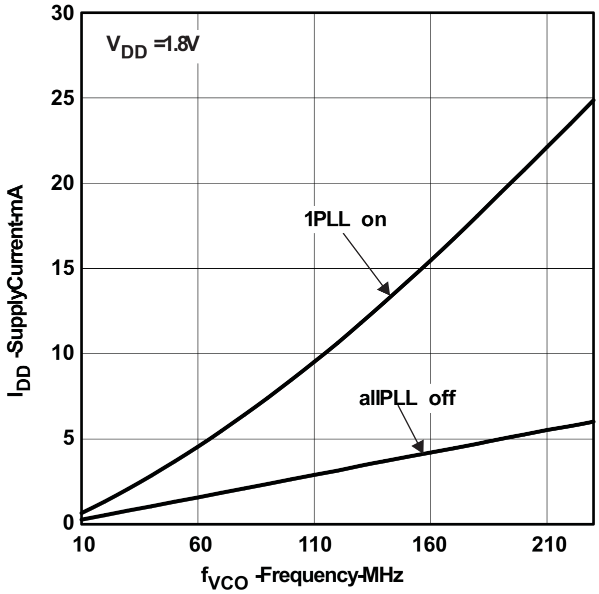


Figure 3.

CDCE913
OUTPUT CURRENT
vs
OUTPUT FREQUENCY

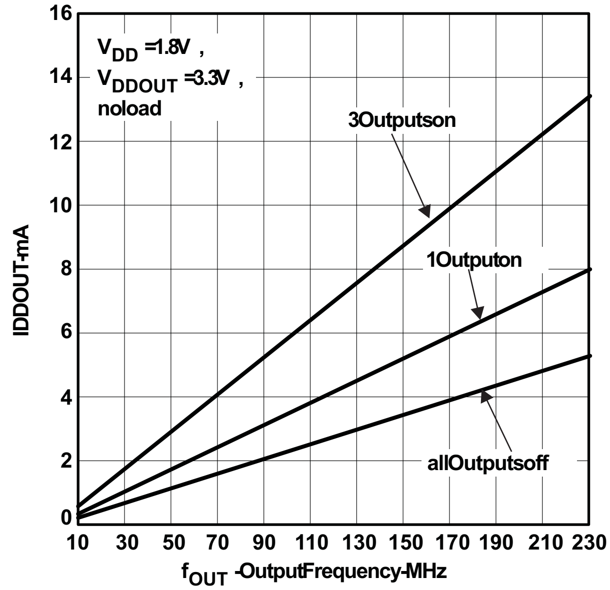


Figure 4.

CDCEL913
OUTPUT CURRENT
vs
OUTPUT FREQUENCY

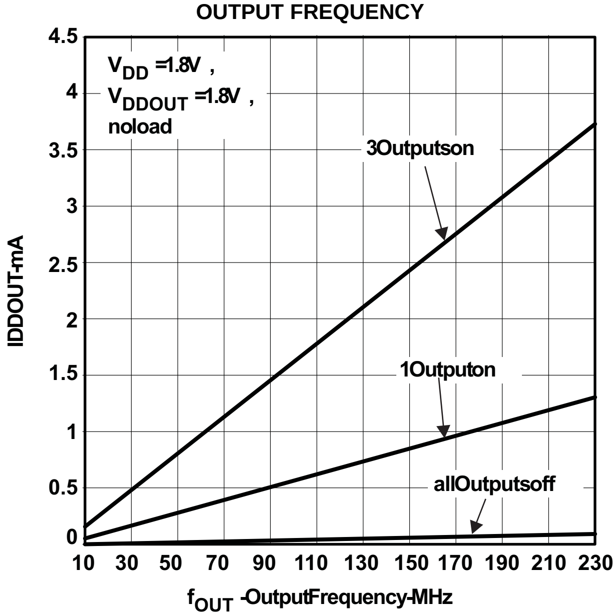


Figure 5.

APPLICATION INFORMATION

CONTROL TERMINAL CONFIGURATION

The CDCE913/CDCEL913 has three user-definable control terminals (S0, S1, and S2) which allow external control of device settings. They can be programmed to any of the following functions:

- Spread spectrum clocking selection → spread type and spread amount selection
- Frequency selection → switching between any of two user-defined frequencies
- Output state selection → output configuration and power down control

The user can predefine up to eight different control settings. Table 1 and Table 2 explain these settings.

Table 1. Control Terminal Definition

External Control Bits	PLL1 Setting			Y1Setting
Control Function	PLL Frequency Selection	SSC Selection	Output Y2/Y3 Selection	Output Y1 and Power-Down Selection

Table 2. PLLx Setting (can be selected for each PLL individual)(1)

SSC Selection (Center/Down)				
SSCx [3-bits]			Center	Down
0	0	0	0% (off)	0% (off)
0	0	1	±0.25%	–0.25%
0	1	0	±0.5%	–0.5%
0	1	1	±0.75%	–0.75%
1	0	0	±1.0%	–1.0%
1	0	1	±1.25%	–1.25%
1	1	0	±1.5%	–1.5%
1	1	1	±2.0%	–2.0%
FREQUENCY SELECTION(2)				
FSx		FUNCTION		
0		Frequency0		
1		Frequency1		
OUTPUT SELECTION(3) (Y2 ... Y3)				
YxYx		FUNCTION		
0		State0		
1		State1		

(1) Center/Down-Spread, Frequency0/1 and State0/1 are user-definable in PLLx Configuration Register;
(2) Frequency0 and Frequency1 can be any frequency within the specified f_{VCO} range.
(3) State0/1 selection is valid for both outputs of the corresponding PLL module and can be power down, 3-state, low or active

Table 3. Y1 Setting(1)

Y1 SELECTION	
Y1	FUNCTION
0	State 0
1	State 1

(1) State0 and State1 are user definable in Generic Configuration Register and can be power down, 3-state, low, or active.

S1/SDA and S2/SCL pins of the CDCE913/CDCEL913 are dual function pins. In default configuration they are defined as SDA/SCL for the serial programming interface. They can be programmed as control-pins (S1/S2) by setting the appropriate bits in the EEPROM. Note that the changes to the Control Register (Bit [**6**] of Byte **02h**) have no effect until they are written into the EEPROM.

Once they are set as control pins, the serial programming interface is no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporally act as serial programming pins (SDA/SCL).

S0 is **not** a multi use pin; it is a control pin only.

DEFAULT DEVICE CONFIGURATION

The internal EEPROM of CDCE913/CDCEL913 is pre-configured with a factory default configuration as shown in Figure 6 (The input frequency is passed through the output as a default).This allows the device to operate in default mode without the extra production step of programming it. The default setting appears after power is supplied or after power-down/up sequence until it is reprogrammed by the user to a different application configuration. A new register setting is programmed via the serial SDA/SCL Interface.

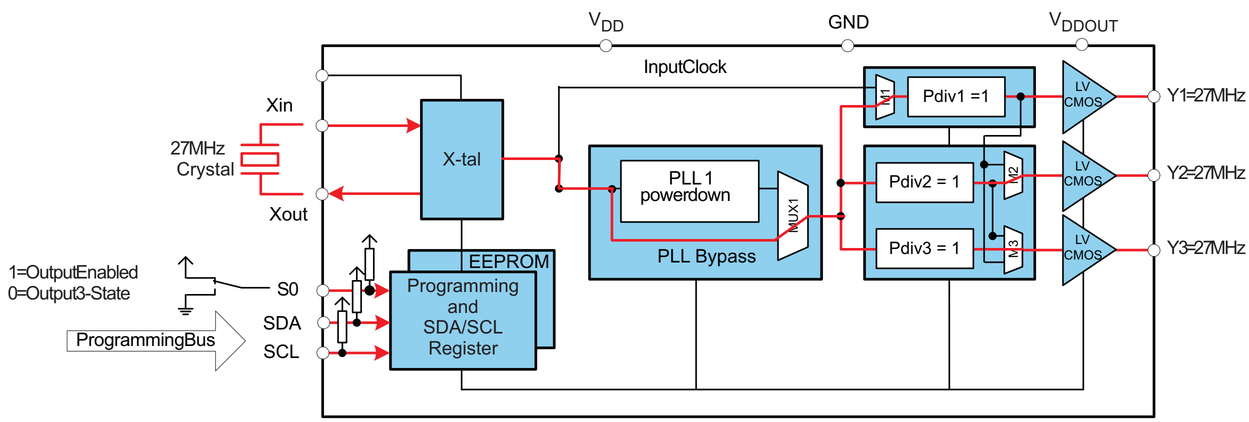


Figure 6. Default Configuration

Table 4 shows the factory default setting for the Control Terminal Register. Note that even though 8 different register settings are possible, in default configuration, only the first two settings (0 and 1) can be selected with S0, as S1 and S2 are configured as programming pins in default mode.

Table 4. Factory Default Setting for Control Terminal Register(1)

			Y1	PLL1 Settings		
External Control Pins			Output Selection	Frequency Selection	SSC Selection	Output Selection
S2	*S1*	**S0**	**Y1**	*FS1*	*SSC1*	**Y2Y3**
SCL (I2C)	SDA (I2C)	**0**	3-state	f_{VCO1_0}	off	**3-state**
SCL (I2C)	SDA (I2C)	**1**	**enabled**	f_{VCO1_0}	off	**enabled**

(1) In default mode or when programmed respectively, S1 and S2 act as serial programming interface, SDA/SCL. They do not have any control-pin function but they are internally interpreted as if S1=0 and S2=0. S0, however, is a control-pin which in the default mode switches all outputs ON or OFF (as previously predefined).

SDA/SCL SERIAL INTERFACE

The CDCE913/CDCEL913 operates as a slave device of the 2-wire serial SDA/SCL bus, compatible with the popular SMBus or I2C specification. It operates in the standard-mode transfer (up to 100kbit/s) and fast-mode transfer (up to 400kbit/s) and supports 7-bit addressing.

The S1/SDA and S2/SCL pins of the CDCE913/CDCEL913 are dual function pins. In the default configuration they are used as SDA/SCL serial programming interface. They can be re-programmed as general purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, Byte **02h**, Bit [**6**].

DATA PROTOCOL

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most significant bit first) with the ability to stop after any complete byte has been transferred. The numbers of Bytes read-out are defined by Byte Count in the Generic Configuration Register. At Block Read instruction, all bytes defined in the Byte Count must be readout to correctly finish the read cycle.

Once a byte has been sent, it is written into the internal register and is effective immediately. This applies to each transferred byte regardless of whether this is a *Byte Write* or a *Block Write* sequence.

If the EEPROM Write Cycle is initiated, the internal SDA registers are written into the EEPROM. During this Write Cycle, data is not accepted at the SDA/SCL bus until the write cycle is completed. However, data can be read out during the programming sequence (Byte Read or Block Read). The programming status can be monitored by *EEPIP*, byte 01h–bit 6.

The offset of the indexed byte is encoded in the command code, as described in Table 5.

Table 5. Slave Receiver Address (7 Bits)

DEVICE	A6	A5	A4	A3	A2	A1 (1)	A0 (1)	R/$\overline{W}$
CDCE913/CDCEL913	**1**	**1**	**0**	**0**	**1**	**0**	**1**	**1/0**
CDCE925/CDCEL925	1	1	0	0	1	0	0	1/0
CDCE937/CDCEL937	1	1	0	1	1	0	1	1/0
CDCE949/CDCEL949	1	1	0	1	1	0	0	1/0

(1) Address bits A0 and A1 are programmable via the SDA/SCL bus (byte **01**, bit [**1:0**]. This allows addressing up to 4 devices connected to the same SDA/SCL bus. The least-significant bit of the address byte designates a write or read operation.

COMMAND CODE DEFINITION

Table 6. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Byte Offset for *Byte Read*, *Block Read*, *Byte Write* and *Block Write* operation.

Generic Programming Sequence

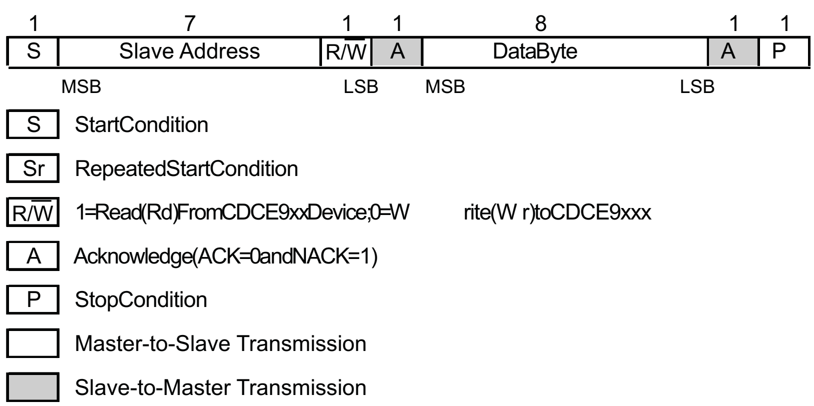


Figure 7. Generic Programming Sequence

Byte Write Programming Sequence

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	CommandCode	A	DataByte	A	P

Figure 8. Byte Write Protocol

Byte Read Programming Sequence

1	7	1	1	8	1	1	7	1	1
S	Slave Address	Wr	A	CommandCode	A	S	Slave Address	Rd	A

8	1	1
DataByte	A	P

Figure 9. Byte Read Protocol

Block Write Programming Sequence

1	7	1	1	8	1	8	1
S	Slave Address	Wr	A	CommandCode	A	ByteCount=N	A

8	1	8	1		8	1	1
DataByte0	A	DataByte1	A	…	DataByteN-1	A	P

(1) Data byte 0 bits [7:0] is reserved for Revision Code and Vendor Identification. Also, it is used for internal test purpose and should not be overwritten.

Figure 10. Block Write Protocol

Block Read Programming Sequence

1	7	1	1	8	1	1	7	1	1
S	Slave Address	Wr	A	CommandCode	A	Sr	Slave Address	Rd	A

8	1	8	1		8	1	1
ByteCountN	A	DataByte0	A	…	DataByteN-1	A	P

Figure 11. Block Read Protocol

Timing Diagram for the SDA/SCL Serial Control Interface

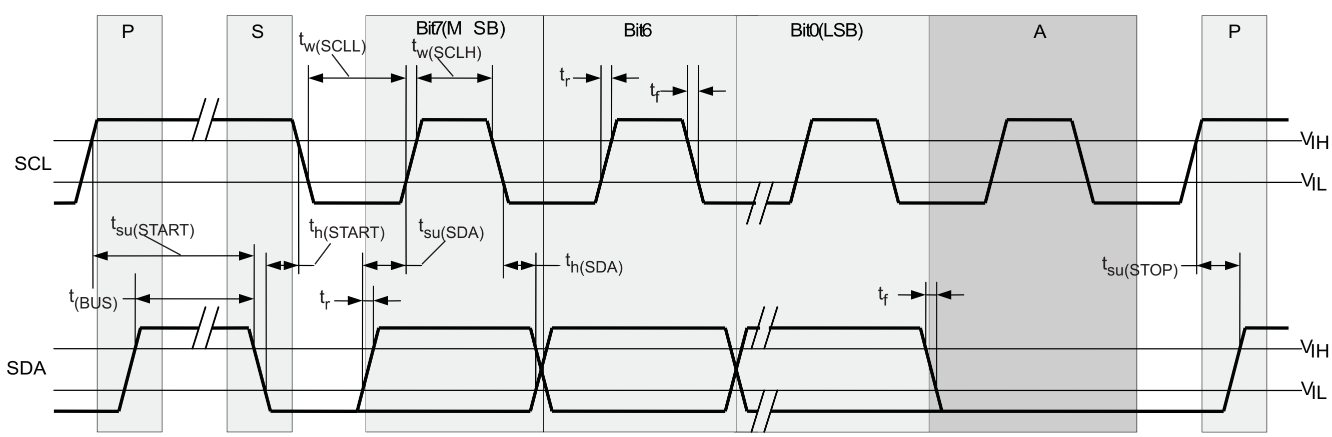


Figure 12. Timing Diagram for SDA/SCL Serial Control Interface

SDA/SCL HARDWARE INTERFACE

Figure 13 shows how the CDCE913/CDCEL913 clock synthesizer is connected to the SDA/SCL serial interface bus. Multiple devices can be connected to the bus but the speed may need to be reduced (400 kHz is the maximum) if many devices are connected.

Note that the pullup resistors (R_P) depends on the supply voltage, bus capacitance, and number of connected devices. The recommended pullup value is 4.7 kΩ. It must meet the minimum sink current of 3 mA at V_{OL}max = 0.4 V for the output stages (for more details see the SMBus or I^2C™ Bus specification).

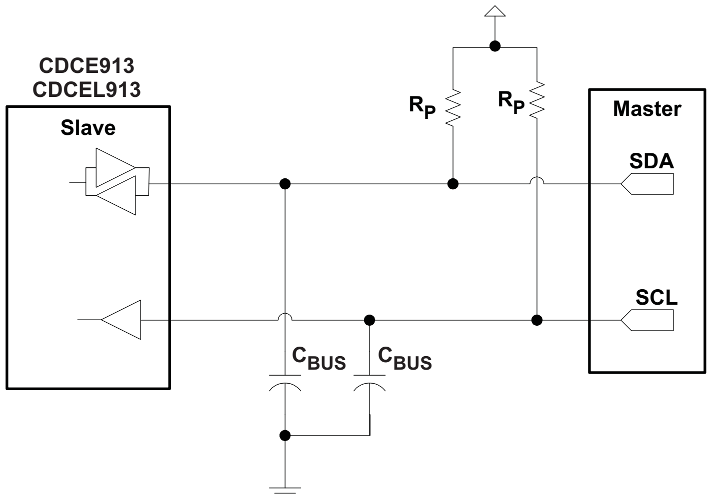


Figure 13. SDA / SCL Hardware Interface

SDA/SCL CONFIGURATION REGISTERS

The clock input, control pins, PLLs, and output stages are user configurable. The following tables and explanations describe the programmable functions of the CDCE913/CDCEL913. All settings can be manually written into the device via the SDA/SCL bus or easily programmed by using the TI Pro-Clock™ software. TI Pro-Clock™ software allows the user to quickly make all settings and automatically calculates the values for optimized performance at lowest jitter.

Table 7. SDA/SCL Registers

Address Offset	Register Description	Table
00h	Generic Configuration Register	Table 9
10h	PLL1 Configuration Register	Table 10

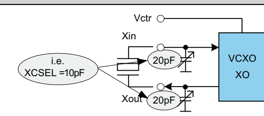
The grey-highlighted bits, described in the Configuration Registers tables in the following pages, belong to the Control Terminal Register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2. See the Control Terminal Configuration section.

Table 8. Configuration Register, External Control Terminals

				Y1	PLL1 Settings		
	External Control Pins			Output Selection	Frequency Selection	SSC Selection	Output Selection
	S2	S1	S0	Y1	FS1	SSC1	Y2Y3
0	0	0	0	Y1_0	FS1_0	SSC1_0	Y2Y3_0
1	0	0	1	Y1_1	FS1_1	SSC1_1	Y2Y3_1
2	0	1	0	Y1_2	FS1_2	SSC1_2	Y2Y3_2
3	0	1	1	Y1_3	FS1_3	SSC1_3	Y2Y3_3
4	1	0	0	Y1_4	FS1_4	SSC1_4	Y2Y3_4
5	1	0	1	Y1_5	FS1_5	SSC1_5	Y2Y3_5
6	1	1	0	Y1_6	FS1_6	SSC1_6	Y2Y3_6
7	1	1	1	Y1_7	FS1_7	SSC1_7	Y2Y3_7
	Address Offset(1)			04h	13h	10h–12h	15h

(1) Address Offset refers to the byte address in the Configuration Register in Table 9 and Table 10.

Table 9. Generic Configuration Register

Offset[(1)]	Bit[(2)]	Acronym	Default[(3)]	Description
00h	7	E_EL	Xb	Device identification (read-only): 1 is CDCE913 (3.3 V out), 0 is CDCEL913 (1.8 V out)
	6:4	RID	Xb	Revision Identification Number (read only)
	3:0	VID	1h	Vendor Identification Number (read only)
01h	7	–	0b	Reserved – always write 0
	6	EEPIP	0b	EEPROM Programming Status4:[(4)] (read only) — 0 – EEPROM programming is completed 1 – EEPROM is in programming mode
	5	EELOCK	0b	Permanently Lock EEPROM Data[(5)] — 0 – EEPROM is not locked 1 – EEPROM will be permanently locked
	4	PWDN	0b	Device Power Down (overwrites S0/S1/S2 setting; configuration register settings are unchanged) Note: PWDN cannot be set to 1 in the EEPROM. 0 – device active (PLL1 and all outputs are enabled) 1 – device power down (PLL1 in power down and all outputs in 3-state)
	3:2	INCLK	00b	Input clock selection: 00 – Xtal; 10 – LVCMOS; 01 – VCXO; 11 – reserved
	1:0	SLAVE_ADR	01b	Address Bits A0 and A1 of the Slave Receiver Address
02h	7	M1	1b	Clock source selection for output Y1: 0 – input clock; 1 – PLL1 clock
	6	SPICON	0b	Operation mode selection for pin 12/13[(6)] 0 – serial programming interface SDA (pin 13) and SCL (pin 12) 1 – control pins S1 (pin 13) and S2 (pin 12)
	5:4	Y1_ST1	11b	Y1-State0/1 Definition 00 – device power down (all PLLs in power down and all outputs in 3-State) 01 – Y1 disabled to 3-state 10 – Y1 disabled to low 11 – Y1 enabled
	3:2	Y1_ST0	01b	
	1:0	Pdiv1 [9:8]	001h	10-Bit Y1-Output-Divider Pdiv1: 0 – divider reset and stand-by 1-to-1023 – divider value
03h	7:0	Pdiv1 [7:0]		
04h	7	Y1_7	0b	Y1_x State Selection[(7)] — 0 – State0 (predefined by Y1_ST0) 1 – State1 (predefined by Y1_ST1)
	6	Y1_6	0b	
	5	Y1_5	0b	
	4	Y1_4	0b	
	3	Y1_3	0b	
	2	Y1_2	0b	
	1	Y1_1	1b	
	0	Y1_0	0b	
05h	7:3	XCSEL	0Ah	Crystal Load Capacitor Selection[(8)] — 00h → 0 pF 01h → 1 pF 02h → 2 pF :14h-to-1Fh → 20 pF 
	2:0		0b	Reserved – do not write other than 0

(1) Writing data beyond ‘20h’ may affect device function.
(2) All data transferred with the MSB first.
(3) Unless customer-specific setting.
(4) During EEPROM programming, no data is allowed to be sent to the device via the SDA/SCL bus until the programming sequence is completed. Data, however, can be read out during the programming sequence (Byte Read or Block Read).
(5) If this bit is set to high in the EEPROM, the actual data in the EEPROM is permanently locked. No further programming is possible. Data, however can still be written via SDA/SCL bus to the internal register to change device function on the fly. But new data can no longer be saved to the EEPROM. EELOCK is effective only, if written into the EEPROM.
(6) Selection of “control pins” is effective only if written into the EEPROM. Once written into the EEPROM, the serial programming pins are no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporally act as serial programming pins (SDA/SCL), and the two slave receiver address bits are reset to A0=”0” and A1=“0”.
(7) These are the bits of the Control Terminal Register (see Table 8). The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2.
(8) The internal load capacitor (C1, C2) has to be used to achieve the best clock performance. External capacitors should be used only to finely adjust CL by a few picofarads. The value of CL can be programmed with a resolution of 1 pF for a crystal load range of 0 pF to 20 pF. For CL > 20 pF, use additional external capacitors. Also, the value of the device input capacitance has to be considered which always adds 1.5 pF (6 pF//2 pF) to the selected CL. For more information about VCXO configuration and crystal recommendation, see application report SCAA085.

Table 9. Generic Configuration Register (continued)

Offset(1)	Bit(2)	Acronym	Default(3)	Description	
06h	7:1	BCOUNT	20h	7-Bit Byte Count (defines the number of bytes which will be sent from this device at the next Block Read transfer); all bytes have to be read out to correctly finish the read cycle.	
	0	EEWRITE	0b	Initiate EEPROM Write Cycle (4) (9)	0– no EEPROM write cycle 1 – start EEPROM write cycle (internal register are saved to the EEPROM)
07h-0Fh		—	0h	Unused address range	

(9) The EEPROM WRITE bit must be sent last. This ensures that the content of all internal registers are stored in the EEPROM. The EEWRITE cycle is initiated with the rising edge of the EEWRITE bit. A static level high does not trigger an EEPROM WRITE cycle. The EEWRITE bit has to be reset to low after the programming is completed. The programming status can be monitored by reading out EEPIP. If EELOCK is set to high, no EEPROM programming is possible.

Table 10. PLL1 Configuration Register

OFFSET(1)	Bit(2)	Acronym	Default(3)	DESCRIPTION	
10h	7:5	SSC1_7 [2:0]	000b	SSC1: PLL1 SSC Selection (Modulation Amount)(4) **Down** 000 (off) 001 – 0.25% 010 – 0.5% 011 – 0.75% 100 – 1.0% 101 – 1.25% 110 – 1.5% 111 – 2.0%	**Center** 000 (off) 001 ± 0.25% 010 ± 0.5% 011 ± 0.75% 100 ± 1.0% 101 ± 1.25% 110 ± 1.5% 111 ± 2.0%
	4:2	SSC1_6 [2:0]	000b		
	1:0	SSC1_5 [2:1]	000b		
11h	7	SSC1_5 [0]			
	6:4	SSC1_4 [2:0]	000b		
	3:1	SSC1_3 [2:0]	000b		
	0	SSC1_2 [2]	000b		
12h	7:6	SSC1_2 [1:0]			
	5:3	SSC1_1 [2:0]	000b		
	2:0	SSC1_0 [2:0]	000b		
13h	7	FS1_7	0b	FS1_x: PLL1 Frequency Selection (4) 0 – f_{VCO1_0} (predefined by PLL1_0 – Multiplier/Divider value) 1 – f_{VCO1_1} (predefined by PLL1_1 – Multiplier/Divider value)	
	6	FS1_6	0b		
	5	FS1_5	0b		
	4	FS1_4	0b		
	3	FS1_3	0b		
	2	FS1_2	0b		
	1	FS1_1	0b		
	0	FS1_0	0b		
14h	7	MUX1	1b	PLL1 Multiplexer:	0 – PLL1 1 – PLL1 Bypass (PLL1 is in power down)
	6	M2	1b	Output Y2 Multiplexer:	0 – Pdiv1 1 – Pdiv2
	5:4	M3	10b	Output Y3 Multiplexer:	00 – Pdiv1-Divider 01 – Pdiv2-Divider 10 – Pdiv3-Divider 11 – reserved
	3:2	Y2Y3_ST1	11b	Y2, Y3-State0/1definition:	00 – Y2/Y3 disabled to 3-State (PLL1 is in power down) 01 – Y2/Y3 disabled to 3-State 10–Y2/Y3 disabled to low 11 – Y2/Y3 enabled
	1:0	Y2Y3_ST0	01b		
15h	7	Y2Y3_7	0b	Y2Y3_x Output State Selection (4) 0 – state0 (predefined by Y2Y3_ST0) 1 – state1 (predefined by Y2Y3_ST1)	
	6	Y2Y3_6	0b		
	5	Y2Y3_5	0b		
	4	Y2Y3_4	0b		
	3	Y2Y3_3	0b		
	2	Y2Y3_2	0b		
	1	Y2Y3_1	1b		
	0	Y2Y3_0	0b		

(1) Writing data beyond 20h may adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 10. PLL1 Configuration Register (continued)

OFFSET(1)	Bit(2)	Acronym	Default(3)	DESCRIPTION	
16h	7	SSC1DC	0b	PLL1 SSC down/center selection:	0 – down 1 – center
	6:0	Pdiv2	01h	7-Bit Y2-Output-Divider Pdiv2:	0 – reset and stand-by 1-to-127 is divider value
17h	7	—	0b	Reserved – do not write others than 0	
	6:0	Pdiv3	01h	7-Bit Y3-Output-Divider Pdiv3:	0 – reset and stand-by 1-to-127 is divider value
18h	7:0	PLL1_0N [11:4]	004h	PLL1_0(5): 30-Bit Multiplier/Divider value for frequency f_{VCO1_0} (for more information, see paragraph *PLL Multiplier/Divider Definition*).	
19h	7:4	PLL1_0N [3:0]			
	3:0	PLL1_0R [8:5]	000h		
1Ah	7:3	PLL1_0R[4:0]			
	2:0	PLL1_0Q [5:3]	10h		
1Bh	7:5	PLL1_0Q [2:0]			
	4:2	PLL1_0P [2:0]	010b		
	1:0	VCO1_0_RANGE	00b	f_{VCO1_0} range selection:	00 – f_{VCO1_0} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_0} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_0} < 175 MHz 11 – f_{VCO1_0} ≥ 175 MHz
1Ch	7:0	PLL1_1N [11:4]	004h	PLL1_1(5): 30-Bit Multiplier/Divider value for frequency f_{VCO1_1} (for more information see paragraph *PLL Multiplier/Divider Definition*)	
1Dh	7:4	PLL1_1N [3:0]			
	3:0	PLL1_1R [8:5]	000h		
1Eh	7:3	PLL1_1R[4:0]			
	2:0	PLL1_1Q [5:3]	10h		
1Fh	7:5	PLL1_1Q [2:0]			
	4:2	PLL1_1P [2:0]	010b		
	1:0	VCO1_1_RANGE	00b	f_{VCO1_1} range selection:	00 – f_{VCO1_1} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_1} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_1} < 175 MHz 11 – f_{VCO1_1} ≥ 175 MHz

(5) PLL settings limits: 16≤q≤63, 0≤p≤7, 0≤r≤511, 0<N<4096

PLL Multiplier/Divider Definition

At a given input frequency (f_{IN}), the output frequency (f_{OUT}) of the CDCE913/CDCEL913 can be calculated:

$$f_{OUT} = \frac{f_{IN}}{Pdiv} \times \frac{N}{M} \quad (1)$$

where

M (1 to 511) and N (1 to 4095) are the multiplier/divide values of the PLL; Pdiv (1 to 127) is the output divider.

The target VCO frequency (f_{VCO}) of each PLL can be calculated:

$$f_{VCO} = f_{IN} \times \frac{N}{M} \quad (2)$$

The PLL internally operates as fractional divider and needs the following multiplier/divider settings:

- N
- $P = 4 - \text{int}\left(\log_2 \frac{N}{M}\right)$ [if $P < 0$ then $P = 0$]
- $Q = \text{int}\left(\frac{N'}{M}\right)$
- $R = N' - M \times Q$

where

$N' = N \times 2^P$;
$N \geq M$;
100 MHz < f_{VCO} > 200 MHz;
$16 \leq q \leq 63$
$0 \leq p \leq 7$
$0 \leq r \leq 51$

Example:

for f_{IN} = 27 MHz; M = 1; N = 4; Pdiv = 2;
→ f_{OUT} = 54 MHz
→ f_{VCO} = 108 MHz
→ $P = 4 - \text{int}(\log_2 4) = 4 - 2 = 2$
→ $N'' = 4 \times 2^2 = 16$
→ Q = int(16) = 16
→ R = 16 – 16 = 0

for f_{IN} = 27 MHz; M = 2; N = 11; Pdiv = 2;
→ f_{OUT} = 74.25 MHz
→ f_{VCO} = 148.50 MHz
→ $P = 4 - \text{int}(\log_2 5.5) = 4 - 2 = 2$
→ $N'' = 11 \times 2^2 = 44$
→ Q = int(22) = 22
→ R = 44 – 44 = 0

The values for P, Q, R, and N’ are automatically calculated when using TI Pro-Clock™ software.

REVISION HISTORY

Changes from Revision B (December 2007) to Revision C **Page**

- Added SDA and SCL can go up to 3.6V as stated in the Recommended Operating Conditions table 3
- Deleted 230 value, moved to Max 6
- Deleted 230 value, moved to Max 6

Changes from Revision C (September) to Revision D **Page**

- Deleted sentence - A different default setting can be programmed upon customer request. Contact Texas Instruments sales or marketing representative for more information. 10

Changes from Revision D (October 2009) to Revision E **Page**

- Added PLL settings limits: 16≤q≤63, 0≤p≤7, 0≤r≤511, 0<N<4096 foot to PLL1 Configure Register Table 17
- Added PLL settings limits: 16≤q≤63, 0≤p≤7, 0≤r≤511 to PLL Multiplier/Divider Definition Section 18

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CDCE913PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCE913PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCE913PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCE913PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCEL913PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCEL913PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCEL913PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCEL913PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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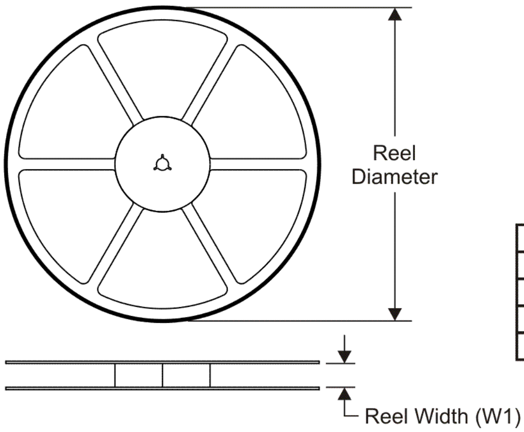
OTHER QUALIFIED VERSIONS OF CDCEL913 :
- Automotive: CDCEL913-Q1

NOTE: Qualified Version Definitions:

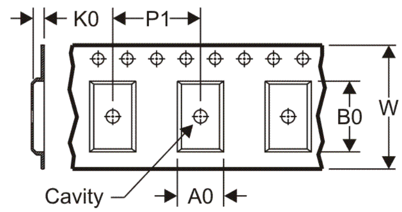
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

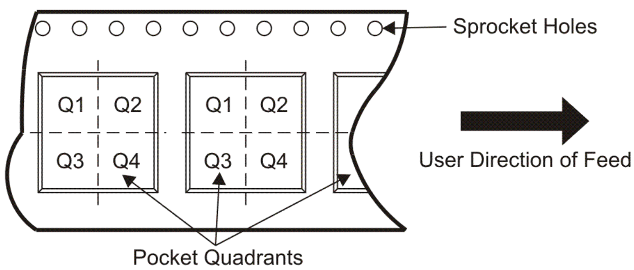


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

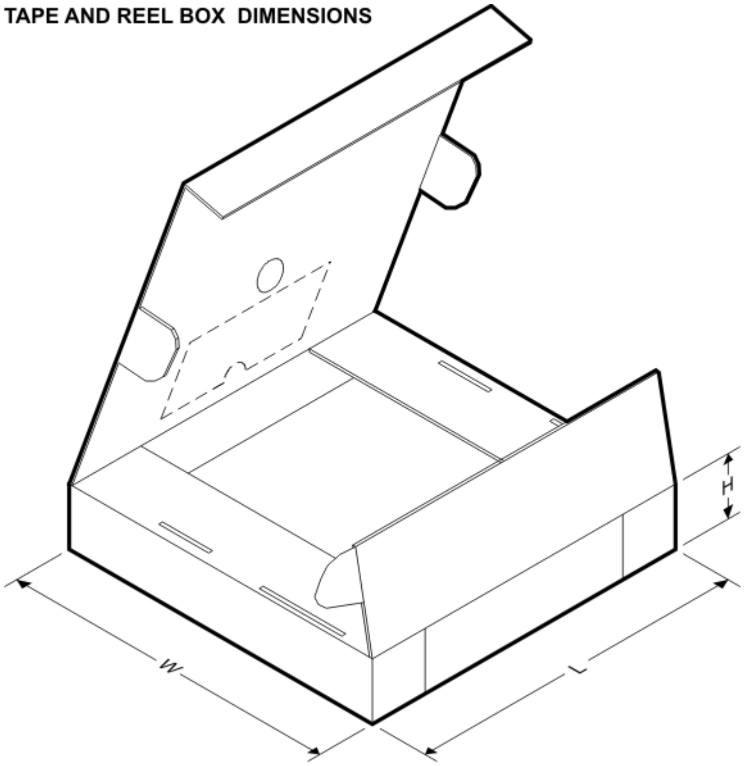
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE913PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CDCEL913PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

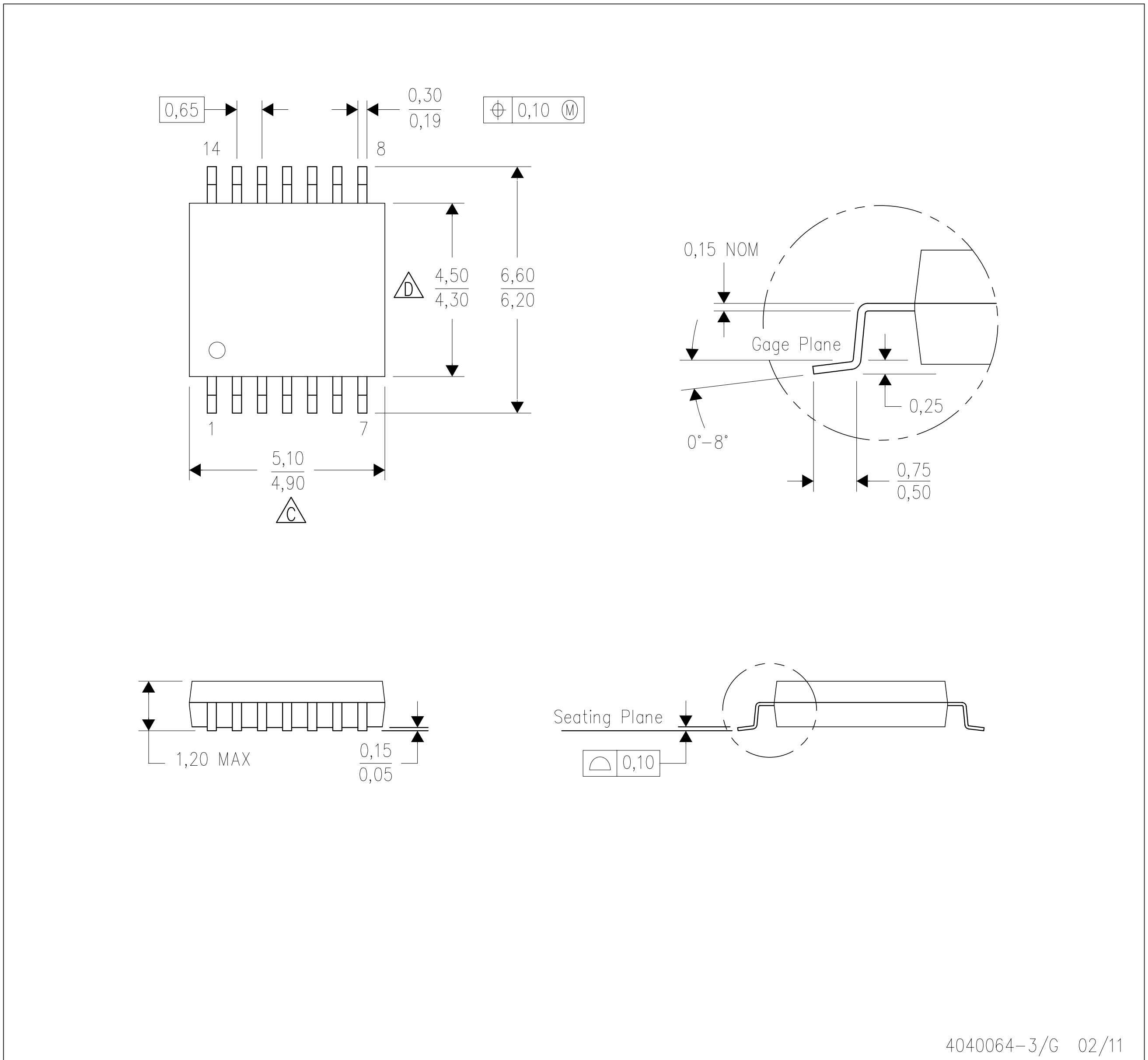
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

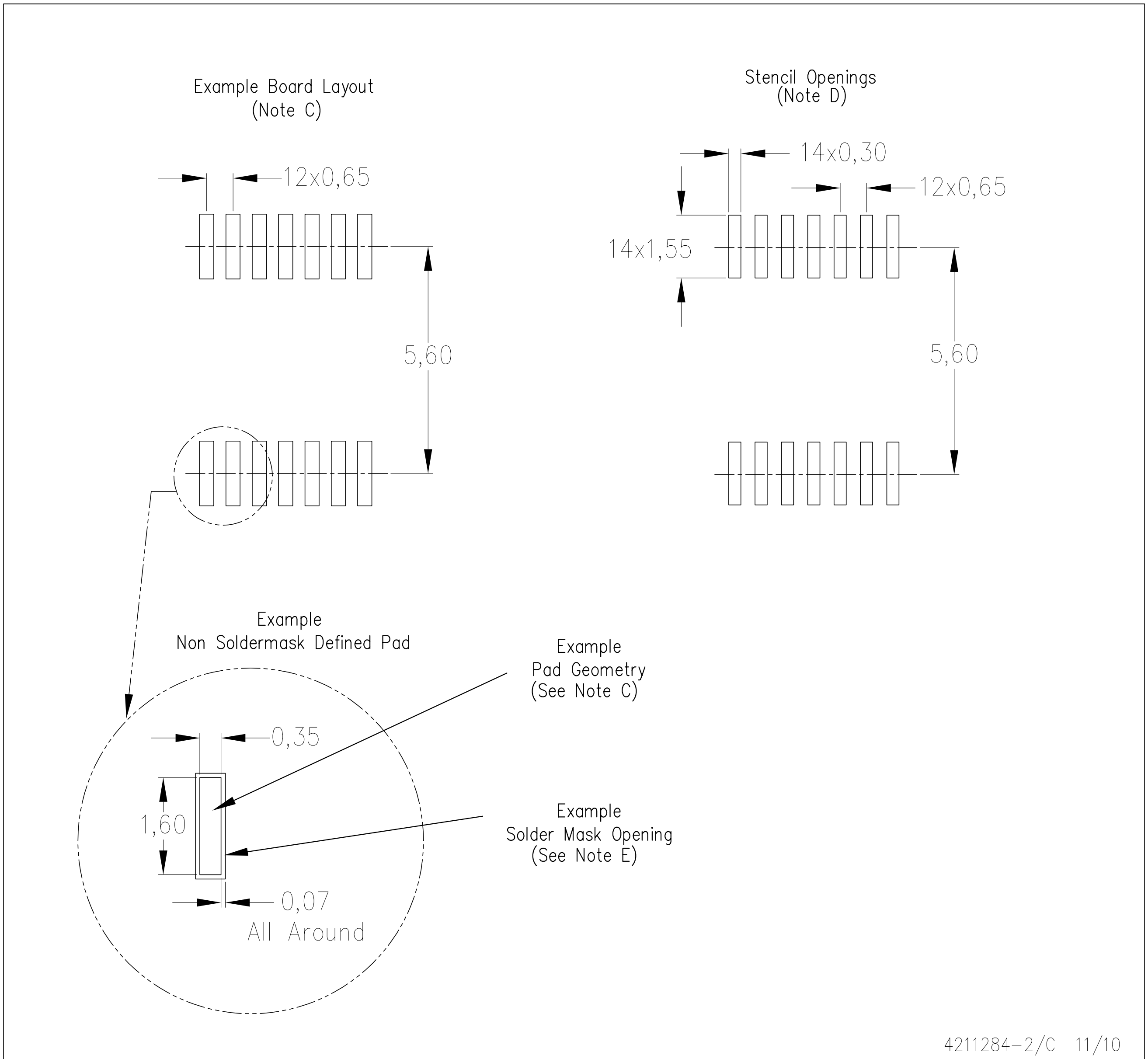
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE913PWR	TSSOP	PW	14	2000	346.0	346.0	29.0
CDCEL913PWR	TSSOP	PW	14	2000	346.0	346.0	29.0

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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