National Semiconductor

MICROCIRCUIT DATA SHEET

MJCD4001A-X REV 1A0

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QUAD 2-INPUT NOR GATE

General Description

These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors.

All inputs are protected against static discharge with diodes to Vdd and Vss.

Industry Part Number

CD4001A

NS Part Numbers

JM4001ABCA

Prime Die

CD4001B

Controlling Document

38510/05202, amend. #3

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

(Absolute Maximum Ratings)
(Note 1, 2)

Voltage at Any Pin	-0.5V to Vdd +0.5V
Power Dissipation (Pd)	200mW
Vdd Range	-0.5V to +15.5V
Storage Temperature (Ts)	-65C to +150C
Lead Temperature (Soldering, 10 seconds)	300C
Input Current (each input)	± 10mA
Thermal Resistance, junction to case	See MIL-STD-1835
Maximum Junction Temperature (Tj max)	175C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
Note 2: All voltages measured with respect to Vss unless otherwise specified.

Recommended Operating Conditions

Supply Voltage (VDD)	4.5V to 12.5V
Operating Temperature Range	-55C to +125C
Input Low Voltage Range (VIL)	
VDD=5.0V	0V to 0.85V
VDD=10.0V	0V to 2.0V
VDD=12.5V	0V to 2.1V
Input High Voltage Range (VIH)	
VDD=5.0V	3.95V to 5.0V
VDD=10.0V	8.0V to 10.0V
VDD=12.5V	10.0V to 12.5V

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vic+	Input Clamping Voltage (positive)	VDD=0.0V, IIN = 1mA	5, 6	INPUTS		1.5	V	1
Vic-	Input Clamping Voltage (negative)	VDD=Open, IIN= -1mA	5, 6	INPUTS		-6.0	V	1
IIH	Input High Current	VDD=15.0V, VM=15.0V (each input measured separately)	3, 4	INPUTS		100.0	nA	1, 2
IIL	Input Low Current	VDD=15.0V, VM=0.0V (each input measured separately)	3, 4	INPUTS		-100.0	nA	1, 2
ISS	Power Supply Current	VDD=15.0V, VINH=15.0V (one input per gate, others at 0.0V)	3, 4	VSS		-25.0	nA	1
			3, 4	VSS		-750.0	nA	2
		VDD=15.0V, VINL= 0.0V (all inputs)	3, 4	VSS		-25	nA	1
			3, 4	VSS		-750	nA	2
VOH1	Output High Voltage	VDD=4.5V, VIL=1.1V, IOH= -0.10mA	1, 2	OUTPUTS	2.5		V	1
		VDD=4.5V, VIL=0.85V, IOH= -0.10mA	1, 2	OUTPUTS	2.5		V	2
		VDD=4.5V, VIL=1.35V, IOH= -0.10mA	1, 2	OUTPUTS	2.5		V	3
VOH2	Output High Voltage	VDD=5.0V, VIL=1.1V, IOH= -0.20mA	1, 2	OUTPUTS	4.2		V	1
		VDD=5.0V, VIL=0.85V, IOH= -0.13mA	1, 2	OUTPUTS	4.2		V	2
		VDD=5.0V, VIL=1.35V, IOH= -0.25mA	1, 2	OUTPUTS	4.2		V	3
VOH3	Output High Voltage	VDD=5.0V, VIL=1.1V, IOH= -0.0mA	1, 2	OUTPUTS	4.95		V	1
		VDD=5.0V, VIL=0.85V, IOH= -0.0mA	1, 2	OUTPUTS	4.95		V	2
		VDD=5.0V, VIL=1.35V, IOH= -0.0mA	1, 2	OUTPUTS	4.95		V	3
VOH4	Output High Voltage	VDD=12.5V, VIL=2.50V, IOH= -0.0mA	1, 2	OUTPUTS	11.25		V	1
		VDD=12.5V, VIL=2.20V, IOH= -0.0mA	1, 2	OUTPUTS	11.25		V	2
		VDD=12.5V, VIL=2.65V, IOH= -0.0mA	1, 2	OUTPUTS	11.25		V	3
VOL1	Output Low Voltage	VDD=5.5V, VIH=3.80V, IOL=0.23mA	1, 2	OUTPUTS		0.4	V	1
		VDD=5.5V, VIH=3.65V, IOL=0.23mA	1, 2	OUTPUTS		0.5	V	2
		VDD=5.5V, VIH=3.95V, IOL=0.23mA	1, 2	OUTPUTS		0.4	V	3
VOL2	Output Low Voltage	VDD=5.0V, VIH=3.80V, IOL=0.40mA	1, 2	OUTPUTS		0.7	V	1
		VDD=5.0V, VIH=3.65V, IOL=0.28mA	1, 2	OUTPUTS		0.7	V	2
		VDD=5.0V, VIH=3.95V, IOL=0.50mA	1, 2	OUTPUTS		0.7	V	3

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VOL3	Output Low Voltage	VDD=5.0V, VIH=3.80V, IOL=0.0mA	1, 2	OUTPUTS		0.05	V	1
		VDD=5.0V, VIH=3.65V, IOL=0.0mA	1, 2	OUTPUTS		0.05	V	2
		VDD=5.0V, VIH=3.95V, IOL=0.0mA	1, 2	OUTPUTS		0.05	V	3
VOL4	Output Low Voltage	VDD=12.5V, VIH=9.50V, IOL=0.0mA	1, 2	OUTPUTS		1.25	V	1
		VDD=12.5V, VIH=9.25V, IOL=0.0mA	1, 2	OUTPUTS		1.25	V	2
		VDD=12.5V, VIH=9.75V, IOL=0.0mA	1, 2	OUTPUTS		1.25	V	3
VOL5	Output Low Voltage	VDD=5.0V, VIH=3.80V, IOL=0.80mA	1, 2	OUTPUTS		0.4	V	1
		VDD=5.0V, VIH=3.65V, IOL=0.56mA	1, 2	OUTPUTS		0.5	v	2
		VDD=5.0V, VIH=3.95V, IOL=1.00mA	1, 2	OUTPUTS		0.4	V	3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VDD=5.0V, CL=50pF, RL=200K Ohms to ground, Tr/Tf=10 ± 2ns.

tpHL	Propagation Delay Time		7, 8	In to On	13	210	nS	9, 11
			7, 8	In to On	18	315	nS	10
tpLH	Propagation Delay Time		7, 8	In to On	13	210	nS	9, 11
			7, 8	In to On	18	315	nS	10
tTHL	Transition Time		7, 8	On	10	300	nS	9, 11
			7, 8	On	14	450	nS	10
tTLH	Transition Time		7, 8	On	10	410	nS	9, 11
			7, 8	On	14	615	nS	10
Cin	Input Capacitance	VDD=Gnd, f=1MHz	10	INPUTS		12	pF	4

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Delta calculations performed at production burn-in and Group C (operational life test).

ISS	Power Supply Current	VDD=15.0V, VINH=15.0V (one input per gate, others at 0.0V)	12	VSS	-10.0	10.0	nA	1
		VDD=15.0V, VINL=0.0V (all inputs)	12	VSS	-10.0	10.0	nA	1
VOL1	Output Low Voltage	VDD=5.5V, VIH=3.8V, IOL=0.23ma	12	OUTPUTS	-0.04	0.04	V	1
VOH1	Output High Voltage	VDD=4.5V, VIL=1.1V, IOH= -0.10ma	12	OUTPUTS	-0.08	0.08	V	1

Note 1: Screen tested 100% on each device at +25C, +125C and -55C temperature, subgroups A1, 2 and 3.
Note 2: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C and -55C temperature, subgroups A1, 2 and 3.
Note 3: Screen tested 100% on each device at +25C and +125C temperature only, subgroup A1 and 2.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C and +125C temperature only, subgroup A1 and 2.
Note 5: Screen tested 100% on each device at +25C temperature only, subgroup A1.
Note 6: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C temperature only, subgroup A1.
Note 7: Screen tested 100% on each device at +25C temperature only, subgroup A9.
Note 8: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C and -55C temperature, subgroups A9, 10 and 11.
Note 9: VIL, VIH, IOL and IOH are guaranteed by applying specified conditions and testing VOL and VOH.
Note 10: Guaranteed parameter. This test is only performed during qualification.
Note 11: Guaranteed parameter, not tested.
Note 12: Drift values need not be calculated if post burn-in electrical test is performed within 24 hours after burn-in.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A0	M0003467	07/30/99	Linda Collins	1) Conversion from JRETS to MDS. Obsolete JRETS4001MX, rev. 2C. Release to MDS: MJCD4001A-X, rev. 1A0. 2) Change IIH limit from 1nA to 100nA. 3). Change ILL limit from -1nA to -100nA.