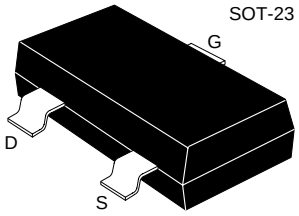
N-Channel JFET Switch

J111 - J113 / SST111 – SST113

FEATURES

- **Low Cost**
- **Automated Insertion Package**
- **Low Insertion Loss**
- **No Offset or Error Voltage Generated By Closed Switch**
  - **Purely Resistive**
  - **High Isolation Resistance From Driver**
- **Fast Switching**
- **Short Sample and Hold Aperture Time**

PIN CONFIGURATION



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PRODUCT MARKING (SOT-23)	
SST111	111
SST112	112
SST113	113

APPLICATIONS

- **Analog Switches**
- **Choppers**
- **Commutators**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Gate-Drain or Gate-Source Voltage . . . . . -35V
Gate Current 50mA
Storage Temperature Range . . . . . -55°C to +150°C
Operating Temperature Range . . . . . -55°C to +135°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Power Dissipation 360mW
Derate above 25°C . . . . . 3.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
J111-113	Plastic SOT-23	-55°C to +135°C
SST111-113	Plastic SOT-23	-55°C to +135°C

For Sorted Chips in Carriers see 2N4391 series.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	111			112			113			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSSR}	Gate Reverse Current (Note 1)			-1			-1			-1	nA	V_{DS} = 0V, V_{GS} = -15V	
$V_{GS(off)}$	Gate Source Cutoff Voltage	-3		-10	-1		-5	-0.5		-3	V	V_{DS} = 5V, I_D = 1µA	
BV_{GSS}	Gate Source Breakdown Voltage	-35			-35			-35				V_{DS} = 0V, I_G = -1µA	
I_{DSS}	Drain Saturation Current (Note 2)	20			5			2			mA	V_{DS} = 15V, V_{GS} = 0V	
$I_{D(off)}$	Drain Cutoff Current (Note 1)			1			1			1	nA	V_{DS} = 5V, V_{GS} = -10V	
$r_{DS(on)}$	Drain Source ON Resistance			30			50			100	Ω	V_{DS} = 0.1V, V_{GS} = 0V	
$C_{dg(off)}$	Drain Gate OFF Capacitance			5			5			5	pF	V_{DS} = 0, V_{GS} = -10V (Note 3)	f = 1MHz
$C_{sg(off)}$	Source Gate OFF Capacitance			5			5			5			
$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance			28			28			28		V_{DS} = V_{GS} = 0 (Note 3)	
$t_{d(on)}$	Turn On Delay Time		7			7			7		ns	Switching Time Test Conditions (Note 3)	
t_r	Rise Time		6			6			6				
$t_{d(off)}$	Turn Off Delay Time		20			20			20				
t_f	Fall Time		15			15			15				

	J111	J112	J113
V_{DD}	10V	10V	10V
$V_{GS(off)}$	-12V	-7V	-5V
R_L	0.8kΩ	1.6kΩ	3.2kΩ

NOTES: **1.** Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration 300µs; duty cycle ≤3%.
3. For design reference only, not 100% tested.

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