# ANALOG DEVICES

# Dual Bipolar/JFET, Precision Operational Amplifier

T-79-15 **OP-285***

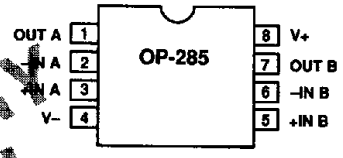


**FEATURES**
- Low Offset Voltage: 250 μV
- Wide Bandwidth: 8 MHz
- High Slew Rate: 20 V/μs
- Low Noise: 6 nV/√Hz
- Low Distortion: 0.001%
- Low Supply Current: 5 mA
- Low Offset Current: 2 nA
- Unity-Gain Stable

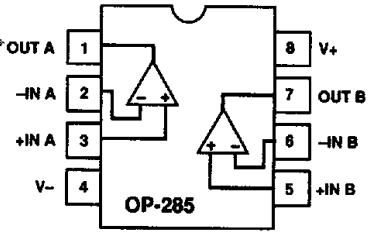
**APPLICATIONS**
- Active Filters
- Fast Amplifiers
- Integrators

**PIN CONNECTIONS**

8-Lead Narrow-Body SOIC
(S Suffix)




8-Lead Epoxy DIP
(P Suffix)






**GENERAL DESCRIPTION**

The OP-285 is a precision high speed amplifier featuring the Butler Amplifier front-end. This new front-end design combines the accuracy and low noise performance of bipolar transistors with the speed of JFETs. This yields an amplifier with high slew rates, low offset and good noise performance at low supply currents. Bias currents are also low compared to bipolar designs.

The OP-285 is specified over the extended industrial (−40°C to +85°C) temperature range. OP-285s are available in plastic DIP plus SO-8 surface mount packages.

*Patents pending.

T-79-15

# OP-285—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = ±15.0 V, $T_A$ = +25°C unless otherwise specified.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | | | 125 | 250 | µV |
| Input Bias Current | $I_B$ | $V_{CM}$ = 0 V | | 150 | | nA |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = 0 V | | 2 | | nA |
| Input Voltage Range | $V_{CM}$ | | −10.5 | | +10.5 | V |
| Common-Mode Rejection | CMR | $V_{CM}$ = ±10.5 V | 86 | | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 600 Ω | | 200 | | V/mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 5 | | µV/°C |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage Swing | $V_O$ | $R_L$ = 10 kΩ | −13 | ±14.1 | +13 | V |
| Open Loop Output Resistance | $R_{OUT}$ | | | | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_S$ = ± 4.5 V to ±15 V | | 80 | | dB |
| Supply Current | $I_{SY}$ | $V_O$ = 0 V, [illegible] | | 4 | 5 | mA |
| Supply Voltage Range | $V_S$ | | [illegible] | | ±18 | V |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | 20 | | V/µs |
| Full-Power Bandwidth | BWp | | | | | kHz |
| Settling Time | $t_S$ | | | | | µs |
| Gain Bandwidth Product | GBP | | | 8 | | MHz |
| Total Harmonic Distortion | THD | @ 20 kHz | | 0.002 | | % |
| | | @ 1 kHz | | 0.0006 | | % |
| Phase Margin | $\theta_0$ | | | 62 | | Degrees |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | $e_n$ p–p | 0.1 Hz to 10 Hz | | 1.1 | | µV p–p |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 6 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 1 kHz | | 1.5 | | pA/√Hz |

Specifications subject to change without notice.

## WAFER TEST LIMITS @ $V_S$ = ±15.0 V, $T_A$ = +25°C unless otherwise specified.)

| Parameter | Symbol | Conditions | Limit | Units |
|---|---|---|---|---|
| Offset Voltage | $V_{OS}$ | | 250 | mV max |
| Input Bias Current | $I_B$ | $V_{CM}$ = 0 V | 200 | nA max |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = 0 V | 50 | nA max |
| Input Voltage Range[1] | | | ±10.5 | V min |
| Common-Mode Rejection | CMRR | $V_{CM}$ = ±10.5 V | 86 | dB min |
| Power Supply Rejection Ratio | PSRR | V = ±4.5 V to ±15 V | 80 | dB min |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 10 kΩ | 100 | V/mV min |
| Output Voltage Range | $V_O$ | $R_L$ = 10 kΩ | ±13 | V min |
| Supply Current | $I_{SY}$ | $V_O$ = 0 V, $R_L$ = ∞ | 5 | mA max |

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.



### ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ± 18 V
Differential Input Voltage[2] . . . . . ±7.5
Output Short-Circuit Duration . . . . . Limited
Storage Temperature Range
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
OP-285E, F . . . . . −40°C to +85°C
Junction Temperature Range
P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec) . . . . . +300°C

| Package Type | $\theta_{JA}$[3] | $\theta_{JC}$ | Units |
|---|---|---|---|
| 8-Pin Plastic DIP (P) | 103 | 43 | °C/W |
| 8-Pin SOIC (S) | 158 | 43 | °C/W |

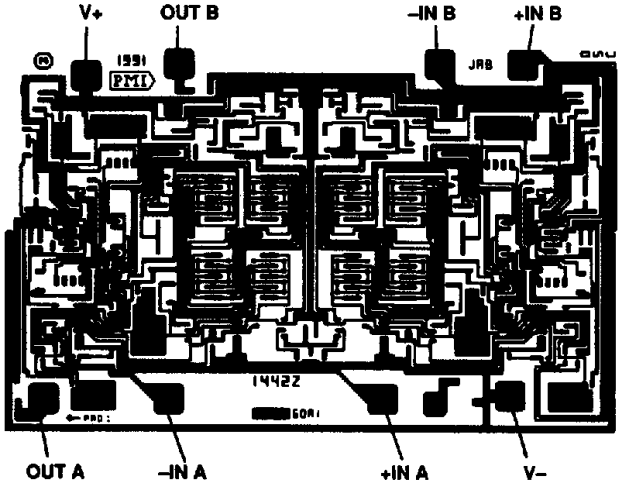
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]$\theta_{JA}$ is specified for the worst case conditions, i.e., $\theta_{JA}$ is specified for device in socket for cerdip, P-DIP, and LCC packages; $\theta_{JA}$ is specified for device soldered in circuit board for SOIC package.

### ORDERING GUIDE

| Model | Temperature Range | Package Option* |
|---|---|---|
| OP285EP | −40°C to +85°C | 8-Pin Plastic DIP |
| OP285ES | −40°C to +85°C | 8-Pin SOIC |
| OP285FP | −40°C to +85°C | 8-Pin Plastic DIP |
| OP285FS | −40°C to +85°C | 8-Pin SOIC |
| OP285GBC | +25°C | DICE |

*For outline information see Package Information section.

### DICE CHARACTERISTICS




*OP-285 Die Size 0.070 in. × 0.108 in. (7,560 sq. mils)*

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.