ANALOG DEVICES

12-Bit 200 KSPS Complete Sampling ADC

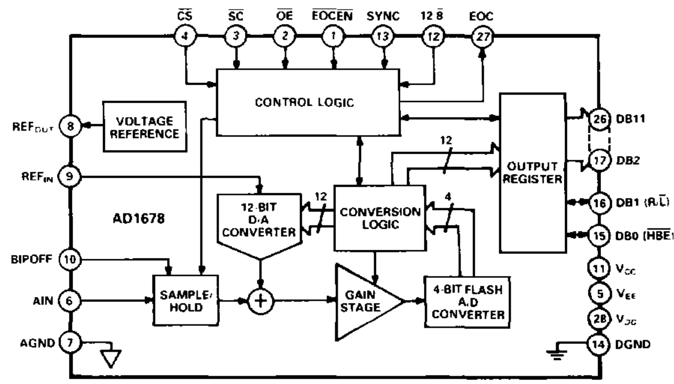
AD1678

3

FEATURES

AC Characterized and Specified
200k Conversions per Second
1 MHz Full Power Bandwidth
500 kHz Full Linear Bandwidth
72 dB S/N+D (K Grade)
Twos Complement Data Format (Bipolar Mode)
Straight Binary Data Format (Unipolar Mode)
10 MΩ Input Impedance
8-Bit or 16-Bit Bus Interface
On-Board Reference and Clock
10 V Unipolar or Bipolar Input Range

AD1678 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1678 is a complete 12-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD1678 offers a choice of digital interface formats; the 12 data bits can be accessed by a 16-bit bus in a single read operation or by an 8-bit bus in two read operations (8+4), with right or left justification. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD1678 operates from +5 V and ±12 V supplies and dissipates 745 mW. A 28-pin plastic DIP and a 0.6" wide ceramic DIP are available. Contact factory for surface-mount package options.

PRODUCT HIGHLIGHTS

1. INTEGRATION: The AD1678 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. PERFORMANCE: The AD1678 provides a throughput of 200k conversions per second. S/N+D is 72 dB (K grade) at 10 kHz and remains flat beyond the Nyquist frequency.
3. SPECIFICATIONS: The AD1678 is specified for ac (or "dynamic") specifications such as S/N+D ratio, THD and IMD. These parameters are important in signal processing applications as they represent the effect on the spectral content of the input signal.
4. EASE OF USE: The pinout is designed for easy board layout, and the choice of single or two read cycle output provides compatibility with 16- or 8-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
5. RELIABILITY: The AD1678 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.

SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V, V_{EE} = −12 V, V_{DD} = +5 V, f_{SAMPLE} = 200 KSPS, f_{IN} = 10.06 kHz[1], unless otherwise noted)

Parameter	AD1678J Min	AD1678J Typ	AD1678J Max	AD1678K Min	AD1678K Typ	AD1678K Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO[2]							
@ +25°C	**70**	71		**72**	73		dB
T_{min} to T_{max}	**70**	71		**71**	73		dB
TOTAL HARMONIC DISTORTION (THD)[3]							
@ +25°C		−88	**−80**		−88	**−80**	dB
		0.004	**0.010**		0.004	**0.010**	%
T_{min} to T_{max}		−85	**−78**		−85	**−78**	dB
		0.005	**0.012**		0.005	**0.012**	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−87	**−80**		−87	**−80**	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[4]							
2nd Order Products		−85	**−80**		−85	**−80**	dB
3rd Order Products		−90	**−80**		−90	**−80**	dB

NOTE
[1] f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a 0 dB (9.997 V p-p) input signal.
[2] See Figures 7 and 8 for higher frequencies and other input amplitudes.
[3] See Figure 6 for other conditions.
[4] f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 200 KSPS. See Figure 10 and Definition of Specifications section.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V, V_{EE} = −12 V, V_{DD} = +5 V ±10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		**2.4**		V
V_{IL}	Low Level Input Voltage			**0.8**	V
I_{IH}	High Level Input Current	V_{IN} = 5 V		**10**	µA
I_{IL}	Low Level Input Current	V_{IN} = 0 V		**10**	µA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	**2.4**		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		**0.4**	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or 5 V		**10**	µA
C_{OZ}	High Z Output Capacitance			10	pF

NOTES
Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.
Specifications subject to change without notice.

DC SPECIFICATIONS (@ +25°C, V_{CC} = +12 V, V_{EE} = −12 V, V_{DD} = +5 V unless otherwise indicated)

Parameter	AD1678J Min	AD1678J Typ	AD1678J Max	AD1678K Min	AD1678K Typ	AD1678K Max	Units
ACCURACY							
Resolution	**12**			**12**			Bits
Differential Linearity							
T_{min} to T_{max} (No Missing Codes)	**12**			**12**			Bits
Integral Linearity Error		±1			±1		LSB
Unipolar Zero Error[1]		±4			±4		LSB
Bipolar Zero Error[1]		±4			±4		LSB
Unipolar Gain Error[1,2]		±3			±3		LSB
Bipolar Gain Error[1,2]		±3			±3		LSB
Temperature Drift (Coefficients)[3]							
Unipolar Zero		±2 (10)			±2 (10)		LSB (ppm/°C)
Bipolar Zero		±2 (10)			±2 (10)		LSB (ppm/°C)
Unipolar Gain		±4 (20)			±4 (20)		LSB (ppm/°C)
Bipolar Gain		±4 (20)			±4 (20)		LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance (f_{IN} = 100 kHz)		10			10		pF
Input Settling Time			1			1	μs
Aperture Delay	5		20	5		20	ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[4]	**4.95**		**5.05**	**4.95**		**5.05**	V
External Load							
Unipolar Mode			**+1.5**			**+1.5**	mA
Bipolar Mode			**+0.5**			**+0.5**	mA
POWER SUPPLIES (T_{min} to T_{max})							
Operating Voltages							
V_{CC}	+11.4	+12	+12.6	+11.4	+12	+12.6	V
V_{EE}	−12.6	−12	−11.4	−12.6	−12	−11.4	V
V_{DD}	+4.5	+5	+5.5	+4.5	+5	+5.5	V
Operating Current							
I_{CC}		18	**20**		18	**20**	mA
I_{EE}		25	**34**		25	**34**	mA
I_{DD}		8	**12**		8	**12**	mA
Power Consumption		560	745		560	745	mW

NOTES
[1]Adjustable to zero; see Figures 12 and 13.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]With maximum external load applied.

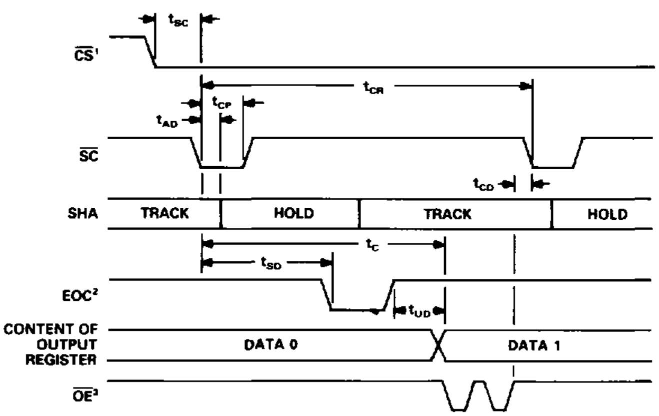
Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V, V_{EE} = −12 V, V_{DD} = +5 V)

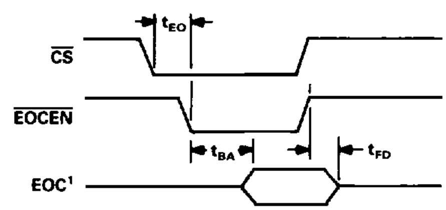
Parameter	Symbol	Min	Typ	Max	Units
$\overline{SC}$ Delay	t_{SC}	50			ns
Conversion Rate	t_{CR}			5	μs
Convert Pulse Width	t_{CP}	150			ns
Aperture Delay	t_{AD}	5		20	ns
Conversion Time[1]	t_C		3.9	4.47	μs
Status Delay	t_{SD}	0		400	ns
Access Time[2]	t_{BA}			100	ns
Float Delay[3]	t_{FD}	10		80	ns
Update Delay	t_{UD}			200	ns
Format Setup	t_{FS}	60			ns
$\overline{OE}$ Delay	t_{OE}	20			ns
Read Pulse Width	t_{RP}	100			ns[4]
		150			ns[5]
Conversion Delay	t_{CD}	150			ns
$\overline{EOCEN}$ Delay	t_{EO}	20			ns

NOTES
[1]Includes Acquisition Time.
[2]Measured from the falling edge of $\overline{OE}/\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 3; C_{OUT} = 100 pF.
[3]Measured from the rising edge of $\overline{OE}/\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 3; C_{OUT} = 10 pF.
[4]12-bit read mode.
[5]8-bit read mode.
Specifications subject to change without notice.



NOTES
[1]IN ASYNCHRONOUS MODE, STATE OF $\overline{CS}$ DOES NOT AFFECT OPERATION. SEE THE START CONVERSION TRUTH TABLE FOR DETAILS.
[2]$\overline{EOCEN}$ = LOW; SEE FIGURE 2. IN SYNCHRONOUS MODE, EOC IS A THREE-STATE OUTPUT. IN ASYNCHRONOUS MODE, EOC IS AN OPEN DRAIN OUTPUT.
[3]DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing



NOTE
[1]SEE END-OF-CONVERT (EOC) PARAGRAPH FOR DETAILS.

Figure 2. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	5 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	0 V	10 pF

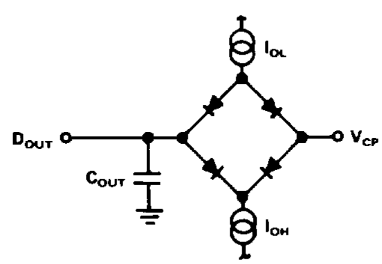


Figure 3. Load Circuit for Bus Timing Specifications

CONVERSION CONTROL

In synchronous mode (SYNC = HIGH), both Chip Select ($\overline{CS}$) and Start Convert ($\overline{SC}$) must be brought LOW to start a conversion. $\overline{CS}$ should be LOW t_{SC} before $\overline{SC}$ is brought LOW. In asynchronous mode (SYNC = LOW), a conversion is started by bringing $\overline{SC}$ low, regardless of the state of $\overline{CS}$.

Before a conversion is started, End-Of-Convert (EOC) is HIGH, and the sample-hold is in track mode. After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample. EOC goes HIGH when the conversion is finished.

In track mode, the sample-hold will settle to ±0.01% (12 bits) in 1 μs maximum. The acquisition time does not affect the throughput rate as the AD1678 goes back into track mode more than 1 μs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW if the maximum throughput rate is needed.

END-OF-CONVERT

In asynchronous mode, End-Of-Convert (EOC) is an open drain output (requiring a minimum 3 kΩ pull-up resistor) enabled by End-Of-Convert ENable ($\overline{EOCEN}$). In synchronous mode, EOC is a three-state output which is enabled by $\overline{EOCEN}$ and $\overline{CS}$. See the Conversion Status Truth Table for details. Access (t_{BA}) and float (t_{FD}) timing specifications do not apply in asynchronous mode where they are a function of the time constant formed by the 10 pF output capacitance and the pull-up resistor.

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12-BIT MODE CODING FORMAT (1 LSB = 2.44 mV)

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
V_{IN}	Output Code	V_{IN}	Output Code
0	000 . . . 0	−5.000 V	100 . . . 0
5.000 V	100 . . . 0	−0.002 V	111 . . . 1
9.9964 V	111 . . . 1	0	000 . . . 0
		+2.500 V	010 . . . 0
		+4.9964 V	011 . . . 1

OUTPUT ENABLE TRUTH TABLES

12-BIT MODE (12/$\overline{8}$ = HIGH)

INPUTS	OUTPUT
($\overline{CS}$ U $\overline{OE}$)	DB11–DB0
1	High Z
↓	Enable 12-Bit Output

8-BIT MODE (12/$\overline{8}$ = LOW)

	INPUTS			OUTPUTS							
	R/$\overline{L}$	HBE	($\overline{CS}$ U $\overline{OE}$)	DB11 . . . DB4							
	X	X	1	← High Z →							
Unipolar Mode	1	0	↓	0	0	0	0	a	b	c	d
	1	1	↓	e	f	g	h	i	j	k	l
	0	0	↓	a	b	c	d	e	f	g	h
	0	1	↓	i	j	k	l	0	0	0	0
Bipolar Mode	1	0	↓	a	a	a	a	a	b	c	d
	1	1	↓	e	f	g	h	i	j	k	l
	0	0	↓	a	b	c	d	e	f	g	h
	0	1	↓	i	j	k	l	0	0	0	0

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
U = Logical OR.
a = MSB.
l = LSB.
↓ = HIGH to LOW transition. Must stay low for $t = t_{RP}$.

START CONVERSION TRUTH TABLE

	INPUTS			
	SYNC	$\overline{CS}$	$\overline{SC}$	STATUS
Synchronous Mode	1	1	X	No Conversion
	1	0	↓	Start Conversion
	1	↓	0	Start Conversion (Not Recommended)
	1	0	0	Continuous Conversion
Asynchronous Mode	0	X	1	No Conversion
	0	X	↓	Start Conversion
	0	X	0	Continuous Conversion

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
↓ = HIGH to LOW transition. Must stay low for $t = t_{CP}$.

CONVERSION STATUS TRUTH TABLE

	INPUTS			OUTPUT	
	SYNC	$\overline{CS}$	$\overline{EOCEN}$	EOC	STATUS
Synchronous Mode	1	0	0	0	Converting
	1	0	0	1	Not Converting
	1	1	X	High Z	Either
	1	X	1	High Z	Either
Asynchronous Mode*	0	X	0	0	Converting
	0	X	0	High Z	Not Converting
	0	X	1	High Z	Either

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
*EOC requires a pull-up resistor in asynchronous mode.

OUTPUT ENABLE OPERATION

The data bits (DB11–DB0) are three-state outputs enabled by Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). $\overline{CS}$ should be LOW t_{OE} before $\overline{OE}$ is brought LOW. Bits DB1 (R/$\overline{L}$) and DB0 ($\overline{HBE}$) are bidirectional. In 12-bit mode they are data output bits. In 8-bit mode they are inputs which define the format of the output register.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REF_{OUT}), output coding is twos complement binary.

When EOC goes HIGH, the output register contains the results of the previous conversion. A period of time t_{UD} is required for the present conversion results to be loaded into the output register. Bringing $\overline{OE}$ LOW t_{OE} after $\overline{CS}$ goes LOW makes the output register contents available on the data bits. A period of time t_{CD} is required after $\overline{OE}$ is brought HIGH before the next $\overline{SC}$ instruction is issued. This allows internal logic states to reset and guarantees minimum aperture jitter for the next conversion.

Output Enable ($\overline{OE}$) must be toggled to update the output register in both 8- and 12-bit read modes.

Figure 4 illustrates the 8-bit read mode (12/$\overline{8}$ = LOW), where only DB11–DB4 are used as output lines onto an 8-bit bus. The output is read in two steps, with the high byte read first, followed by the low byte. High Byte Enable ($\overline{HBE}$) controls the output sequence. The 12-bit result can be right or left justified depending on the state of R/$\overline{L}$.

In 12-bit read mode (12/$\overline{8}$ = HIGH), a single READ operation accesses all 12 output bits on DB11–DB0 for interface to a 16-bit bus. Figure 5 provides the output timing relationships. Note that t_{CR} must be observed, in that $\overline{SC}$ pulses should not be issued at intervals closer than 5 µs. If $\overline{SC}$ is asserted sooner than 5 µs, conversion accuracy may deteriorate. For this reason $\overline{SC}$ should not be held LOW in an attempt to operate in a continuous convert mode.

POWER-UP

One conversion sequence, consisting of one $\overline{SC}$ instruction, is required after power-up to reset internal logic.

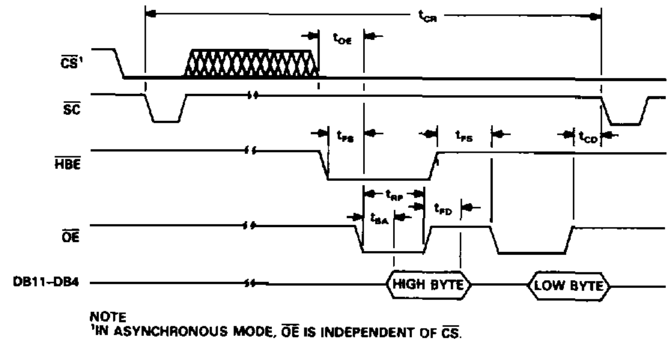

Figure 4. Output Timing, 8-Bit Read Mode

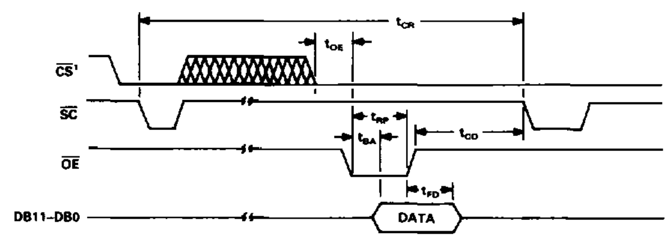

Figure 5. Output Timing, 12-Bit Read Mode

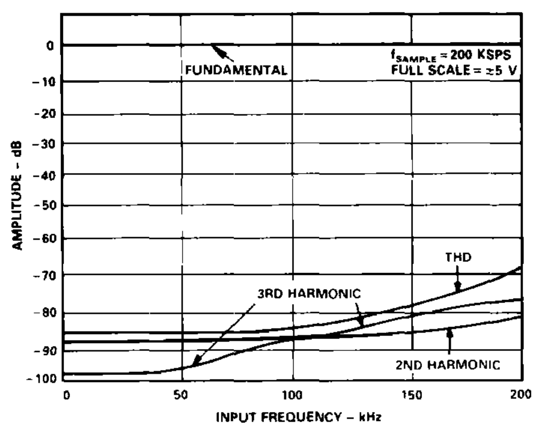

Figure 6. Harmonic Distortion vs. Input Frequency

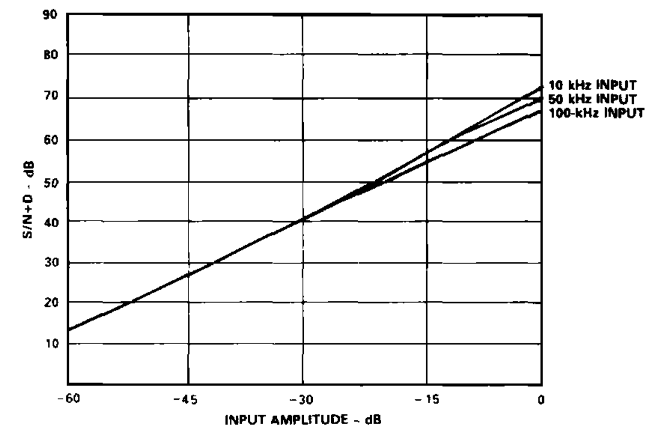

Figure 7. S/N+D vs. Input Amplitude (f_{SAMPLE} = 200 KSPS)

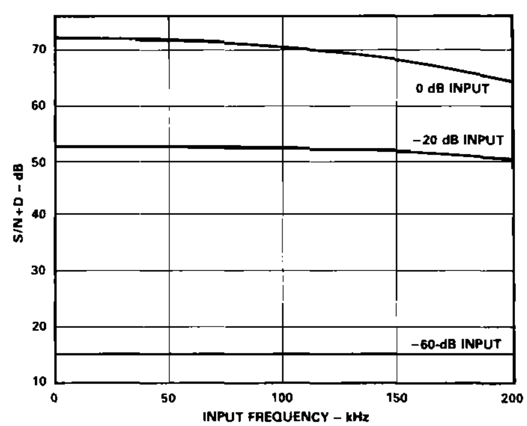

Figure 8. S/N+D vs. Input Frequency and Amplitude

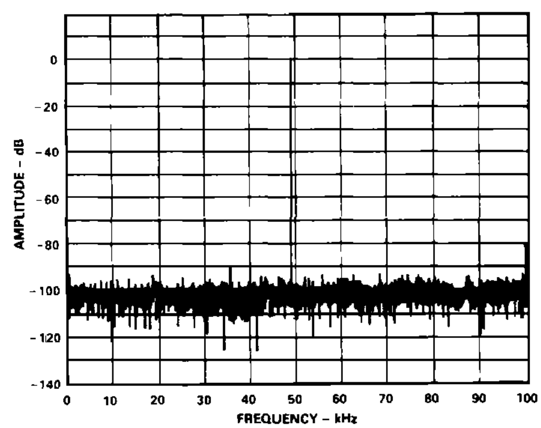

Figure 9. Nonaveraged 2048 Point FFT at 200 KSPS, F_{IN} = 49.902 kHz

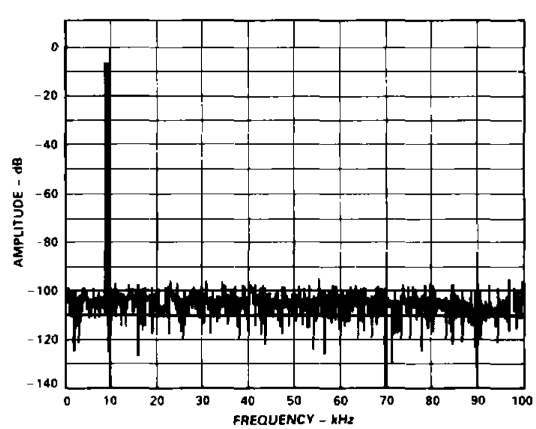

Figure 10. IMD Plot for F_{IN} = 9.08 kHz (fa), 9.58 kHz (fb)

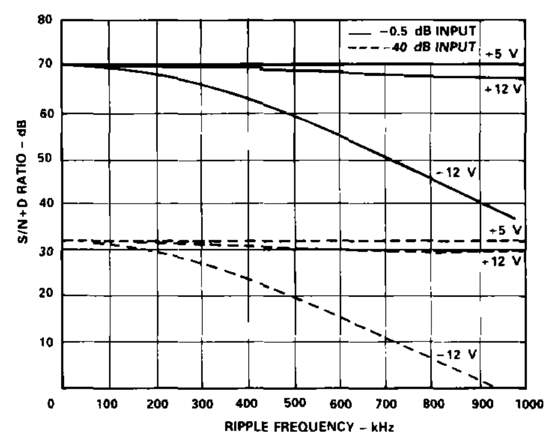

Figure 11. Power Supply Rejection (f_{IN} = 10 kHz, f_{SAMPLE} = 200 KSPS, V_{RIPPLE} = 0.1 V p-p)

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Definition of Specifications

FREQUENCY DOMAIN TESTING
The AD1678 is tested dynamically using a sine wave input and a 2048 point Fast Fourier Transform (FFT) to analyze the resulting output. Coherent sampling is used, wherein the ADC sampling frequency and the analog input frequency are related to each other by a ratio of integers. This ensures that an integral multiple of input cycles is captured, allowing direct FFT processing without windowing or digital filtering which could mask some of the dynamic characteristics of the device. In addition, the frequencies are chosen to be "relatively prime" (no common factors) to maximize the number of different ADC codes that are present in a sample sequence. The result, called Prime Coherent Sampling, is a highly accurate and repeatable measure of the actual frequency domain response of the converter.

NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter, is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of the measured input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is −0.5 dB from full scale (9.44 V p-p). The IMD products are normalized to a 0 dB input signal.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD1678 has been designed to optimize input bandwidth, allowing the AD1678 to undersample input signals with frequencies significantly above the converter's Nyquist frequency. If the input signal is suitably band-limited, the spectral content of the input signal can be recovered.

APERTURE DELAY
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion. In synchronous mode, Chip Select ($\overline{CS}$) should be LOW before $\overline{SC}$ to minimize aperture delay.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

For the AD1678, this specification is 12 bits from T_{min} to T_{max}, which guarantees that all 4096 codes are present over temperature.

UNIPOLAR ZERO ERROR
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR
In the bipolar mode, the major carry transition (1111 1111 1111 to 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR
The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for a 0–10 V range, 4.9963 volts for a ±5 V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

AD1678 PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	7	P	Analog Ground.
AIN	6	AI	Analog Signal Input.
BIPOFF	10	AI	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} through 50 Ω resistor for ±5 V input bipolar mode and twos complement binary output coding. See Figures 12 and 13.
$\overline{CS}$	4	DI	Chip Select. Active LOW.
DGND	14	P	Digital Ground
DB11–DB4	26–19	DO	Data Bits 11 through 4. In 12-bit format (see $12/\overline{8}$ pin), these pins provide the upper 8 bits of data. In 8-bit format, these pins provide all 12 bits in two bytes (see $R/\overline{L}$ pin). Active HIGH.
DB3, DB2	18, 17	DO	Data Bits 3 and 2. In 12-bit format, these pins provide Data Bit 3 and Data Bit 2. Active HIGH. In 8-bit format they are undefined and should be tied to V_{DD}.
DB1 ($R/\overline{L}$)	16	DO	In 12-bit format, Data Bit 1. Active HIGH.
DB0($\overline{HBE}$)	15	DO	In 12-bit format, Data Bit 0. Active HIGH.
EOC	27	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. In asynchronous mode, EOC is an open drain output and requires an external 3 kΩ pull-up resistor. See $\overline{EOCEN}$ and SYNC pins for information on EOC gating.
$\overline{EOCEN}$	1	DI	End-Of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{HBE}$ (DB0)	15	DI	In 8-bit format, High Byte Enable. If LOW, output contains high byte. If HIGH, output contains low byte.
$\overline{OE}$	2	DI	Output Enable. The falling edge of $\overline{OE}$ enables DB11–DB0 in 12-bit format and DB11–DB4 *in 8-bit format. Gated with* $\overline{CS}$. Active LOW.
REF_{IN}	9	AI	Reference Input. +5 V input gives 10 V full scale range.
REF_{OUT}	8	AO	+5 V Reference Output. Tied to REF_{IN} through 50 Ω resistor for normal operation.
$R/\overline{L}$ (DB1)	16	DI	In 8-bit format, Right/Left justified. Sets alignment of 12-bit result within 16-bit field. Tied to V_{DD} for right-justified output and tied to DGND for left-justified output.
$\overline{SC}$	3	DI	Start Convert. Active LOW. See SYNC pin for gating.
SYNC	13	DI	SYNC Control. If tied to V_{DD} (synchronous mode), $\overline{SC}$, EOC and $\overline{EOCEN}$ are gated by $\overline{CS}$. If tied to DGND (asynchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are independent of $\overline{CS}$, and EOC is an open drain output. EOC requires an external 3k Ω pull-up resistor in asynchronous mode.
V_{CC}	11	P	+12 V Analog Power.
V_{EE}	5	P	−12 V Analog Power.
V_{DD}	28	P	+5 V Digital Power.
$12/\overline{8}$	12	DI	Twelve/eight bit format. If tied HIGH, sets output format to 12-bit parallel. If tied LOW, sets output format to 8-bit multiplexed.

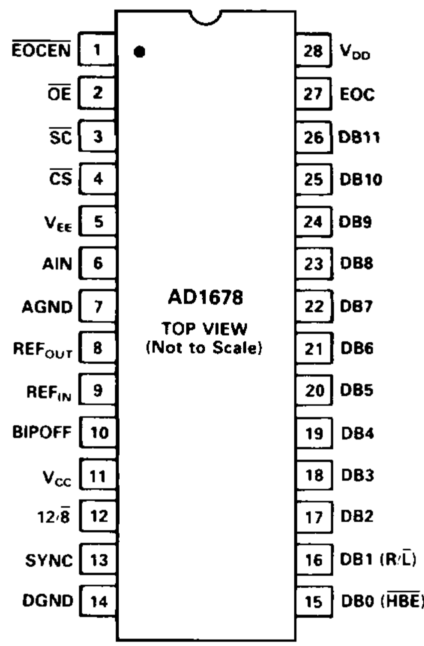
Type: AI = Analog Input.
AO = Analog Output.
DI = Digital Input (TTL and 5 V CMOS compatible).
DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are three-state drivers.
P = Power.

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	−12	+12	V
REF_{IN}	V_{EE}	0	V_{CC}	V
REF_{IN}	V_{CC}	V_{EE}	0	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C
Operating Temperature		0	+70	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Package	Minimum S/N+D @ 10 kHz, −0.5 dB Input	Temperature Range	Package Options*
AD1678JN	28-Pin Plastic DIP	70 dB	0 to +70°C	N-28A
AD1678KN	28-Pin Plastic DIP	72 dB	0 to +70°C	N-28A
AD1678JD	28-Pin Ceramic DIP	70 dB	0 to +70°C	D-28A
AD1678KD	28-Pin Ceramic DIP	72 dB	0 to +70°C	D-28A

*See Section 14 for package outline information.

ESD SENSITIVITY

The AD1678 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high-energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD1678 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual.*

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD1678 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 1000 Ω. The 10 V p-p full-scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC. The AD1678 is factory trimmed to minimize offset, gain and linearity errors. In unipolar mode, the only external component that is required is a 50 Ω ±1% resistor. Two resistors are required in bipolar mode. If offset and gain are not critical, even these components can be eliminated.

In some applications, offset and gain errors need to be more precisely trimmed. The following sections describe the correct procedure for these various situations.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 12. In this mode, data output coding will be twos complement binary. This circuit will allow approximately ±25 mV of offset trim range (±10 LSB) and ±0.5% of gain trim range (±20 LSB).

Either or both of the trim pots can be replaced with 50 Ω ±1% fixed resistors if the AD1678 accuracy limits are sufficient for application. If the pins are shorted together, the additional offset and gain errors will be approximately 20 LSB.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (−1.22 mV for a ±5 V range) and adjust R1 until the major carry transition is located (1111 1111 1111 to 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9963 V for a ±5 V range) and adjust R2 to give the last positive transition (0111 1111 1110 to 0111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9988 V for a ±5 V range) and adjust R1 until the minus full scale transition is located (1000 0000 0000 to 1000 0000 0001). Then perform the gain error trim as outlined above.

UNIPOLAR RANGE INPUTS

The connections for the unipolar mode are shown in Figure 13. In this mode, data output coding will be straight binary. This circuit will allow approximately ±25 mV of offset trim range (±10 LSB) and ±0.5% of gain trim range (±20 LSB).

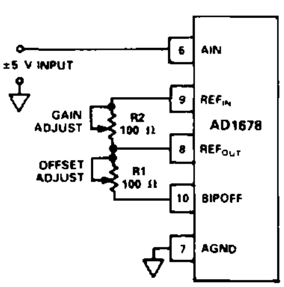


Figure 12. Bipolar Input Connections with Gain and Offset Trims

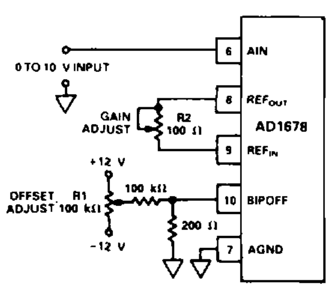


Figure 13. Unipolar Input Connections with Gain and Offset Trims

If the standard accuracy limits of the AD1678 are sufficient for the application, the gain adjust resistor (R2) can be replaced by a 50 Ω ±1% fixed resistor and BIPOFF can be connected to ground.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 5 mA current through a 0.5 Ω trace will develop a voltage drop of 2.5 mV, which is 1 LSB at the 12-bit level for a 10 V full scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD1678 incorporates several features to help the user's layout. Analog pins (V_{EE}, AIN, AGND, REF_{OUT}, REF_{IN}, BIPOFF, V_{CC}) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit architecture. Current through AGND is 200 μA, with no code dependent variation. The current through DGND is dominated by the return current for DB11–DB0 and EOC.

SUPPLY DECOUPLING

The AD1678 power supplies should be well filtered, well regulated and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF disk ceramic capacitor provides adequate decoupling over a wide range of frequencies.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD1678, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD1678 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD1678 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD1678. If multiple AD1678s are used or the AD1678 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at

3

each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

INTERFACING THE AD1678 TO MICROPROCESSORS

The I/O capabilities of the AD1678 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD1678 interface configurations.

AD1678 TO TMS320C25

In Figure 14 the AD1678 is mapped into the TMS320C25 I/O space. AD1678 conversions are initiated by issuing an OUT instruction to Port 8. EOC status and the conversion result are read in with an IN instruction to Port 8. A single wait state is inserted by generating the processor READY input from $\overline{\text{IS}}$, Port 8 and $\overline{\text{MSC}}$. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD1678 read instruction.

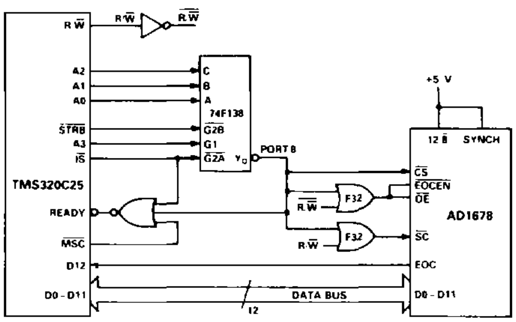


Figure 14. AD1678 to TMS320C25 Interface

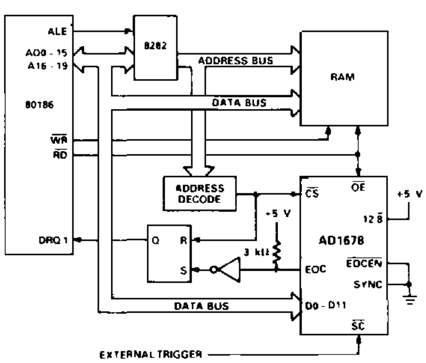


Figure 15. AD1678 to 80186 DMA Interface

AD1678 TO 80186

Figure 15 shows the AD1678 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD1678 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

In this application the AD1678 is configured in the asynchronous mode, which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD1678 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ operation resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6 MHz and 8 MHz 80186 processors.

AD1678 TO Z80

The AD1678 can be interfaced to the Z80 processor in an I/O or memory mapped configuration. Figure 16 illustrates an I/O configuration, where the AD1678 occupies several port addresses to allow separate polling of the EOC status and reading of the data. The lower address bit, A0, is used to select the high and low order bytes of the result. The AD1678 $R/\overline{L}$ line is tied HIGH, resulting in right justified output data.

A useful feature of the Z80 is that a single wait state is automatically inserted during I/O operations, allowing the AD1678 to be used with Z80 processors having clock speeds up to 8 MHz.

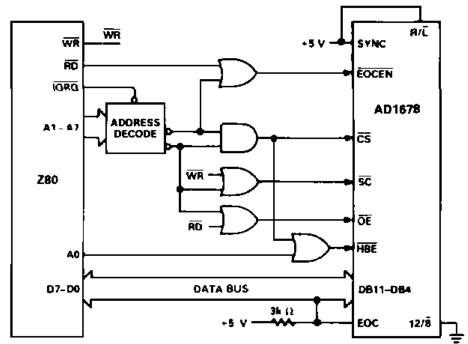


Figure 16. AD1678 to Z80 Interface

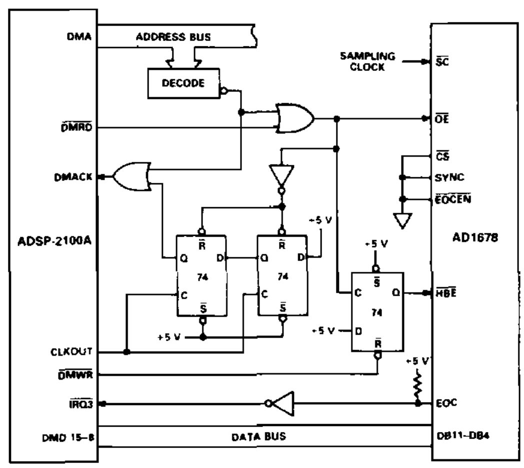


Figure 17. AD1678 to ADSP-2100A Interface

AD1678 TO ANALOG DEVICES' ADSP-2100A

Figure 17 demonstrates the AD1678 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD1678 data memory interface with two hardware wait states.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD1678 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2100A immediately executes a data memory write instruction which asserts $\overline{\text{HBE}}$. In the following cycle, the processor starts a data memory read (high byte read) by providing an address on the DMA bus. The decoded address generates $\overline{\text{OE}}$ for the converter. $\overline{\text{OE}}$, together with logic and latches, is used to force the ADSP-2100A into a two cycle wait state by generating DMACK. The read operation is thus started and completed within three processor cycles (240 ns). HBE is released during "high byte read." This allows the processor to read the lower byte of data as soon as "high byte read" is complete. The low byte read operation executes in a similar manner to the first and is completed during the next 240 ns.