Supervisory Circuits with Watchdog and Manual Reset in 5-Lead SC70 and SOT-23

ADM823/ADM824/ADM825

FEATURES

Precision 2.5 V to 5 V power supply monitor
7 reset threshold options: 2.19 V to 4.63 V
140 ms (min) reset timeout
Watchdog timer with 1.6s timeout (ADM823, ADM824)
Manual reset input (ADM823, ADM825)
Push-pull output stages:
- **$\overline{\text{RESET}}$ (ADM823)**
- **$\overline{\text{RESET}}$, RESET (ADM824/ADM825)**

Low power consumption (5 µA)
Guaranteed reset output valid to V_{CC} = 1 V
Power supply glitch immunity
Specified over automotive temperature range
5-lead SC70 and SOT-23 packages

APPLICATIONS

Microprocessor systems
Computers
Controllers
Intelligent instruments
Portable equipment

FUNCTIONAL BLOCK DIAGRAM

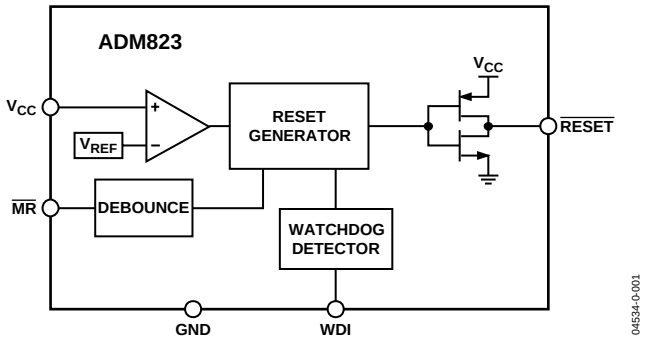

Figure 1.

GENERAL DESCRIPTION

The ADM823/ADM824/ADM825 are supervisory circuits which monitor power supply voltage levels and code execution integrity in microprocessor-based systems. As well as providing power on reset signals, an on-chip watchdog timer can reset the microprocessor if it fails to strobe within a preset timeout period. A reset signal can also be asserted by an external push-button, through a manual reset input. The three parts feature different combinations of watchdog input, manual reset input and output stage configuration, as shown in Table 1.

Each part is available in a choice of seven reset threshold options ranging from 2.19 V to 4.63 V. The reset and watchdog timeout periods are fixed at 140 ms (min) and 1.6s (typ), respectively.

The ADM823/ADM824/ADM825 are available in 5-lead SC70 and SOT-23 packages and typically consume only 3 µA, making them suitable for use in low power portable applications.

Table 1. Selection Table

Part No.	Watchdog Timer	Manual Reset	Output Stage	
			$\overline{\text{RESET}}$	RESET
ADM823	Yes	Yes	Push-Pull	–
ADM824	Yes	–	Push-Pull	Push-Pull
ADM825	–	Yes	Push-Pull	Push-Pull

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

10/04—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 4.75 V to 5.5 V for ADM82_L, V_{CC} = 4.5 V to 5.5 V for ADM82_M, V_{CC} = 3.15 V to 3.6 V for ADM82_T, V_{CC} = 3 V to 3.6 V for ADM82_S, V_{CC} = 2.7 V to 3.6 V for ADM82_R, V_{CC} = 2.38 V to 2.75 V for ADM82_Z, V_{CC} = 2.25 V to 2.75 V for ADM82_Y, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	1		5.5	V	T_A = 0°C to +70°C
	1.2			V	$T_A = T_{MIN}$ to T_{MAX}
Supply Current		10	24	µA	WDI and $\overline{MR}$ unconnected ADM82_L/M
		5	12	µA	WDI and $\overline{MR}$ unconnected ADM82_T/S/R/Z/Y
RESET THRESHOLD VOLTAGE					
ADM82_L	4.56	4.63	4.70	V	T_A = 25°C
	4.50		4.75	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82_M	4.31	4.38	4.45	V	T_A = 25°C
	4.25		4.50	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82_T	3.04	3.08	3.11	V	T_A = 25°C
	3.00		3.15	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82_S	2.89	2.93	2.96	V	T_A = 25°C
	2.85		3.00	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82_R	2.59	2.63	2.66	V	T_A = 25°C
	2.55		2.70	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82_Z (SC70 only)	2.28	2.32	2.35	V	T_A = 25°C
	2.25		2.38	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82_Y (SC70 only)	2.16	2.19	2.22	V	T_A = 25°C
	2.13		2.25	V	$T_A = T_{MIN}$ to T_{MAX}
RESET THRESHOLD TEMPERATURE COEFFICIENT		40		ppm/°C	
RESET THRESHOLD HYSTERESIS		10		mV	ADM82_L/M
		5		mV	ADM82_T/S/R/Z/Y
RESET TIMEOUT PERIOD	140	200	280	ms	
V_{CC} TO RESET DELAY		40		µs	$V_{TH} - V_{CC}$ = 100 mV
$\overline{RESET}$ Output Voltage			0.4	V	$V_{CC} = V_{TH}$ min, I_{SINK} = 3.2 mA, ADM82_L/M
			0.3	V	$V_{CC} = V_{TH}$ min, I_{SINK} = 1.2 mA, ADM82_T/S/R/Z/Y
			0.3	V	T_A = 0°C to 70°C, V_{CC} = 1 V, V_{CC} falling, I_{SINK} = 50 µA
	V_{CC} – 1.5			V	$V_{CC} = V_{TH}$ max, I_{SOURCE} = 120 µA, ADM82_L/M
	0.8 × V_{CC}			V	$V_{CC} = V_{TH}$ max, I_{SOURCE} = 30 µA, ADM82_T/S/R/Z/Y
RESET Output Voltage			0.4	V	$V_{CC} = V_{TH}$ max, I_{SINK} = 3.2 mA, ADM824L/M, ADM825L/M
			0.3	V	$V_{CC} = V_{TH}$ max, I_{SINK} = 1.2 mA, ADM824T/S/R/Z/Y, ADM825T/S/R/Z/Y
	0.8 × V_{CC}			V	$V_{CC} \geq$ 1.8 V, I_{SOURCE} = 150 µA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
WATCHDOG INPUT (ADM823, ADM824)					
Watchdog Timeout Period	1.12	1.6	2.40	s	
WDI Pulse Width	50			ns	V_{IL} = 0.4 V, V_{IH} = 0.8 × V_{CC}
WDI Input Threshold					
V_{IL}	0.7 × V_{CC}		0.3 × V_{CC}	V	
WDI Input Current		120	160	µA	V_{WDI} = V_{CC}, time average
	−20	−15		µA	V_{WDI} = 0, time average
MANUAL RESET INPUT (ADM823, ADM825)					
$\overline{MR}$ Input Threshold			0.3 × V_{CC}	V	
	0.7 × V_{CC}			V	
$\overline{MR}$ Input Pulse Width	1			µs	
$\overline{MR}$ Glitch Rejection		100		ns	
$\overline{MR}$ Pull-Up Resistance	35	52	75	kΩ	
$\overline{MR}$ to Reset Delay		500		ns	

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
Output Current (RESET, $\overline{RESET}$)	20 mA
All Other Pins	−0.3 V to (V_{CC} + 0.3 V)
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
θ_{JA} Thermal Impedance	
SC70	146°C/W
SOT-23	270°C/W
Lead Temperature	
Soldering (10 s)	300°C
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

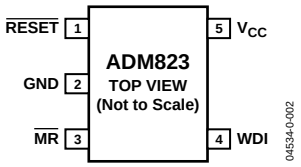

Figure 2. ADM823 Pin Configuration

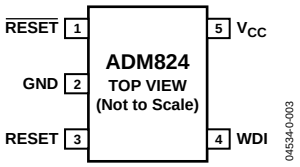

Figure 3. ADM824 Pin Configuration

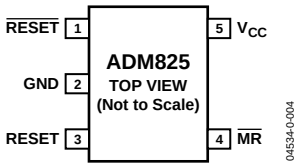

Figure 4. ADM825 Pin Configuration

Table 4. Pin Function Descriptions

Pin. No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Push-Pull Active-Low Reset Output. Asserted whenever V_{CC} is below the reset threshold, V_{TH}.
2	GND	Ground.
3	$\overline{\text{MR}}$ (ADM823)	Manual Reset Input. This is an active-low input which, when forced low for at least 1 µs, generates a reset. It features a 52 kV internal pull-up.
	RESET (ADM824/ADM825)	Active-High, Push-Pull Reset Output.
4	WDI (ADM823/ADM824)	Watchdog Input. Generates a reset if the voltage on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin or if a reset is generated.
	$\overline{\text{MR}}$ (ADM825)	Manual Reset Input.
5	V_{CC}	Power Supply Voltage Being Monitored.

TYPICAL PERFORMANCE CHARACTERISTICS

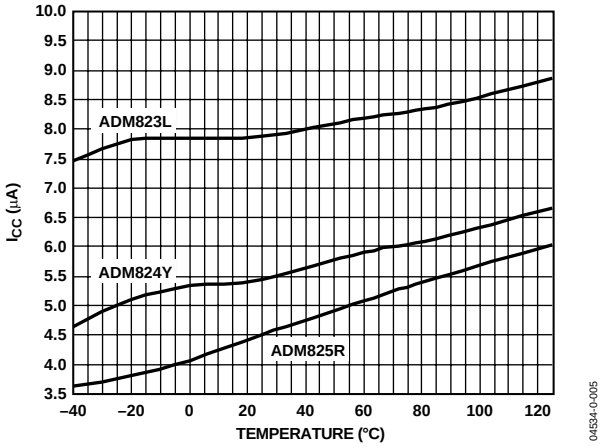

Figure 5. Supply Current vs. Temperature

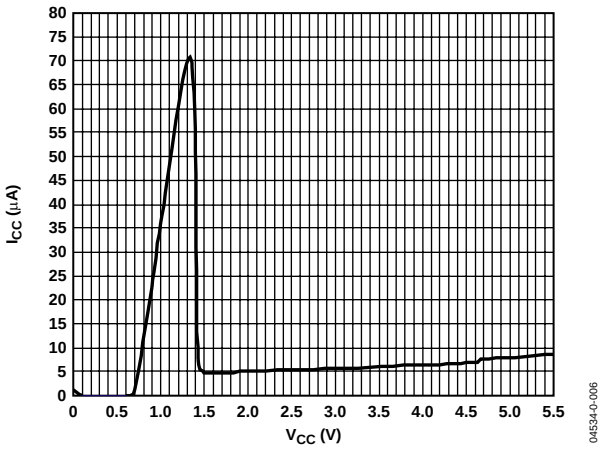

Figure 6. Supply Current vs. Supply Voltage

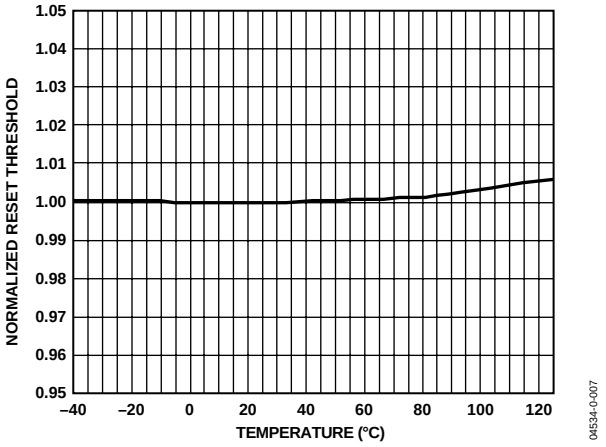

Figure 7. Normalized Reset Threshold vs. Temperature

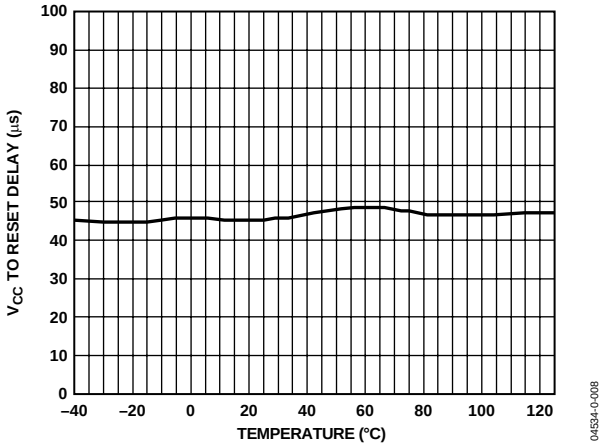

Figure 8. Reset Comparator Propagation Delay vs. Temperature (V_{CC} Falling)

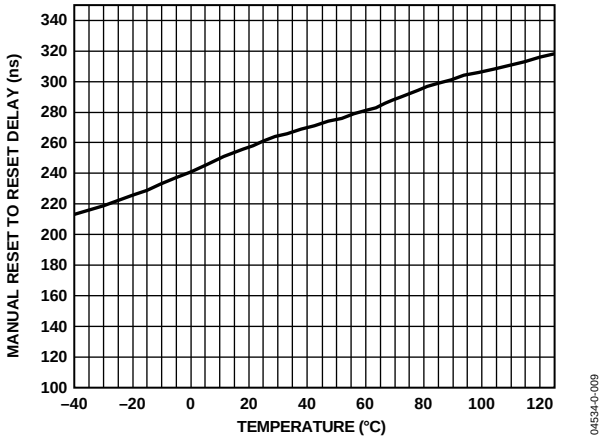

Figure 9. Manual Reset to Reset Propagation Delay vs. Temperature (ADM823/ADM825)

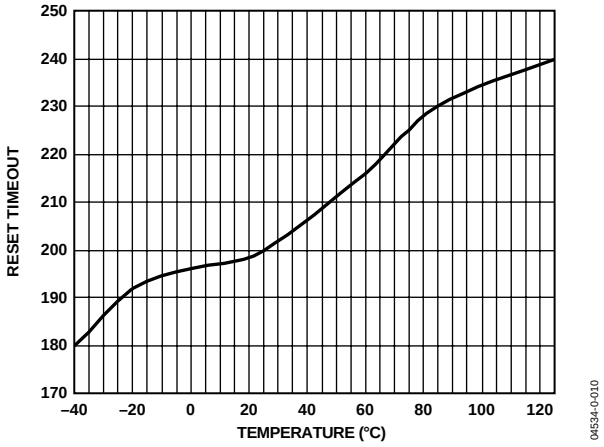

Figure 10. Reset Timeout Period vs. Temperature

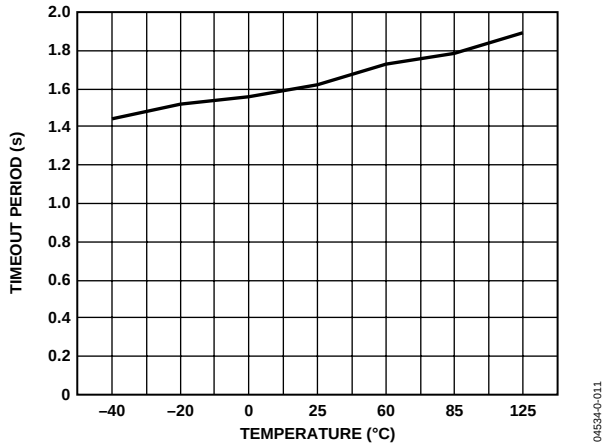

Figure 11. Watchdog Timeout Period vs. Temperature (ADM823/ADM824)

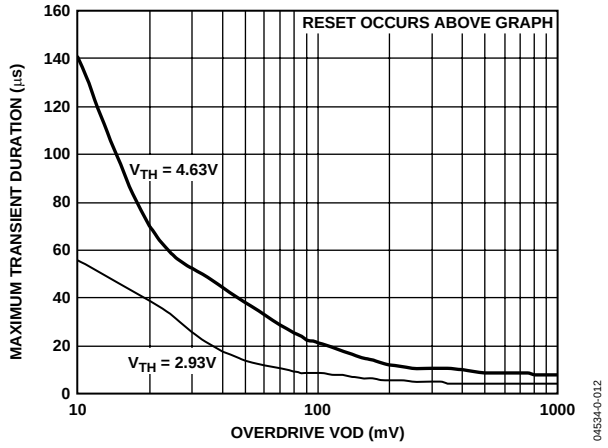

Figure 12. Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive

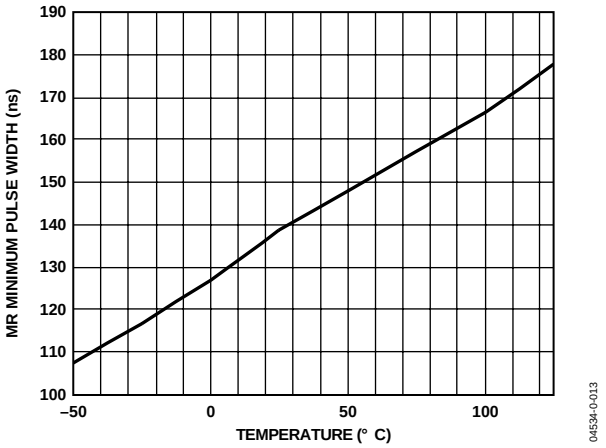

Figure 13. Manual Reset Minimum Pulse Width vs. Temperature (ADM823/ADM825)

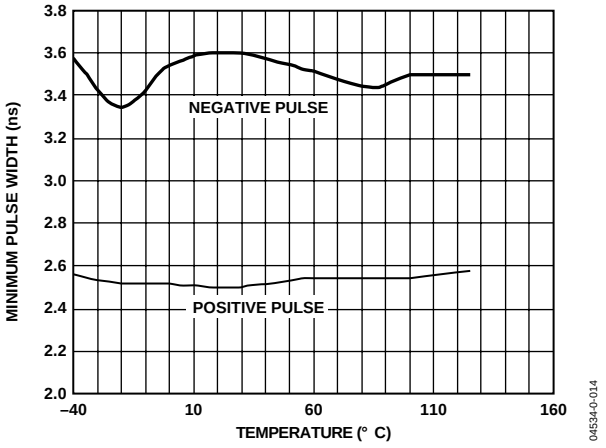

Figure 14. Watchdog Input Minimum Pulse Width vs. Temperature (ADM823/ADM824)

CIRCUIT DESCRIPTION

The ADM823/ADM824/ADM825 provide microprocessor supply voltage supervision by controlling the microprocessor's reset input. Code-execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold. They are also avoided by allowing supply voltage stabilization with a fixed-timeout reset pulse after the supply voltage rises above the threshold. In addition, problems with microprocessor code execution can be monitored and corrected with a watchdog timer (ADM823/ ADM824). By including watchdog strobe instructions in microprocessor code, a watchdog timer can detect if the microprocessor code breaks down or becomes stuck in an infinite loop. If this happens, the watchdog timer asserts a reset pulse that restarts the microprocessor in a known state. If the user detects a problem with the system's operation, a manual reset input is available (ADM823/ADM825) to reset the microprocessor with an external push-button, for example.

RESET OUTPUT

The ADM823 features an active-low, push-pull reset output while the ADM824/ADM825 feature dual active-low and active-high push-pull reset outputs. For active-low and active-high outputs, the reset signal is guaranteed to be logic low and logic high, respectively, for V_{CC} down to 1 V.

The reset output is asserted when V_{CC} is below the reset threshold (V_{TH}), when $\overline{MR}$ is driven low, or when WDI is not serviced within the watchdog timeout period (t_{WD}). Reset remains asserted for the duration of the reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold, after $\overline{MR}$ transitions from low-to-high, or after the watchdog timer times out. Figure 15 illustrates the behavior of the reset outputs.

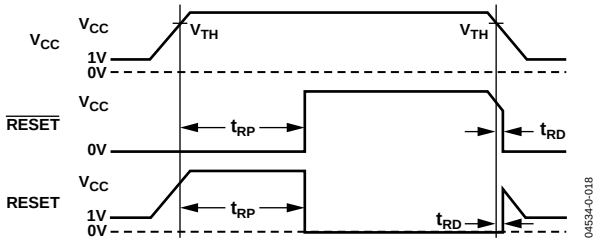

Figure 15. Reset Timing Diagram

MANUAL RESET INPUT

The ADM823/ADM825 feature a manual reset input ($\overline{MR}$) which, when driven low, asserts the reset output. When $\overline{MR}$ transitions from low to high, reset remains asserted for the duration of the reset active timeout period before deasserting. The $\overline{MR}$ input has a 52 kV internal pull-up so that the input is always high when unconnected. An external push-button switch can be connected between $\overline{MR}$ and ground so that the user can generate a reset. Debounce circuitry for this purpose is integrated on-chip. Noise immunity is provided on the $\overline{MR}$ input and fast, negative-going transients of up to 100 ns (typ) are ignored. A 0.1 µF capacitor between $\overline{MR}$ and ground provides additional noise immunity.

WATCHDOG INPUT

The ADM823/ADM824 feature a watchdog timer which monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI), which detects pulses as short as 50 ns. If the timer counts through the preset watchdog timeout period (t_{WD}), reset is asserted. The microprocessor is required to toggle the WDI pin to avoid being reset. Failure of the microprocessor to toggle WDI within the timeout period therefore indicates a code execution error, and the reset pulse generated restarts the microprocessor in a known state.

In addition to logic transitions on WDI, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on V_{CC} or by $\overline{MR}$ being pulled low. When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset deassserts. The watchdog timer can be disabled by leaving WDI floating or by three-stating the WDI driver.

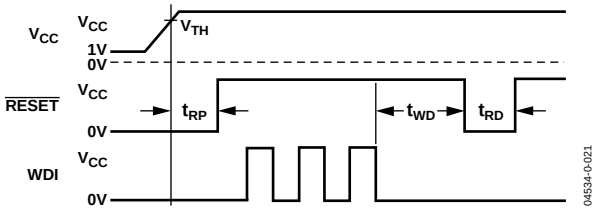

Figure 16. Watchdog Timing Diagram

APPLICATION INFORMATION

WATCHDOG INPUT CURRENT

In order to minimize watchdog input current (and minimize overall power consumption), leave WDI low for the majority of the watchdog timeout period. When driven high, WDI can draw as much as 160 µA. Pulsing WDI low-high-low at a low duty cycle reduces the effect of the large input current. When WDI is unconnected, a window comparator disconnects the watchdog timer from the reset output circuitry so that reset is not asserted when the watchdog timer times out.

NEGATIVE-GOING V_{CC} TRANSIENTS

To avoid unnecessary resets caused by fast power supply transients, the ADM823/ADM824/ADM825 are equipped with glitch rejection circuitry. The typical performance characteristic in Figure 12 plots V_{CC} transient duration vs. the transient magnitude. The curves show combinations of transient magnitude and duration for which a reset is not generated for 4.63 V and 2.93 V reset threshold parts. For example, with the 2.93 V threshold, a transient that goes 100 mV below the threshold and lasts 8 µs typically does not cause a reset, but if the transient is any bigger in magnitude or duration, a reset is generated. An optional 0.1 µF bypass capacitor mounted close to V_{CC} provides additional glitch rejection.

ENSURING RESET VALID TO V_{CC} = 0 V

Both active-low and active-high reset outputs are guaranteed to be valid for V_{CC} as low as 1 V. However, by using an external resistor with push-pull configured reset outputs, valid outputs for V_{CC} as low as 0 V are possible. For an active-low reset output, a resistor connected between $\overline{\text{RESET}}$ and ground pulls the output low when it is unable to sink current. For the active-high case, a resistor connected between RESET and V_{CC} pulls the output high when it is unable to source current. A large resistance such as 100 kΩ should be used so that it does not overload the reset output when V_{CC} is above 1 V.

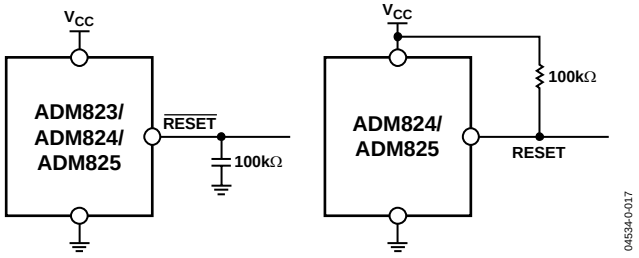

Figure 17. Ensuring Reset Valid to V_{CC} = 0 V

WATCHDOG SOFTWARE CONSIDERATIONS

In implementing the microprocessor's watchdog strobe code, quickly switching WDI low-high and then high-low (minimizing WDI high time) is desirable for current consumption reasons. However, a more effective way of using the watchdog function can be considered.

A low-high-low WDI pulse within a given subroutine prevents the watchdog timing out. However, if the subroutine becomes stuck in an infinite loop, the watchdog cannot detect this because the subroutine continues to toggle WDI. A more effective coding scheme for detecting this error involves using a slightly longer watchdog timeout. In the program that calls the subroutine, WDI is set high. The subroutine sets WDI low when it is called. If the program executes without error, WDI is toggled high and low with every loop of the program. If the subroutine enters an infinite loop, WDI is kept low, the watchdog times out, and the microprocessor is reset.

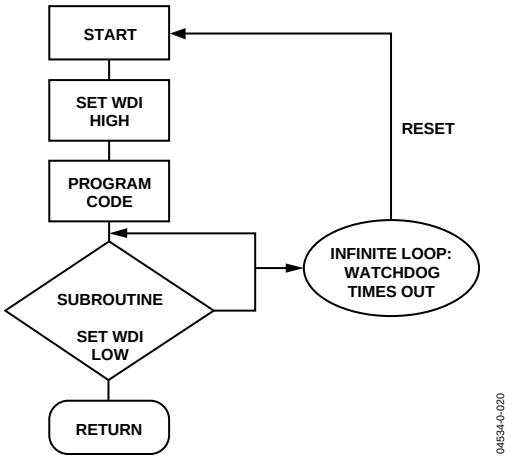

Figure 18. Watchdog Flow Diagram

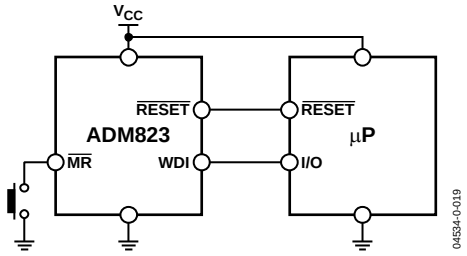

Figure 19. Typical Application Circuit

OUTLINE DIMENSIONS

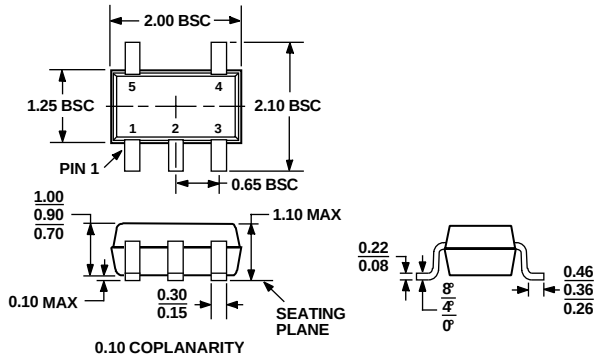

Figure 20. 5-Lead Plastic Surface-Mount Package [SC-70]
(KS-5)
Dimensions shown in millimeters

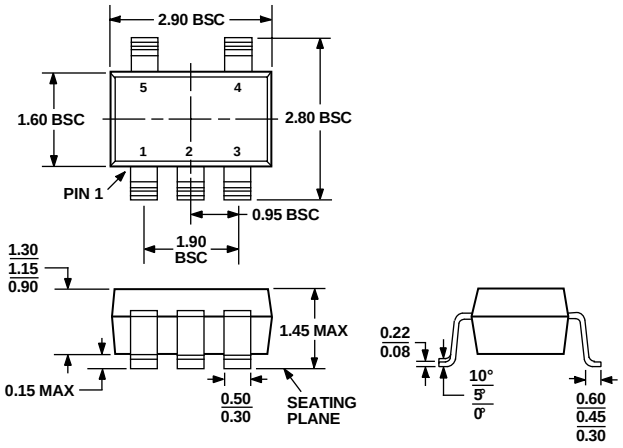

Figure 21. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

ORDERING GUIDES

Table 5. ADM823 Ordering Guide

Model	Reset Threshold (V)	Temperature Range	Quantity	Package Type	Branding
ADM823LYKS-R7	4.63	–40°C to +125°C	3k	SC70-5	N07
ADM823LYRJ-R7	4.63	–40°C to +125°C	3k	SOT-23-5	N07
ADM823MYKS-R7	4.38	–40°C to +125°C	3k	SC70-5	N07
ADM823MYRJ-R7	4.38	–40°C to +125°C	3k	SOT-23-5	N07
ADM823TYKS-R7	3.08	–40°C to +125°C	3k	SC70-5	N07
ADM823TYRJ-R7	3.08	–40°C to +125°C	3k	SOT-23-5	N07
ADM823SYKS-R7	2.93	–40°C to +125°C	3k	SC70-5	N07
ADM823SYRJ-R7	2.93	–40°C to +125°C	3k	SOT-23-5	N07
ADM823RYKS-R7	2.63	–40°C to +125°C	3k	SC70-5	N07
ADM823RYRJ-R7	2.63	–40°C to +125°C	3k	SOT-23-5	N07
ADM823ZYKS-R7	2.32	–40°C to +125°C	3k	SC70-5	N07
ADM823YYKS-R7	2.19	–40°C to +125°C	3k	SC70-5	N07

Table 6. ADM824 Ordering Guide

Model[1]	Reset Threshold (V)	Temperature Range	Quantity	Package Type	Branding
ADM824LYKS-R7	4.63	–40°C to +125°C	3k	SC70-5	N08
ADM824LYRJ-R7	4.63	–40°C to +125°C	3k	SOT-23-5	N08
ADM824MYKS-R7	4.38	–40°C to +125°C	3k	SC70-5	N08
ADM824MYRJ-R7	4.38	–40°C to +125°C	3k	SOT-23-5	N08
ADM824TYKS-R7	3.08	–40°C to +125°C	3k	SC70-5	N08
ADM824TYRJ-R7	3.08	–40°C to +125°C	3k	SOT-23-5	N08
ADM824SYKS-R7	2.93	–40°C to +125°C	3k	SC70-5	N08
ADM824SYRJ-R7	2.93	–40°C to +125°C	3k	SOT-23-5	N08
ADM824RYKS-R7	2.63	–40°C to +125°C	3k	SC70-5	N08
ADM824RYRJ-R7	2.63	–40°C to +125°C	3k	SOT-23-5	N08
ADM824ZYKS-R7	2.32	–40°C to +125°C	3k	SC70-5	N08
ADM824YYKS-R7	2.19	–40°C to +125°C	3k	SC70-5	N08

[1] All of the ADM824 models are nonstandard. For availability of alternate versions, contact Sales.

Table 7. ADM825 Ordering Guide

Model	Reset Threshold (V)	Temperature Range	Quantity	Package Type	Branding
ADM825LYKS-R7	4.63	–40°C to +125°C	3k	SC70-5	N09
ADM825LYRJ-R7	4.63	–40°C to +125°C	3k	SOT-23-5	N09
ADM825MYKS-R7	4.38	–40°C to +125°C	3k	SC70-5	N09
ADM825MYRJ-R7	4.38	–40°C to +125°C	3k	SOT-23-5	N09
ADM825TYKS-R7	3.08	–40°C to +125°C	3k	SC70-5	N09
ADM825TYRJ-R7	3.08	–40°C to +125°C	3k	SOT-23-5	N09
ADM825SYKS-R7	2.93	–40°C to +125°C	3k	SC70-5	N09
ADM825SYRJ-R7	2.93	–40°C to +125°C	3k	SOT-23-5	N09
ADM825RYKS-R7	2.63	–40°C to +125°C	3k	SC70-5	N09
ADM825RYRJ-R7	2.63	–40°C to +125°C	3k	SOT-23-5	N09
ADM825ZYKS-R7	2.32	–40°C to +125°C	3k	SC70-5	N09
ADM825YYKS-R7	2.19	–40°C to +125°C	3k	SC70-5	N09

D04534–0–10/04(0)