Making Memory Smarter™

5 Volt Synchronous x18 First-In/First-Out Queue

Memory Configuration	Device
4,096 x 18	FQ245
2,048 x 18	FQ235
1,024 x 18	FQ225
512 x 18	FQ215
256 x 18	FQ205

Key Features:

- **Industry leading First-In/First-Out Queues (up to 100MHz)**
- **Independent Write and Read cycle time**
- **5V power supply**
- **Reset clears all previously programmed configurations including Write and Read pointers.**
- **Preset for Almost Full ($\overline{PRAF}$) and Almost Empty ($\overline{PRAE}$) offsets values**
- **Parallel programming of $\overline{PRAF}$ and $\overline{PRAE}$ offset values**
- **Full, Empty, Almost Full, Almost Empty, and Half Full indicators**
- **Asynchronous output enable tri-state data output drivers**
- **Available packages: 64 - pin Plastic Thin Quad Flat Package (TQFP), 64 - pin Slim Thin Quad Flat Package (STQFP)**
- **(0°C to 70°C) Commercial operating temperature available**
- **(-40°C to 85°C) Industrial operating temperature available**

Product Description:

HBA's FlexQ™ I offers industry leading FIFO queuing bandwidth (up to 1.8 Gbps), with a wide range of memory configurations (from 256 x 18 to 4,096 x 18). System designer has full flexibility of implementing deeper and wider queues with Write ($\overline{WEXI}$ and $\overline{WEXO}$) and Read ($\overline{REXI}$ and $\overline{REXO}$) expansion features using Daisy Chain technique. Full, Empty, and Half Full indicators allow easy handshaking between transmitters and receivers. User programmable Almost Full and Almost Empty (Parallel) indicators allow implementation of virtual queue depths.

Asynchronous Output Enable pin configures the tri-state data output drivers. Independent Write and Read controls provide rate-matching capability.

Data is written into the queue at the low to high transition of WCLK if $\overline{WEN}$ is asserted. Data is read from the queue at the low to high transition of RCLK if $\overline{REN}$ is asserted.

Reset clears all previously programmed configurations by providing a low pulse on $\overline{RST}$ pin. In addition, Write and Read pointers to the queue are initialized to zero.

These FlexQ™ I devices have low power consumption, hence minimizing system power requirements. In addition, industry standard 64 - pin Plastic TQFP and 64 - pin STQFP are offered to save system board space.

These queues are ideal for applications such as data communication, telecommunication, graphics, multiprocessing, test equipment, network switching, etc.

Block Diagram of Single Synchronous Queue
4,096 x 18 / 2 ,048 x 18 / 1,024 x 18 / 512 x 18 / 256 x 18

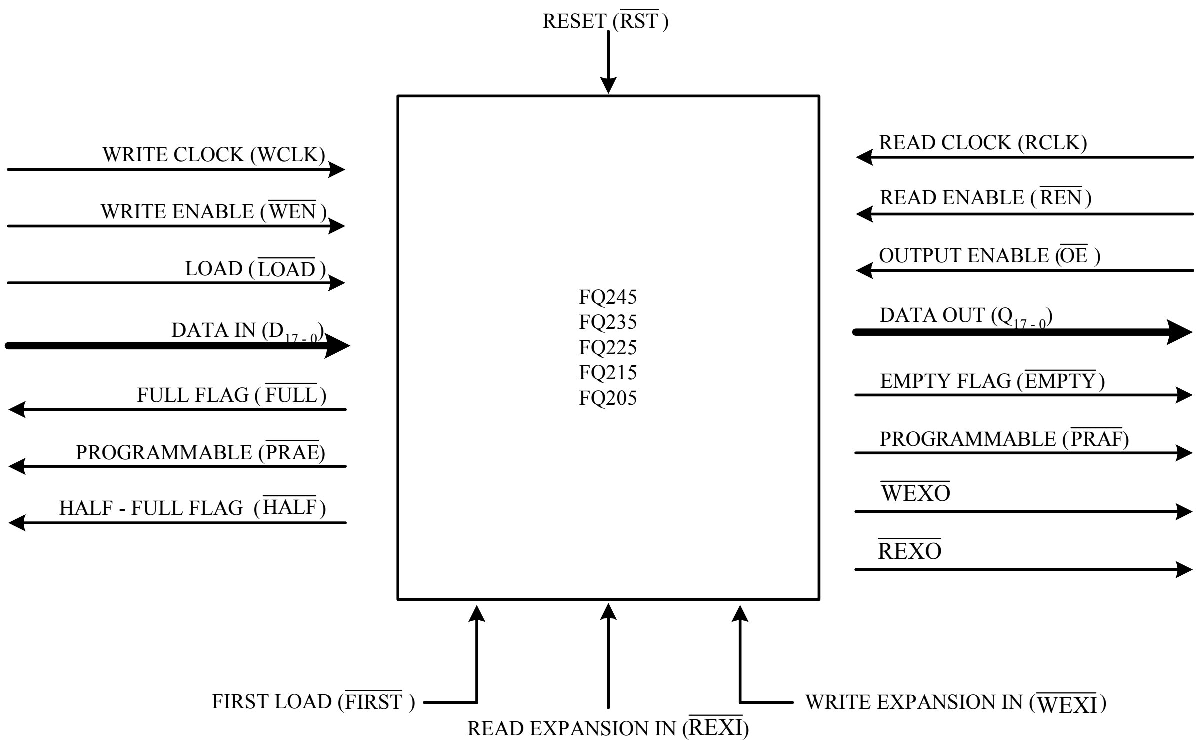


Figure 1. Single Device Configuration Signal Flow Diagram

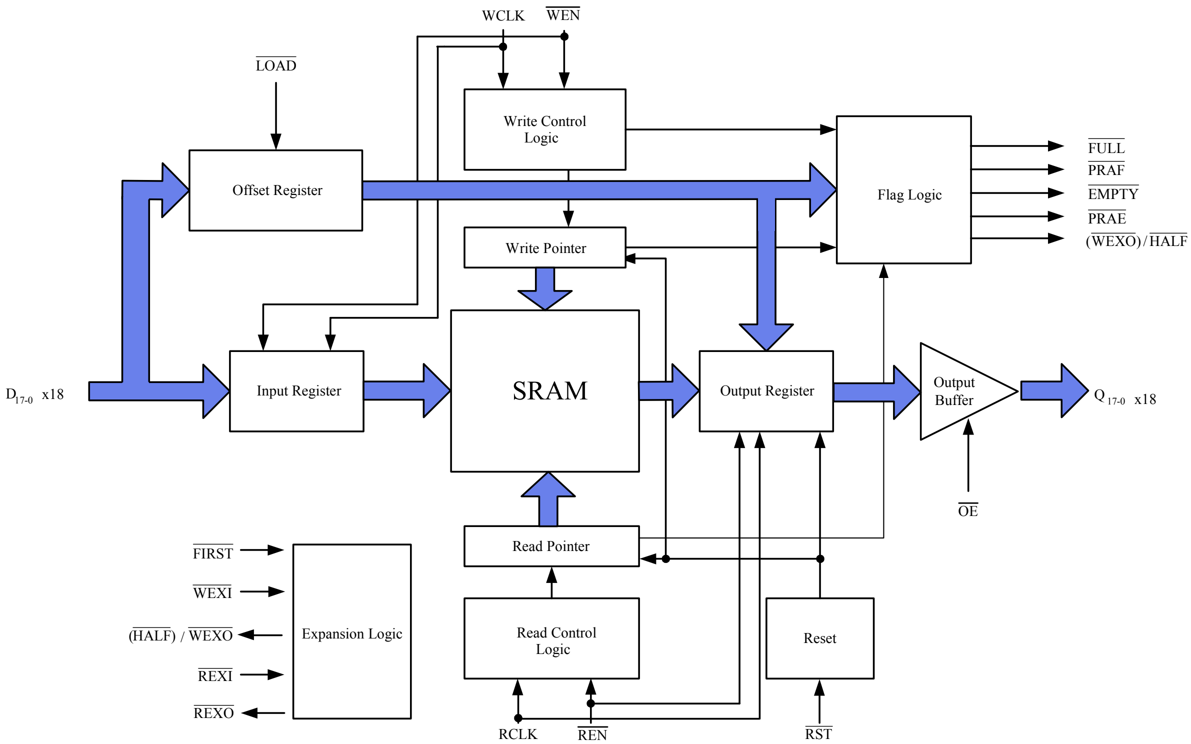
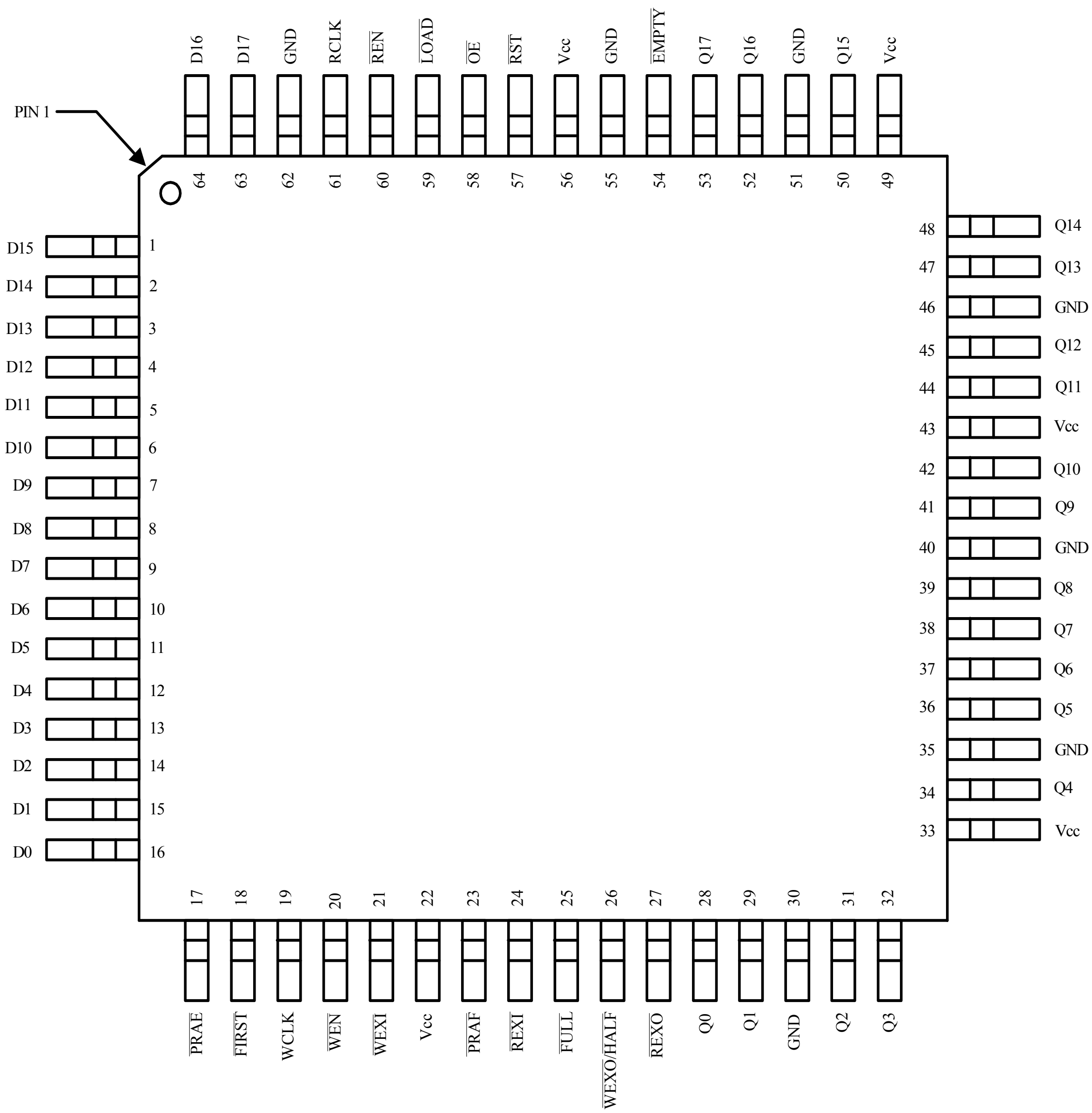


Figure 2. Device Architecture



TQFP – 64 (Drw No: PF-01A; Order Code: PF)
STQFP – 64 (Drw No: TF-01A; Order Code: TF)
Top View

Figure 3. Device Pin Out

Pin #	Pin Name	Pin Symbol	Input/Output	Description
57	Reset	$\overline{RST}$	Input	Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{RST}$ low. $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. All data outputs will go low. Previous programmed configurations will not be maintained.
19	Write Clock	WCLK	Input	Writes data into queue during low to high transitions of WCLK if $\overline{WEN}$ is set low.
20	Write Enable	$\overline{WEN}$	Input	Controls write operation into queue or offset registers during low to high transition of WCLK.
59	Load Enable	$\overline{LOAD}$	Input	$\overline{LOAD}$ controls write/read, to/from offset registers during low to high transition of WCLK/RCLK respectively. Use in conjunction with $\overline{WEN}$ / $\overline{REN}$.
18	First Load	$\overline{FIRST}$	Input	In single device configuration, $\overline{FIRST}$ is set low. In depth expansion configuration, $\overline{FIRST}$ is set low for the first device and set high for other devices in the Daisy Chain.
21	Write Expansion In	$\overline{WEXI}$	Input	In single device configuration, $\overline{WEXI}$ is set low. In depth expansion configuration, $\overline{WEXI}$ is connected to $\overline{WEXO}$ of previous device in the Daisy Chain.
63, 64, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16	Data Inputs	D_{17-0}	Input	18 - bit wide input data bus.
61	Read Clock	RCLK	Input	Reads data from queue during low to high transitions of RCLK if $\overline{REN}$ is set low.
60	Read Enable	$\overline{REN}$	Input	Controls read operation from queue or offset registers during low to high transition of RCLK.
24	Read Expansion In	$\overline{REXI}$	Input	In single device configuration, $\overline{REXI}$ is set low. In depth expansion configuration, $\overline{REXI}$ is connected to $\overline{REXO}$ of previous device in the Daisy Chain.
58	Output Enable	$\overline{OE}$	Input	Setting $\overline{OE}$ low activates the data output drivers. Setting $\overline{OE}$ high deactivates the data output drivers (High-Z).
53, 52, 50, 48, 47, 45, 44, 42, 41, 39, 38, 37, 36, 34, 32, 31, 29, 28	Data Outputs	Q_{17-0}	Output	18 - bit wide output data bus.
27	Read Expansion Out	$\overline{REXO}$	Output	In depth expansion configuration, $\overline{REXO}$ is connected to $\overline{REXI}$ of next device in the Daisy Chain.
25	Full Flag	$\overline{FULL}$	Output	Queue is full when $\overline{FULL}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue.

Table 1. Pin Descriptions

Pin #	Pin Name	Pin Symbol	Input/Output	Description
54	Empty Flag	$\overline{\text{EMPTY}}$	Output	Queue is empty when $\overline{\text{EMPTY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue.
23	Almost Full	$\overline{\text{PRAF}}$	Output	Queue is almost full when $\overline{\text{PRAF}}$ goes low during the low to high transition of WCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{\text{PRAF}}$.
17	Almost Empty	$\overline{\text{PRAE}}$	Output	Queue is almost empty when $\overline{\text{PRAE}}$ goes low during the low to high transition of RCLK. Default (Empty+offset) or programmed offset values determine the status of $\overline{\text{PRAE}}$.
26	Write Expansion Out/Half Full	$\overline{\text{WEXO}}$ / $\overline{\text{HALF}}$	Output	In single device configuration, queue is more than half full when $\overline{\text{WEXO}}$ / $\overline{\text{HALF}}$ goes low. In depth expansion configuration, $\overline{\text{WEXO}}$ / $\overline{\text{HALF}}$ is connected to $\overline{\text{WEXI}}$ of next device in the Daisy Chain.
22, 33, 43, 49, 56	Power	Vcc	N/A	5V power supply.
30, 35, 40, 46, 51, 55, 62	Ground	GND	N/A	0V Ground.

Table 1. Pin Descriptions (Continued)

Symbol	Rating	Com'l & Ind'l	Unit
V_{TERM}	Terminal Voltage with respect to GND	-0.5 to + 7	V
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	-50 to +50	mA

NOTES:
Absolute Max Ratings are for reference only. Permanent damage to the device may occur if extended period of operation is outside this range. Standard operation should fall within the Recommended Operating Conditions.

Table 2. Absolute Maximum Ratings

		FQ245 FQ235 FQ225 FQ215 FQ205						
		Commercial Clock = 10ns, 15ns, 20ns			Industrial Clock = 10ns, 15ns, 20ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Recommended Operating Conditions								
V_{CC}	Supply Voltage Com'l/Ind'l	4.5	5.0	5.5	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	0	0	0	V
V_{IH}	Input High Voltage Com'l/Ind'l	2.0	-	5.5	2.0	-	5.5	V
V_{IL}	Input Low Voltage Com'l/Ind'l	-	-	0.8	-	-	0.8	V
T_A	Operating Temperature Commercial	0	-	70	0	-	70	°C
T_A	Operating Temperature Industrial	-40	-	85	-40	-	85	°C
DC Electrical Characteristics								
I_{LI}(1)	Input Leakage Current (any input)	-10	-	10	-10	-	10	µA
I_{LO}	Output Leakage Current	-10	-	10	-10	-	10	µA
V_{OH}	Output Logic "1" Voltage, IOH=-2mA	2.4	-	-	2.4	-	-	V
V_{OL}	Output Logic "0" Voltage, IOL = 8mA	-	-	0.4	-	-	0.4	V
Power Consumption								
$I_{CC}1$(2,3)	Active Power Supply Current	-	-	30	-	-	30	mA
$I_{CC}2$(4)	Standby Current	-	-	5	-	-	5	mA

Table 3. DC Specifications

Capacitance at 1.0MHz Ambient Temperature (25°C)				
Symbol	**Parameter**	**Conditions**	**Max.**	**Unit**
C_{IN}(2)	Input Capacitance	V_{IN}= 0V	10	pF
C_{OUT}(2,4)	Output Capacitance	V_{OUT}= 0V	10	pF

NOTES:
1. Measurement with 0.4<=V_{IN}<=Vcc
2. With output tri-stated ($\overline{OE}$ = High)
3. Icc(1,2) is measured with WCLK and RCLK at 20 MHz
4. Design simulated, not tested.

Table 3. DC Specifications (Continued)

Symbol	Parameter	Commercial & Industrial						Unit
		FQ245-10 FQ235-10 FQ225-10 FQ215-10 FQ205-10		FQ245-15 FQ235-15 FQ225-15 FQ215-15 FQ205-15		FQ245-20 FQ235-20 FQ225-20 FQ215-20 FQ205-20		
		Min.	Max.	Min.	Max.	Min.	Max.	
fs	Clock Cycle Frequency	-	100	-	66	-	50	MHz
tA	Data Access Time	2	6.5	2	10	2	12	ns
tWCLK	Write Clock Cycle Time	10	-	15	-	20	-	ns
tWCLKH	Write Clock High Time	4.5	-	6	-	8	-	ns
tWCLKL	Write Clock Low Time	4.5	-	6	-	8	-	ns
tRCLK	Read Clock Cycle Time	10	-	15	-	20	-	ns
tRCLKH	Read Clock High Time	4.5	-	6	-	8	-	ns
tRCLKL	Read Clock Low Time	4.5	-	6	-	8	-	ns
tDS	Data Set-up Time	3	-	4	-	5	-	ns
tDH	Data Hold Time	0.5	-	1	-	1	-	ns
tENS	Enable Set-up Time	3	-	4	-	5	-	ns
tENH	Enable Hold Time	0.5	-	1	-	1	-	ns
tRST	Reset Pulse Width(1)	10	-	15	-	20	-	ns
tRSTS	Reset Set-up Time	8	-	10	-	12	-	ns
tRSTR	Reset Recovery Time	8	-	10	-	12	-	ns
tRSTF	Reset to Flag and Output Time	-	15	-	20	-	20	ns
tOLZ	Output Enable to Output in Low-Z(2)	0	-	0	-	0	-	ns
tOE	Output Enable to Output Valid	3	6	3	8	3	10	ns
tOHZ	Output Enable to Output in High-Z(2)	3	6	3	8	3	10	ns
tFULL	Write Clock to Full Flag	-	6.5	-	10	-	12	ns
tEMPTY	Read Clock to Empty Flag	-	6.5	-	10	-	12	ns
tPRAF	Clock to Programmable Almost-Full Flag	-	17	-	24	-	26	ns
tPRAE	Clock to Programmable Almost-Empty Flag	-	17	-	24	-	26	ns
tHALF	Clock to Half-Full Flag	-	17	-	24	-	26	ns
tXO	Clock to Expansion Out	-	6.5	-	10	-	12	ns
tXI	Expansion In Pulse Width	3	-	6.5	-	8	-	ns
tXIS	Expansion In Set-Up Time	3.5	-	5	-	8	-	ns
tSKEW1	Skew time between Read Clock & Write Clock for Full Flag	5	-	6	-	8	-	ns
tSKEW2	Skew time between Read Clock & Write Clock for Empty Flag	5	-	6	-	8	-	ns

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Design simulated, not tested.

Table 4. AC Electrical Characteristics

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load*, clock = 10ns, 15ns, 20ns	See Figure 4

*Include jig and scope capacitances

Table 5. AC Test Condition

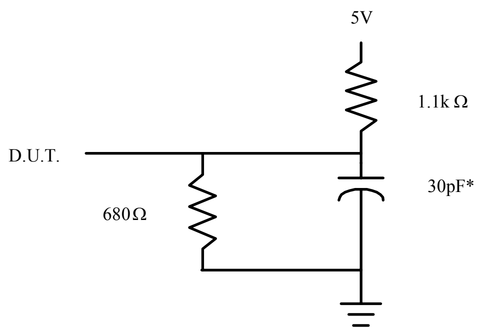


Figure 4. Output Load
for clock = 10ns, 15ns, 20ns
*Includes jig and scope capacitances.

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Pin Functions

$\overline{RST}$	Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{RST}$ low. $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. All data outputs will go low. Previous programmed configurations will not be maintained.
WCLK	Writes data into queue during low to high transitions of WCLK if $\overline{WEN}$ is set low. Synchronizes $\overline{FULL}$ and $\overline{PRAF}$ flags. WCLK and RCLK are independent of each other.
$\overline{WEN}$	Controls write operation into queue or offset registers during low to high transition of WCLK.
$\overline{LOAD}$	$\overline{LOAD}$ controls write/read, to/from offset registers during low to high transition of WCLK/RCLK respectively for parallel programming. Use in conjunction with $\overline{WEN}$ / $\overline{REN}$.
$\overline{FIRST}$	In single device configuration, $\overline{FIRST}$ is set low. In depth expansion configuration, $\overline{FIRST}$ is set low for the first device and set high for other devices in the Daisy Chain.
$\overline{WEXI}$	In single device configuration, $\overline{WEXI}$ is set low. In depth expansion configuration, $\overline{WEXI}$ is connected to $\overline{WEXO}$ of previous device in the Daisy Chain.
D_{17-0}	18 - bit wide input data bus.
RCLK	Reads data from queue during low to high transitions of RCLK if $\overline{REN}$ is set low. Synchronizes the $\overline{EMPTY}$ and $\overline{PRAE}$ flags. RCLK and WCLK are independent of each other.
$\overline{REN}$	Reads data from queue during low to high transitions of RCLK if $\overline{REN}$ is set to low. This also advances the Read pointer of the queue.
$\overline{OE}$	Setting $\overline{OE}$ low activates the data output drivers. Setting $\overline{OE}$ high deactivates the data output drivers (High-Z). $\overline{OE}$ does not control advancement of Read pointer.
Q_{17-0}	18 - bit wide output data bus.
$\overline{REXO}$	In depth expansion configuration, $\overline{REXO}$ is connected to $\overline{REXI}$ of next device in the Daisy Chain.
$\overline{FULL}$	Queue is full when $\overline{FULL}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. Refer to Table 8 for behavior of $\overline{FULL}$.
$\overline{EMPTY}$	Queue is empty when $\overline{EMPTY}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. Refer to Table 8 for behavior of $\overline{EMPTY}$.
$\overline{PRAF}$	Queue is almost full when $\overline{PRAF}$ goes low during the low to high transition of WCLK. $\overline{PRAF}$ goes high during the low to high transition of RCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{PRAF}$. Refer to Table 8 for behavior of $\overline{PRAF}$.
$\overline{PRAE}$	Queue is almost empty when $\overline{PRAE}$ goes low during the low to high transition of RCLK. $\overline{PRAE}$ goes high during the low to high transition of WCLK. Default (Empty+offset) or programmed offset values determine the status of $\overline{PRAE}$. Refer to Table 8 for behavior of $\overline{PRAE}$.
$\overline{WEXO}$ / $\overline{HALF}$	In single device configuration, queue is more than half full when $\overline{HALF}$ goes low during the low to high transition of WCLK. Queue is less than half full when $\overline{HALF}$ goes high during the low to high transition of RCLK. Refer to Table 8 for details. In depth expansion configuration, $\overline{WEXO}$ is connected to $\overline{WEXI}$ of next device in the Daisy Chain
$\overline{REXI}$	In single device configuration, $\overline{REXI}$ is set low. In depth expansion configuration, $\overline{REXI}$ is connected to $\overline{REXO}$ of previous device in the Daisy Chain.

$\overline{LOAD}$	$\overline{WEN}$	$\overline{REN}$	WCLK	RCLK	FQ245 FQ235 FQ225 FQ215 FQ205 Selection / Sequence
0	0	1	↑	X	Parallel write to offset registers: Empty Offset, Full Offset Parallel write to registers: 1. $\overline{PRAE}$ 2. $\overline{PRAF}$
0	1	0	X	↑	Parallel read from offset registers: Empty Offset, Full Offset Parallel read from registers: 1. $\overline{PRAE}$ 2. $\overline{PRAF}$
X	1	1	X	X	No Operation
1	0	X	↑	X	Write Memory
1	X	0	X	↑	Read Memory
1	1	1	X	X	No Operation

Figure 5. Programmable Flag Offset Programming Sequence

Device	$\overline{PRAF}$ Programming (bits)	$\overline{PRAE}$ Programming (bits)
FQ245	D/Q_{11-0}	D/Q_{11-0}
FQ235	D/Q_{10-0}	D/Q_{10-0}
FQ225	D/Q_{9-0}	D/Q_{9-0}
FQ215	D/Q_{8-0}	D/Q_{8-0}
FQ205	D/Q_{7-0}	D/Q_{7-0}

Table 6. Parallel Offset Register Data Mapping Table

Device	Default
FQ245	007FH
FQ235	007FH
FQ225	007FH
FQ215	003FH
FQ205	001FH

Table 7. Default Values of Offset Registers

FQ245 4,096 x 18

Data Width	D/Q17	D/Q16	D/Q15	D/Q14	D/Q13	D/Q12	D/Q11	D/Q10	D/Q9	D/Q8	D/Q7	D/Q6	D/Q5	D/Q4	D/Q3	D/Q2	D/Q1	D/Q0
1st Cycle $\overline{PRAE}$							11	10	9	8	7	6	5	4	3	2	1	0
2nd Cycle $\overline{PRAF}$							11	10	9	8	7	6	5	4	3	2	1	0

FQ235 2,048 x 18

Data Width	D/Q17	D/Q16	D/Q15	D/Q14	D/Q13	D/Q12	D/Q11	D/Q10	D/Q9	D/Q8	D/Q7	D/Q6	D/Q5	D/Q4	D/Q3	D/Q2	D/Q1	D/Q0
1st Cycle $\overline{PRAE}$								10	9	8	7	6	5	4	3	2	1	0
2nd Cycle $\overline{PRAF}$								10	9	8	7	6	5	4	3	2	1	0

FQ225 1,024 x 18

Data Width	D/Q17	D/Q16	D/Q15	D/Q14	D/Q13	D/Q12	D/Q11	D/Q10	D/Q9	D/Q8	D/Q7	D/Q6	D/Q5	D/Q4	D/Q3	D/Q2	D/Q1	D/Q0
1st Cycle $\overline{PRAE}$									9	8	7	6	5	4	3	2	1	0
2nd Cycle $\overline{PRAF}$									9	8	7	6	5	4	3	2	1	0

FQ215 512 x 18

Data Width	D/Q17	D/Q16	D/Q15	D/Q14	D/Q13	D/Q12	D/Q11	D/Q10	D/Q9	D/Q8	D/Q7	D/Q6	D/Q5	D/Q4	D/Q3	D/Q2	D/Q1	D/Q0
1st Cycle $\overline{PRAE}$										8	7	6	5	4	3	2	1	0
2nd Cycle $\overline{PRAF}$										8	7	6	5	4	3	2	1	0

FQ205 256 x 18

Data Width	D/Q17	D/Q16	D/Q15	D/Q14	D/Q13	D/Q12	D/Q11	D/Q10	D/Q9	D/Q8	D/Q7	D/Q6	D/Q5	D/Q4	D/Q3	D/Q2	D/Q1	D/Q0
1st Cycle $\overline{PRAE}$											7	6	5	4	3	2	1	0
2nd Cycle $\overline{PRAF}$											7	6	5	4	3	2	1	0

of Bits for Offset Registers
12 bits for FQ245 11 bits for FQ235 10 bits for FQ225 9 bits for FQ215 8 bits for FQ205
Note: Don't Care applies to all unused bits

Figure 6. Parallel Offset Write/Read Cycles Diagram

FQ245	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 2,048	H	H	H	H	H
2,049 to [4,096-(x+1)]	H	H	L	H	H
(4,096 -x(2)) to 4,095	H	L	L	H	H
4,096	L	L	L	H	H

FQ235	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 1,024	H	H	H	H	H
1,025 to [2,048-(x+1)]	H	H	L	H	H
(2,048 -x(2)) to 2,047	H	L	L	H	H
2,048	L	L	L	H	H

FQ225	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 512	H	H	H	H	H
513 to [1,024-(x+1)]	H	H	L	H	H
(1,024 –x(2)) to 1,023	H	L	L	H	H
1,024	L	L	L	H	H

FQ215	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 256	H	H	H	H	H
257 to [512-(x+1)]	H	H	L	H	H
(512 -x(2)) to 511	H	L	L	H	H
512	L	L	L	H	H

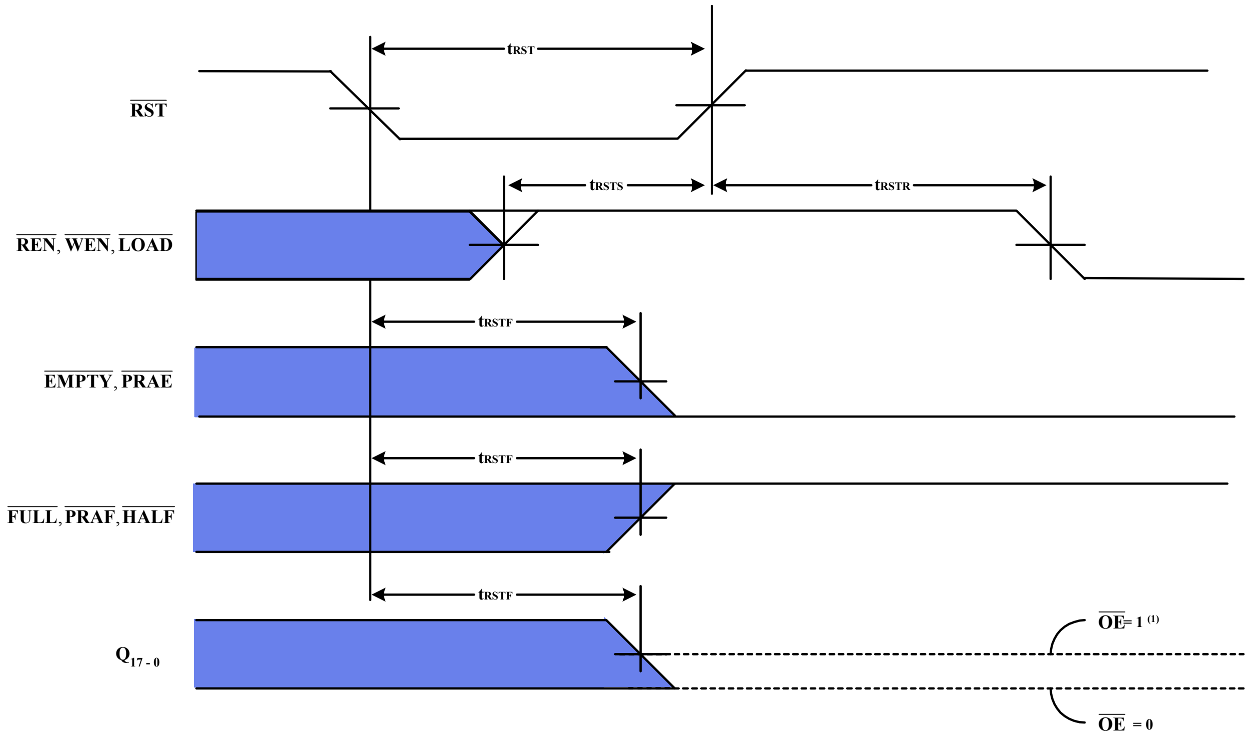
FQ205	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 128	H	H	H	H	H
129 to [256-(x+1)]	H	H	L	H	H
(256 –x(2)) to 255	H	L	L	H	H
256	L	L	L	H	H

NOTES:

1. y = $\overline{\text{PRAE}}$ offset. Default Values: FQ205 y = 31, FQ215 y = 63, FQ245/FQ235/FQ225 y = 127.
2. x = $\overline{\text{PRAF}}$ offset. Default Values: FQ205 x = 31, FQ215 x = 63, FQ245/FQ235/FQ225 x = 127.

Table 8. Status Flags

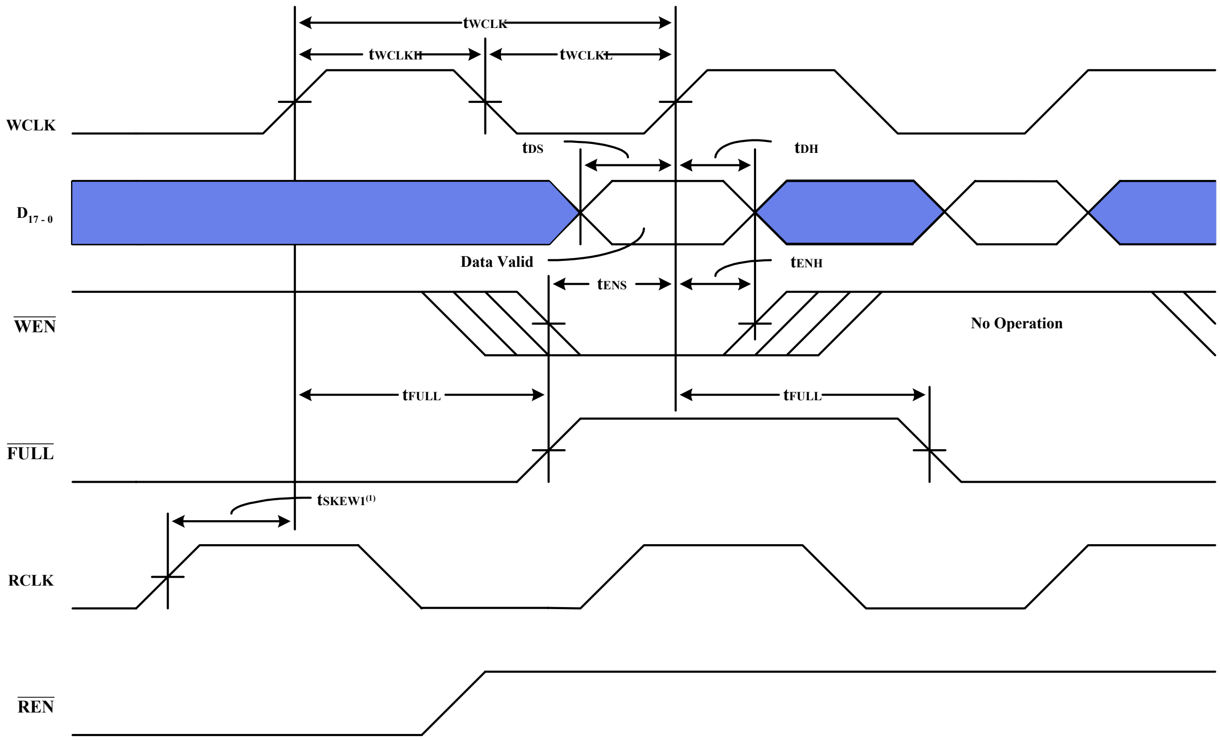
Timing Diagrams



NOTES:

1. After reset, the outputs will be low if $\overline{OE}$ = 0 or tri-state if $\overline{OE}$ =1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

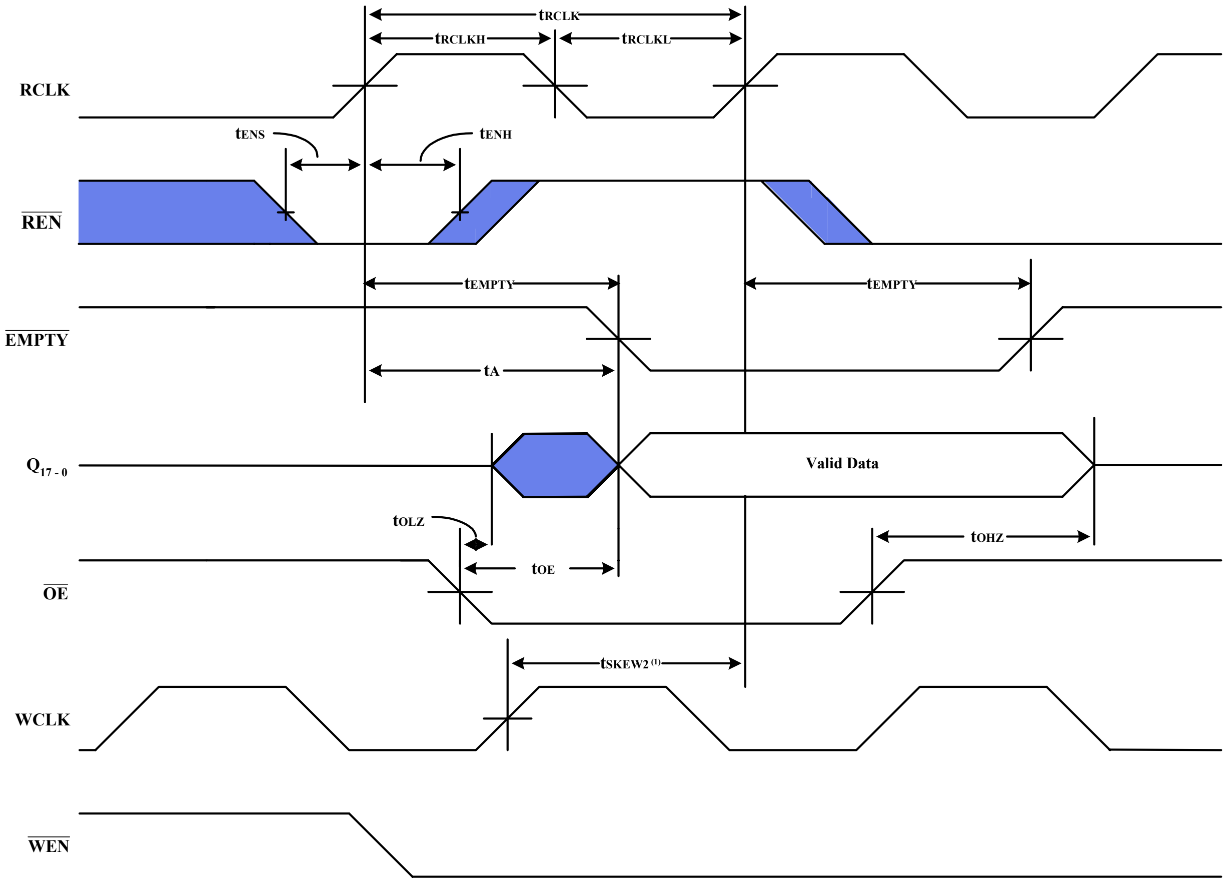
Diagram 1. Reset Timing



NOTES:

1. tSKEW1 is the minimum time between a rising RCLK edge and rising WCLK edge to guarantee that FULL will go high during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is equal to or less than tSKEW1, then FULL may not change state until the next WCLK edge.

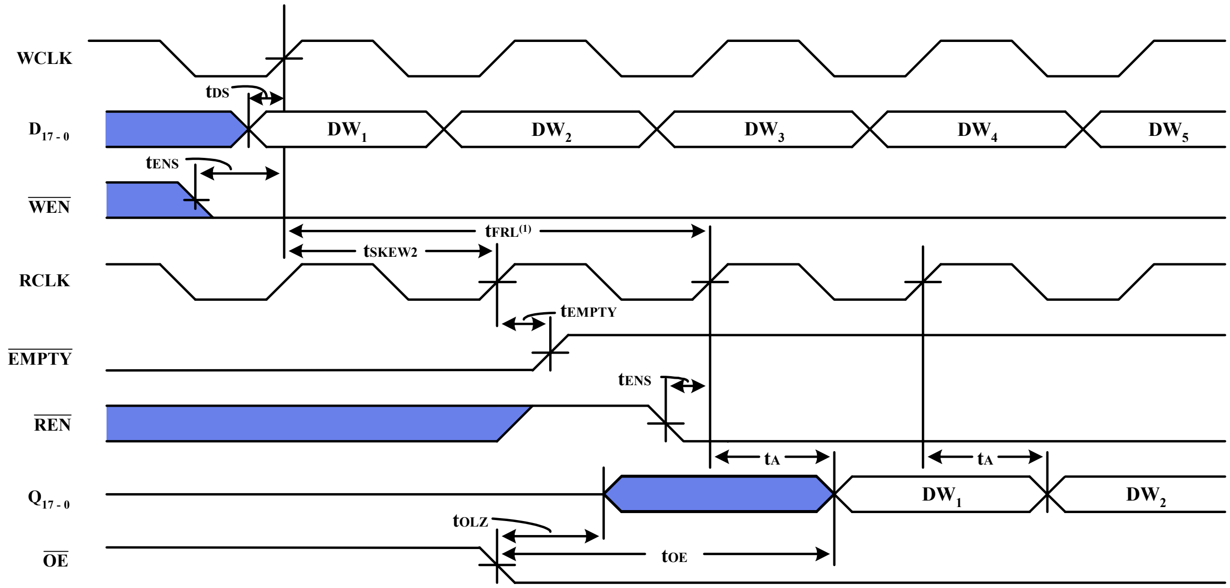
Diagram 2. Write Cycle Timing



NOTES:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EMPTY}$ will go high during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EMPTY}$ may not change state until the next RCLK edge.

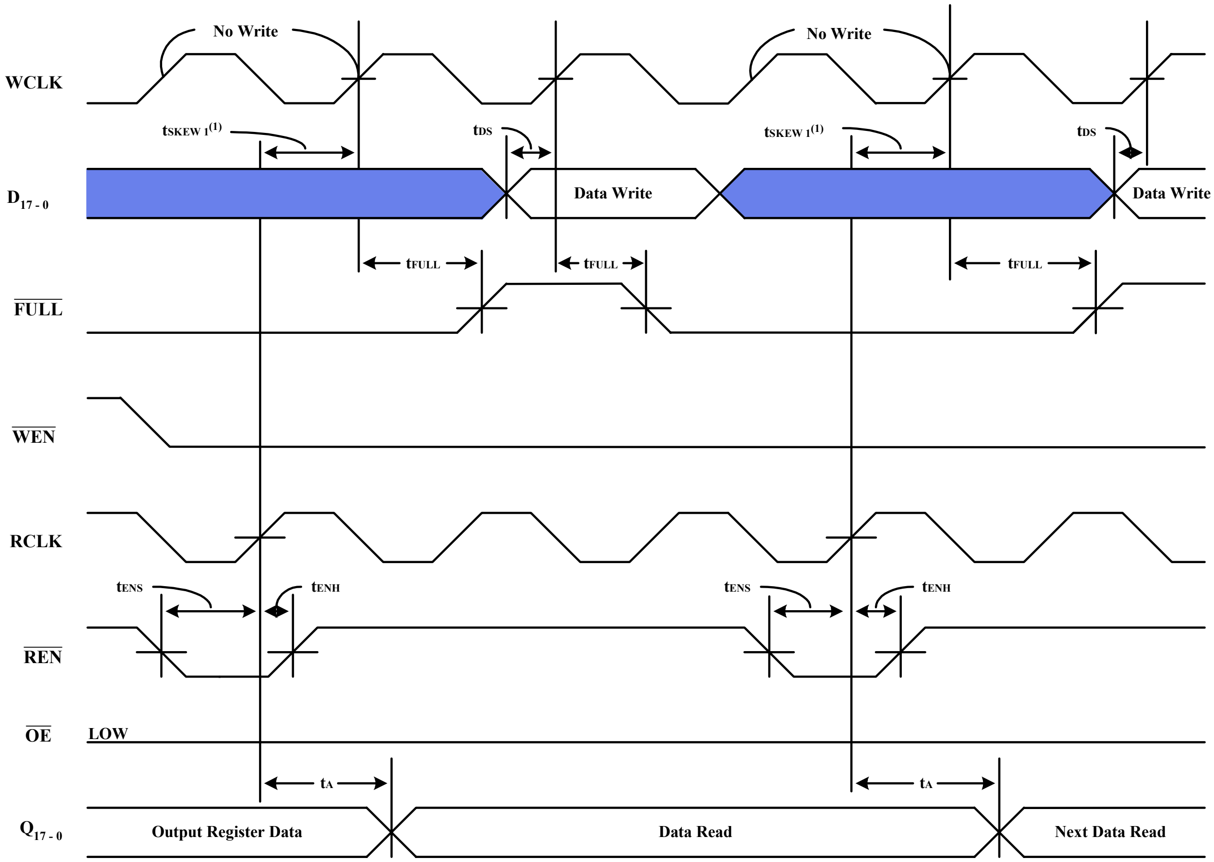
Diagram 3. Read Cycle Timing



NOTES:

1. t_{FRL} is the latency from first write to first Read. When t_{SKEW2} is greater than or equal to minimum specification, t_{FRL} (maximum) = t_{RCLK} + t_{SKEW2}. When t_{SKEW2} is less than minimum specification, t_{FRL} (maximum) equals either 2* t_{RCLK} + t_{SKEW2} or t_{RCLK} + t_{SKEW2}.
   The Latency Timing applies only at the Empty Boundary ($\overline{EMPTY}$ = Low).

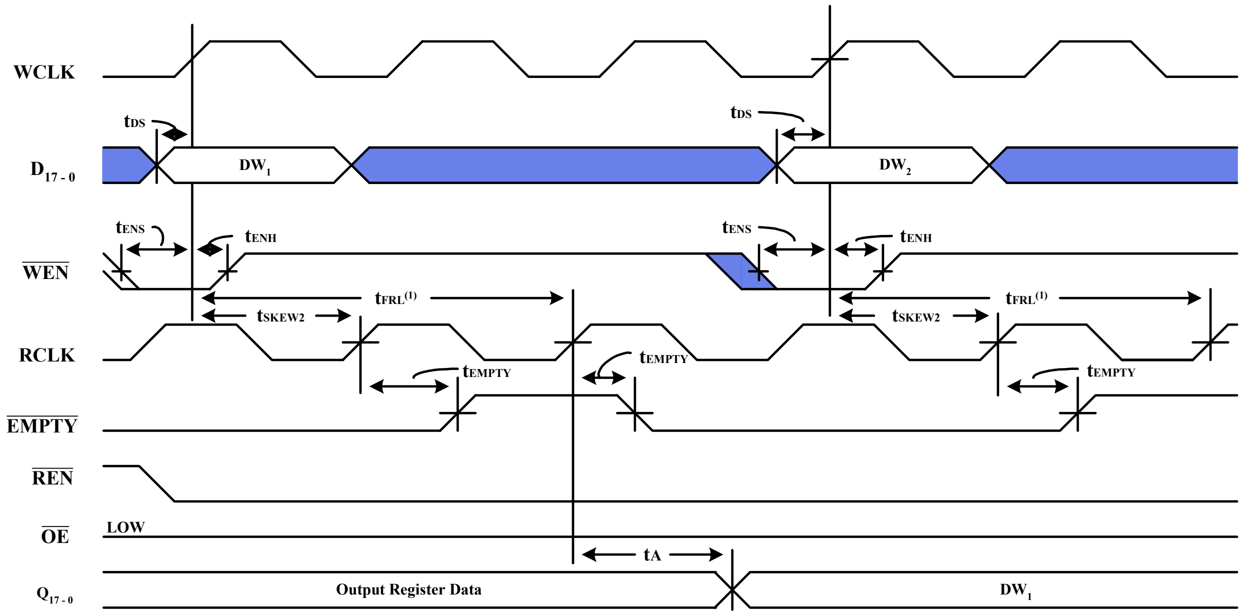
Diagram 4. First Data Word Latency after Reset with Simultaneous Read and Write



NOTES:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FULL}$ will go high during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FULL}$ may not change state until the next WCLK edge.

Diagram 5. Full Flag Timing



NOTES:

1. t_{FRL} is the latency from first write to first Read. When t_{SKEW2} is greater than or equal to minimum specification, t_{FRL} (maximum) = t_{RCLK} + t_{SKEW2}. When t_{SKEW2} less than minimum specification, t_{FRL} (maximum) equals either 2 * t_{RCLK} + t_{SKEW2}, or t_{RCLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EMPTY}$ = Low).

Diagram 6. Empty Flag Timing

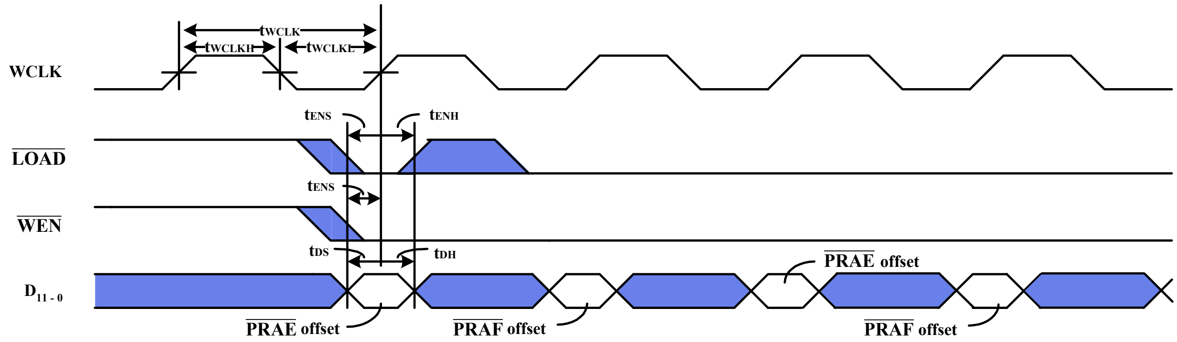


Diagram 7. Write Programmable Registers

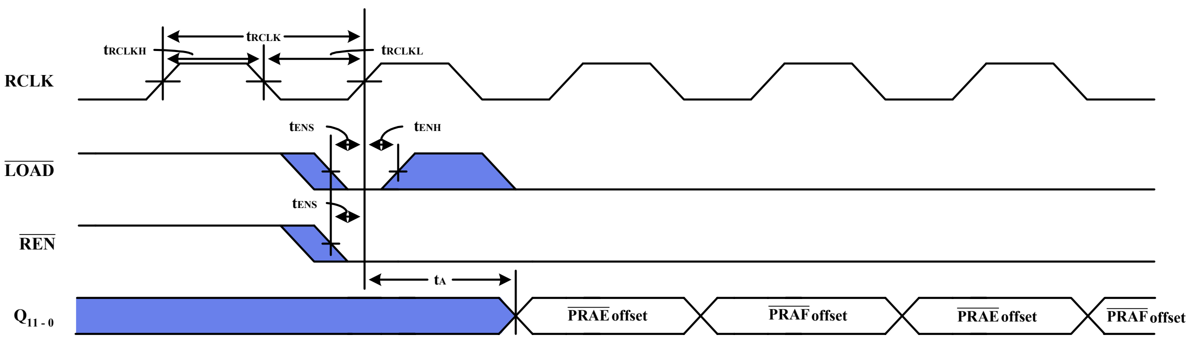
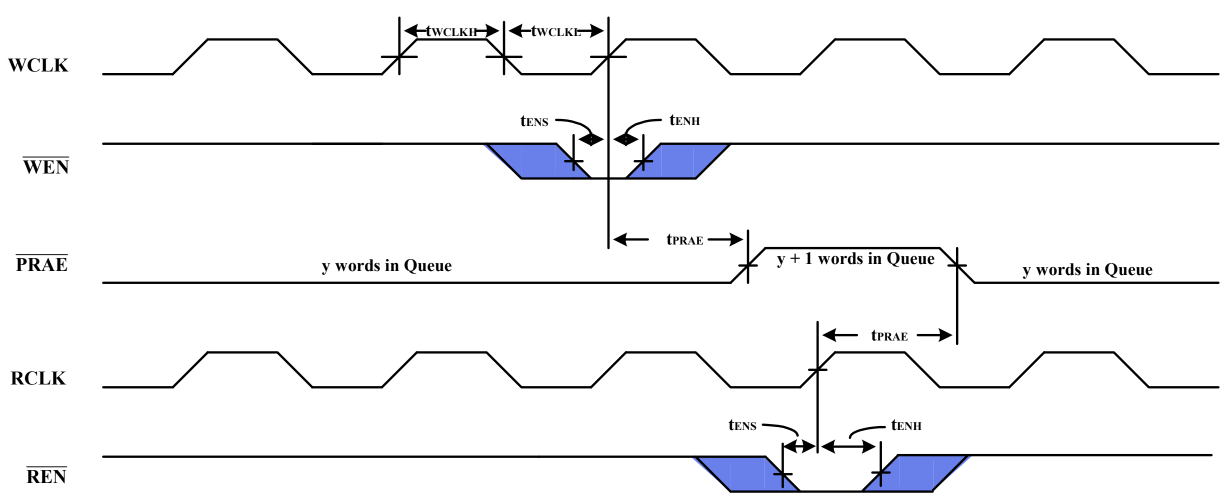


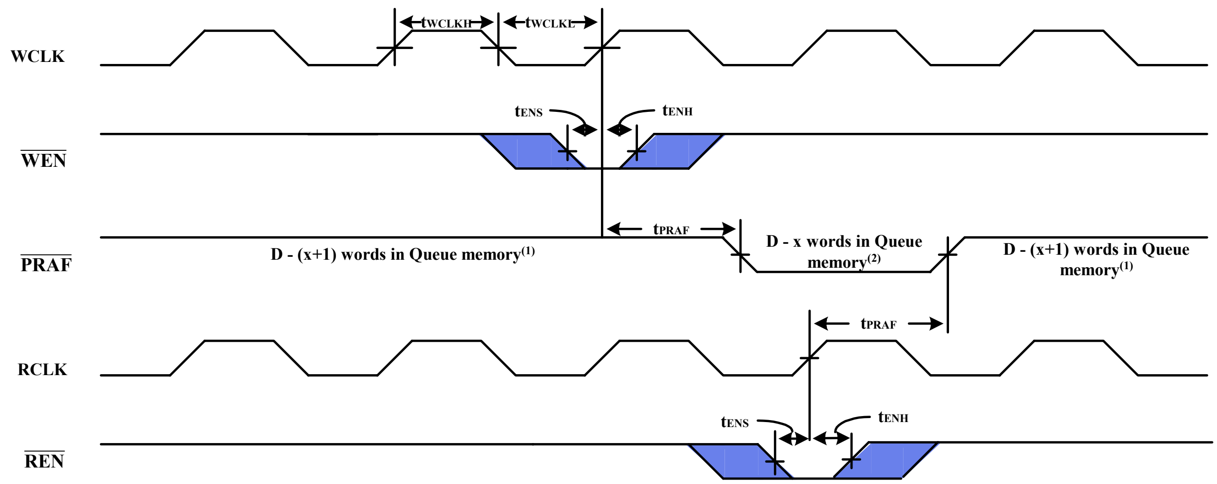
Diagram 8. Read Programmable Registers



NOTES:

1. y = $\overline{\text{PRAE}}$ offset.

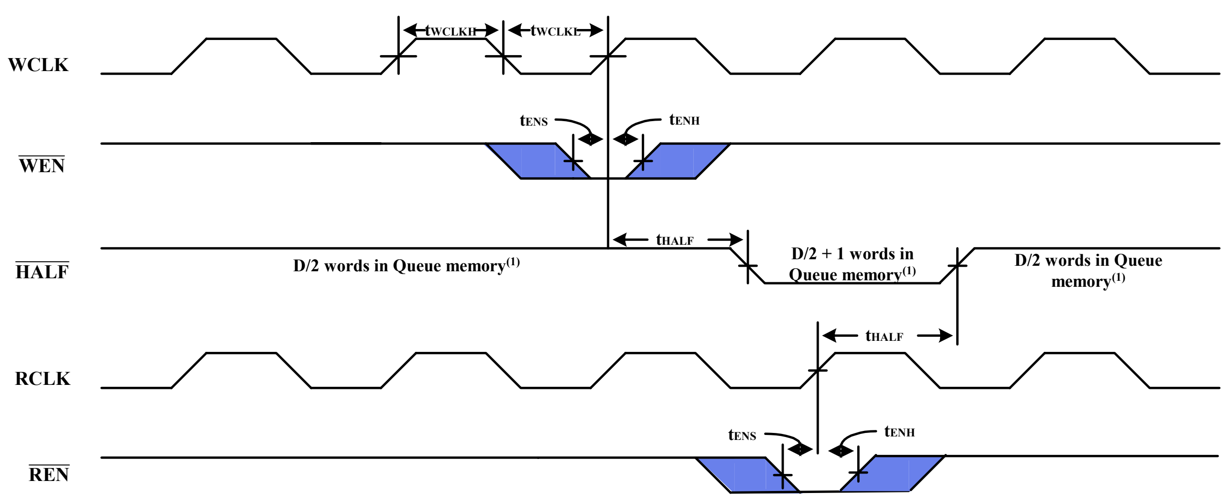
Diagram 9. Programmable Almost-Empty Flag Timing



NOTES:

1. x = $\overline{\text{PRAF}}$ offset.
2. D = maximum queue depth = 256 words for FQ205; 512 words for FQ215; 1,024 words for FQ225; 2,048 words for FQ235; and 4,096 words for FQ245.

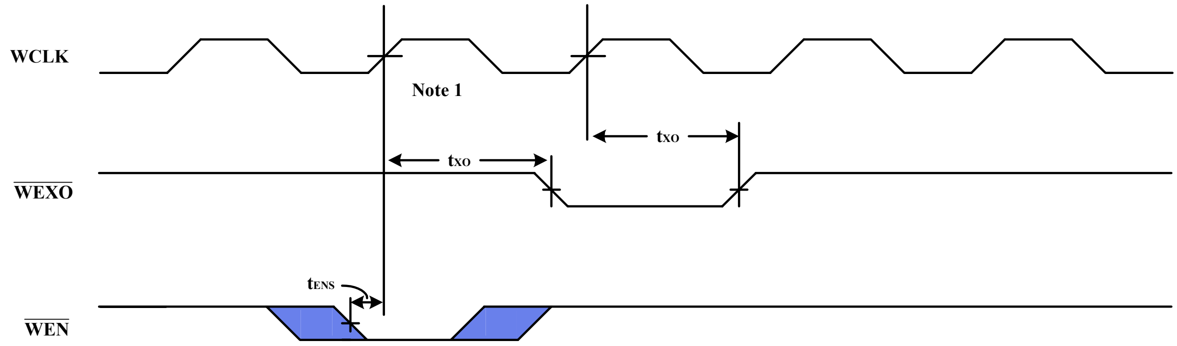
Diagram 10. Programmable Almost-Full Flag Timing



NOTES:

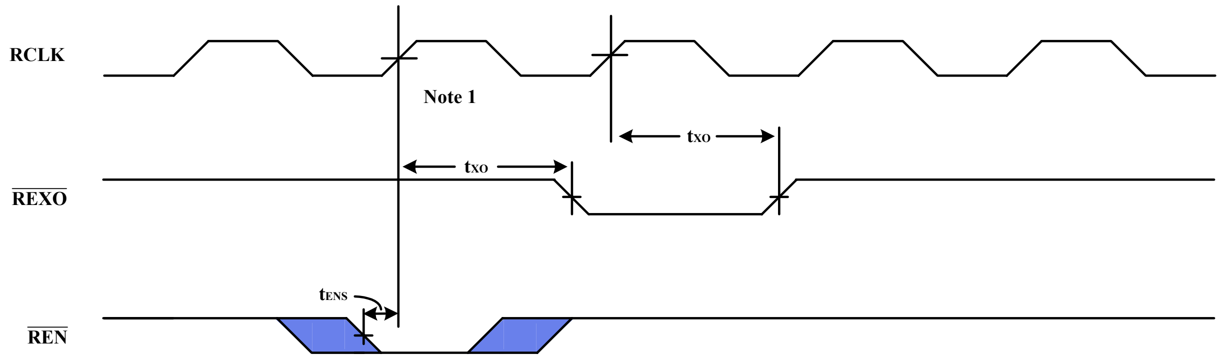
1. D = maximum queue depth = 256 words for FQ205; 512 words for FQ215; 1,024 words for FQ225; 2,048 words for FQ235; and 4,096 words for FQ245.

Diagram 11. Half-Full Flag Timing



NOTES:
1. Write to Last Physical Location.

Diagram 12. Write Expansion Out Timing



NOTES:
1. Read from Last Physical Location.

Diagram 13. Read Expansion Out Timing

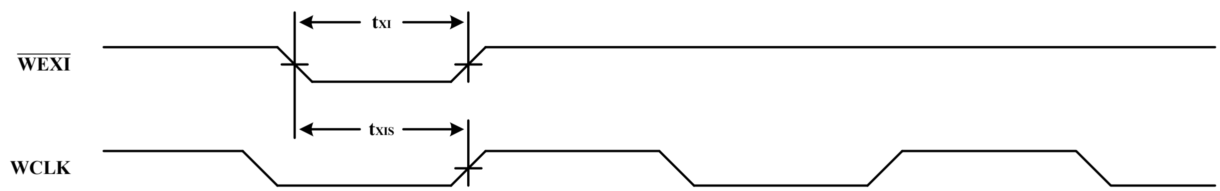


Diagram 14. Write Expansion in Timing

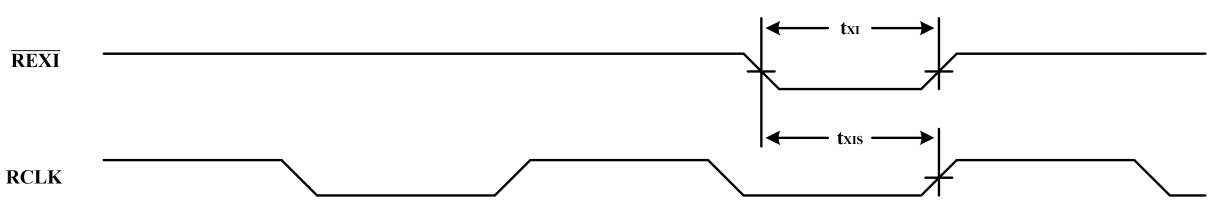
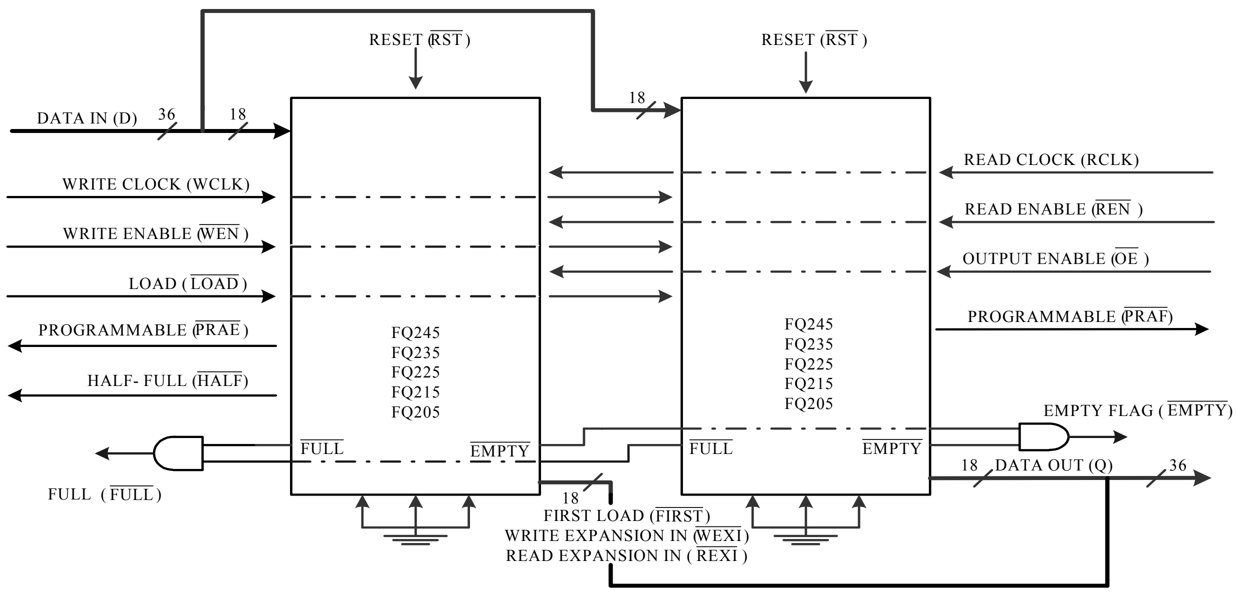


Diagram 15. Read Expansion in Timing

Width Expansion Configuration

Simply connecting together the control signals of multiple devices may increase word width. Status flags can be detected from any one device. The exceptions are the Empty Flag and Full Flag. Because of variations in skew between RCLK and WCLK, it is possible for flag assertion and de-assertion to vary by one cycle between FIFOs. To avoid problems the user must create composite flags by ANDing the Empty Flags of every FIFO, and separately ANDing all Full Flags. Figure 7 demonstrates a 36-bit width by using two FQ245 / 235 / 225 / 215 / 205s. Any word width can be attained by adding additional FQ245 / 235 / 225 / 215 / 205s.

Block Diagram of Synchronous Queue
4,096 x 36 / 2,048 x 36 / 1,024 x 36 / 512 x 36 / 256 x 36



NOTES:
1. Do not connect any output control signals directly together.

Figure 7. Width Expansion Configuration

Depth Expansion Configuration (with Programmable Flags)

These devices can easily be adapted to applications requiring more than 4,096 / 2,048 / 1,024 / 512 / 256 words of buffering. Figure 8 shows Depth Expansion using three FQ245 / 235 / 225 / 215 / 205s. Maximum depth is limited only by signal loading. Follow these steps:

- The first device must be designated by grounding the First Load (FIRST) control input.
- All other devices must have FIRST in the high state.
- The Write Expansion Out (WEXO) pin of each device must be tied to the Write Expansion In (WEXI) pin of the next device.
- The Read Expansion Out (REXO) pin of each device must be tied to the Read Expansion In (REXI) pin of the next device.
- All Load (LOAD) pins are tied together.
- The Half-Full Flag (HALF) is not available in this Depth Expansion Configuration.
- EMPTY , FULL , PRAF , and PRAE are created with composite flags by ORing together every respective flags for monitoring. The composite PRAF and PRAE flags are not precise.

Block Diagram of Synchronous Queue
12,288 x 18 / 6,144 x 18 / 3,072 x 18 / 1,536 x 18 / 768 x 18

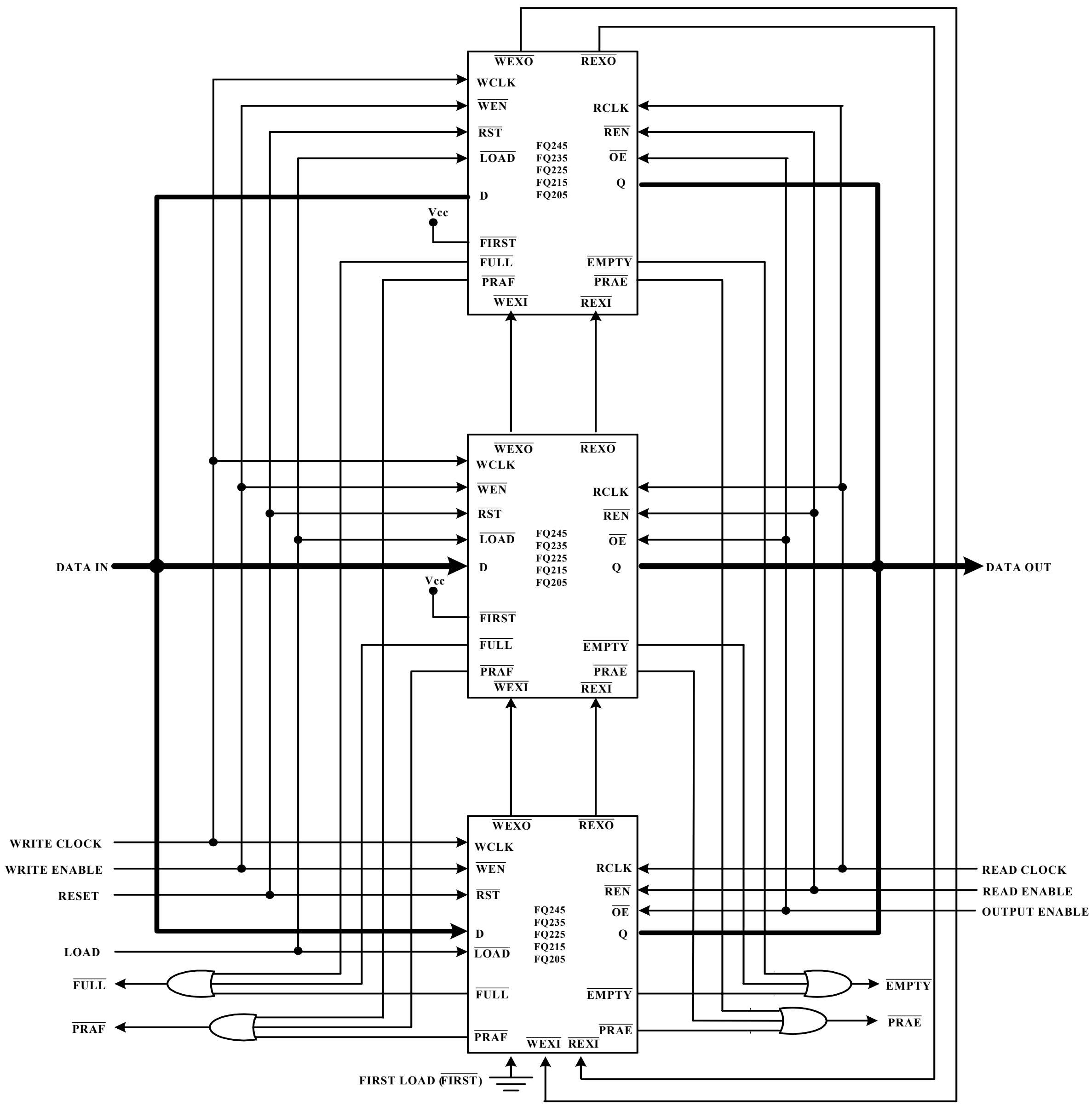


Figure 8. Block Diagram of Multiple Devices with Programmable Flags used in Depth Expansion Configuration

Order Information:

HBA Device Family	Device Type	Power†	Speed (ns)*	Package**	Temperature Range
XX	XXX	X	XX	XX	X
FQ	**245** (4,096 x 18)	Low	**10** – 100 MHz	**PF**	Blank – Commercial (0°C to 70°C)
	235 (2,048 x 18)		**15** – 66 MHz	**TF**	**I** – Industrial (-40° to 85°C)
	225 (1,024 x 18)		**20** – 50 MHz		
	215 (512 x 18)				
	205 (256 x 18)				

†**Power** – Low (LB)
***Speed** – Slower speeds available upon request.
****Package** – 64 pin Plastic Thin Quad Flat Pack (TQFP), 64 pin Slim Thin Quad Flat Pack (STQFP)

Example:

FQ235LB15TF (32k x 18, 15ns, Commercial temp)
FQ225LB10PFI (16k x 18, 10ns, Industrial temp)

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4/29/03 pg. 3, 5, 6, 7, 8, 9, 11, 14, 15, 16, 17, 18, 22, 24

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