Am29LV400B KGD

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with “Am” and “MBM”. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **23427** Revision **C** Amendment **0** Issue Date **October 15, 2003**

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SUPPLEMENT

Am29LV400B Known Good Die

4 Megabit (512 K x 8-Bit/256 K x 16-Bit)
CMOS 3.0 Volt-only, Boot Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — 2.7 to 3.6 V for read, program, and erase operations
  - — Ideal for battery-powered applications
- **Manufactured on 0.32 µm process technology**
- **High performance**
  - — 60R, 70, 80, 90, or 120 ns access time
- **Low power consumption (typical values at 5 MHz)**
  - — 200 nA Automatic Sleep mode current
  - — 200 nA standby mode current
  - — 7 mA read current
  - — 15 mA program/erase current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and seven 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and seven 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-system or via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write cycle guarantee per sector**
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device to reading array data
- **20-year data retention at 125°C**
- **Tested to datasheet specifications at temperature**
- **Quality and reliability levels equivalent to standard packaged components**

Publication# **23427** Rev: **C** Amendment/**0**
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GENERAL DESCRIPTION

The Am29LV400B in Known Good Die (KGD) form is an 4 Mbit, 3.0 volt-only Flash memory. AMD defines KGD as standard product in die form, tested for functionality and speed. AMD KGD products have the same reliability and quality as AMD products in packaged form.

Am29LV400B Features

The Am29LV400B is an 4 Mbit, 3.0 volt-only Flash memory organized as 524,288 bytes or 262,144 words. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. No V_{PP} is required for program or erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET#** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

Electrical Specifications

Refer to the Am29LV400B data sheet, publication number 21523, for full electrical specifications on the Am29LV400B in KGD form.

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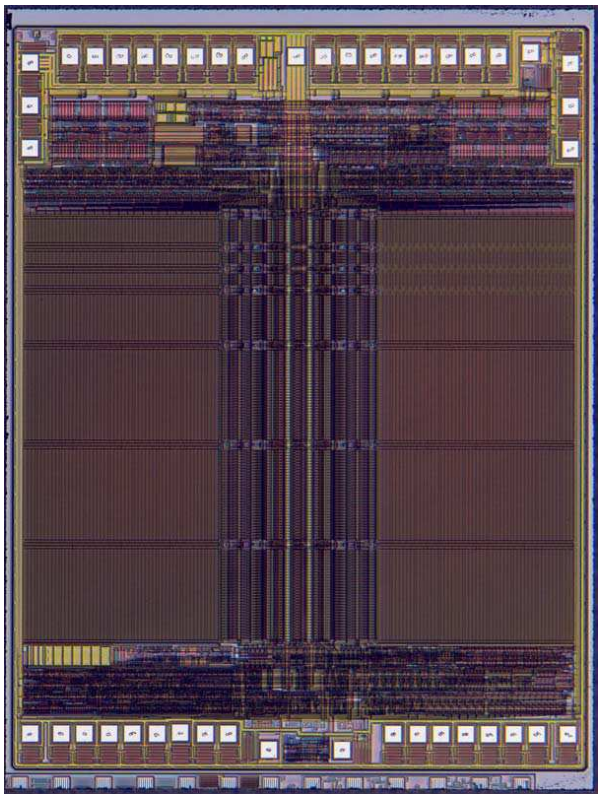
PRODUCT SELECTOR GUIDE

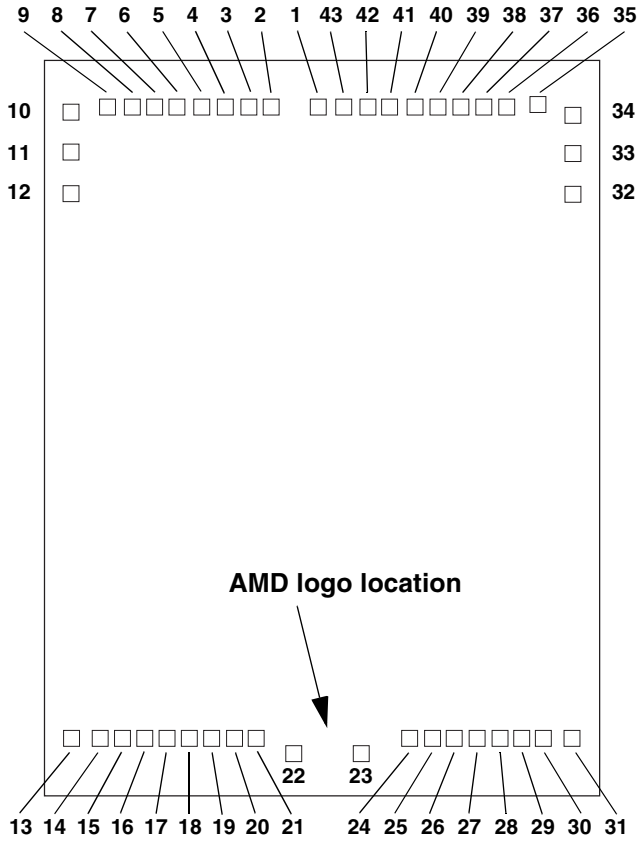
Family Part Number		Am29LV400B KGD				
Speed Option & Voltage Operating Range, V_{CC}	3.0 – 3.6 V	**-60R**				
	2.7 – 3.6 V		**-70**	**-80**	**-90**	**-120**
Max Access Time, t_{ACC} (ns)		60	70	80	90	120
Max CE# Access, t_{CE} (ns)		60	70	80	90	120
Max OE# Access, t_{OE} (ns)		30	30	30	35	50

Note: *Refer to "Test Conditions" for additional information related to speed options.*

DIE PHOTOGRAPH



DIE PAD LOCATIONS



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PAD DESCRIPTION

Pad locations relative to die center.

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	–0.90	80.50	–0.02	2.04
2	DQ4	–13.00	80.50	–0.33	2.04
3	DQ12	–18.90	80.50	–0.48	2.04
4	DQ5	–24.80	80.50	–0.63	2.04
5	DQ13	–30.70	80.50	–0.78	2.04
6	DQ6	–36.50	80.50	–0.93	2.04
7	DQ14	–42.40	80.50	–1.08	2.04
8	DQ7	–48.30	80.50	–1.23	2.04
9	DQ15/A–1	–54.20	80.50	–1.38	2.04
10	V_{SS}	–63.60	78.90	–1.62	2.00
11	BYTE#	–63.60	68.90	–1.62	1.75
12	A16	–63.60	58.80	–1.62	1.49
13	A15	–63.30	–79.00	–1.61	–2.01
14	A14	–55.90	–79.00	–1.42	–2.01
15	A13	–50.50	–79.00	–1.28	–2.01
16	A12	–44.70	–79.00	–1.14	–2.01
17	A11	–39.30	–79.00	–1.00	–2.01
18	A10	–33.40	–79.00	–0.85	–2.01
19	A9	–28.00	–78.70	–0.71	–2.00
20	A8	–22.10	–79.00	–0.56	–2.01
21	WE#	–16.60	–79.00	–0.42	–2.01
22	RESET#	–7.10	–82.80	–0.18	–2.10
23	RY/BY#	10.20	–82.80	0.26	–2.10
24	A17	22.20	–79.00	0.56	–2.01
25	A7	28.00	–79.00	0.71	–2.01
26	A6	33.40	–79.00	0.85	–2.01
27	A5	39.30	–79.00	1.00	–2.01
28	A4	44.70	–79.00	1.14	–2.01
29	A3	50.50	–79.00	1.28	–2.01
30	A2	55.90	–79.00	1.42	–2.01
31	A1	63.30	–79.00	1.61	–2.01
32	A0	63.60	58.60	1.62	1.49
33	CE#	63.60	68.70	1.62	1.75
34	V_{SS}	63.60	78.70	1.62	2.00
35	OE#	54.20	81.40	1.38	2.07
36	DQ0	46.60	80.50	1.18	2.04
37	DQ8	40.70	80.50	1.03	2.04
38	DQ1	34.90	80.50	0.89	2.04
39	DQ9	28.90	80.50	0.73	2.04
40	DQ2	23.10	80.50	0.59	2.04
41	DQ10	17.20	80.50	0.44	2.04
42	DQ3	11.40	80.50	0.29	2.04
43	DQ11	5.40	80.50	0.14	2.04

Note: *The coordinates above are relative to die center and can be used to operate wire bonding equipment.*

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PAD DESCRIPTION

Pad locations relative to V_{CC}.

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	0.00	0.00	0.00	0.00
2	DQ4	–12.10	0.00	–0.31	0.00
3	DQ12	–18.00	0.00	–0.46	0.00
4	DQ5	–23.90	0.00	–0.61	0.00
5	DQ13	–29.80	0.00	–0.76	0.00
6	DQ6	–35.60	0.00	–0.90	0.00
7	DQ14	–41.50	0.00	–1.05	0.00
8	DQ7	–47.40	0.00	–1.20	0.00
9	DQ15/A–1	–53.30	0.00	–1.35	0.00
10	V_{SS}	–62.70	–1.60	–1.59	–0.04
11	BYTE#	–62.70	–11.60	–1.59	–0.29
12	A16	–62.70	–21.70	–1.59	–0.55
13	A15	–62.40	–159.50	–1.58	–4.05
14	A14	–55.00	–159.50	–1.40	–4.05
15	A13	–49.60	–159.50	–1.26	–4.05
16	A12	–43.80	–159.50	–1.11	–4.05
17	A11	–38.40	–159.50	–0.98	–4.05
18	A10	–32.50	–159.50	–0.83	–4.05
19	A9	–27.10	–159.20	–0.69	–4.04
20	A8	–21.20	–159.50	–0.54	–4.05
21	WE#	–15.70	–159.50	–0.40	–4.05
22	RESET#	–6.20	–163.30	–0.16	–4.15
23	RY/BY#	11.10	–163.30	0.28	–4.15
24	A17	23.10	–159.50	0.59	–4.05
25	A7	28.90	–159.50	0.73	–4.05
26	A6	34.30	–159.50	0.87	–4.05
27	A5	40.20	–159.50	1.02	–4.05
28	A4	45.60	–159.50	1.16	–4.05
29	A3	51.40	–159.50	1.31	–4.05
30	A2	56.80	–159.50	1.44	–4.05
31	A1	64.20	–159.50	1.63	–4.05
32	A0	64.50	–21.90	1.64	–0.56
33	CE#	64.50	–11.80	1.64	–0.30
34	V_{SS}	64.50	–1.80	1.64	–0.05
35	OE#	55.10	0.90	1.40	0.02
36	DQ0	47.50	0.00	1.21	0.00
37	DQ8	41.60	0.00	1.06	0.00
38	DQ1	35.80	0.00	0.91	0.00
39	DQ9	29.80	0.00	0.76	0.00
40	DQ2	24.00	0.00	0.61	0.00
41	DQ10	18.10	0.00	0.46	0.00
42	DQ3	12.30	0.00	0.31	0.00
43	DQ11	6.30	0.00	0.16	0.00

Note: *The coordinates above are relative to the die center and can be used to operate wire bonding equipment.*

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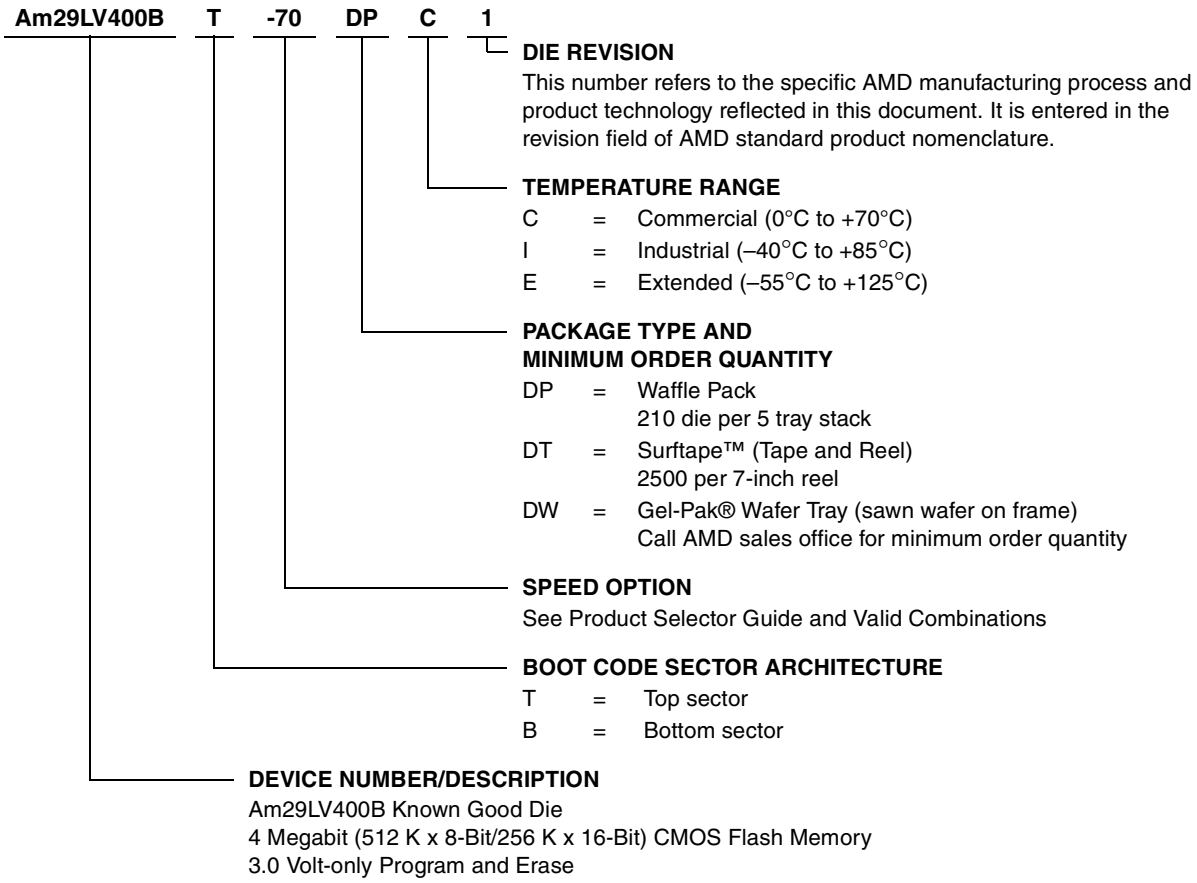
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations		V_{CC} Range
AM29LV400BT-60R AM29LV400BB-60R	DPC 1, DPI 1, DTC 1, DTI 1, DWC 1, DWI 1	3.0–3.6 V
AM29LV400BT-70 AM29LV400BB-70		2.7–3.6 V
AM29LV400BT-80 AM29LV400BB-80	DPC 1, DPI 1, DPE 1 DTC 1, DTI 1, DTE 1 DWC 1, DWI 1, DWE 1	
AM29LV400BT-90 AM29LV400BB-90		
AM29LV400BT-120 AM29LV400BB-120		

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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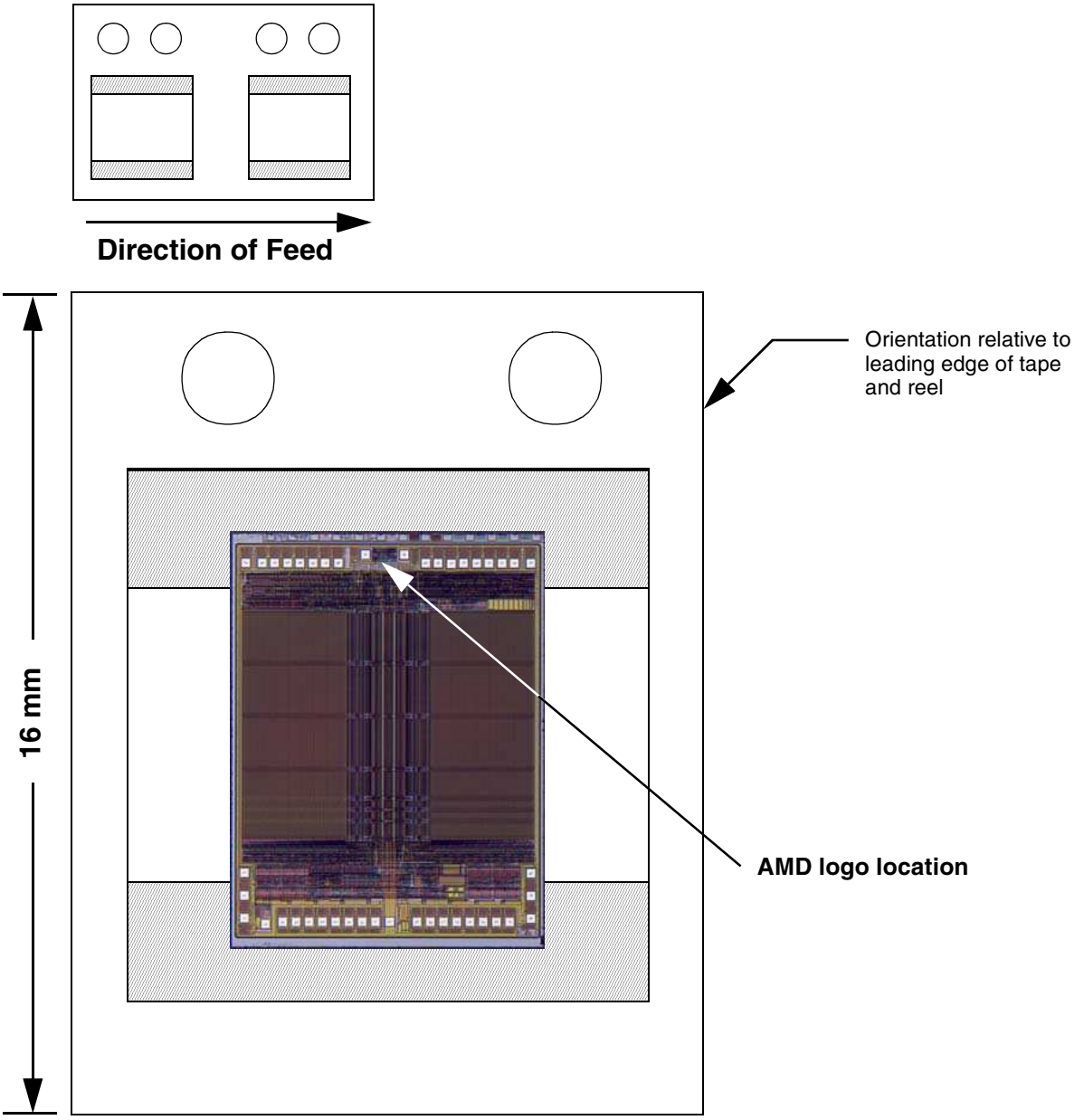
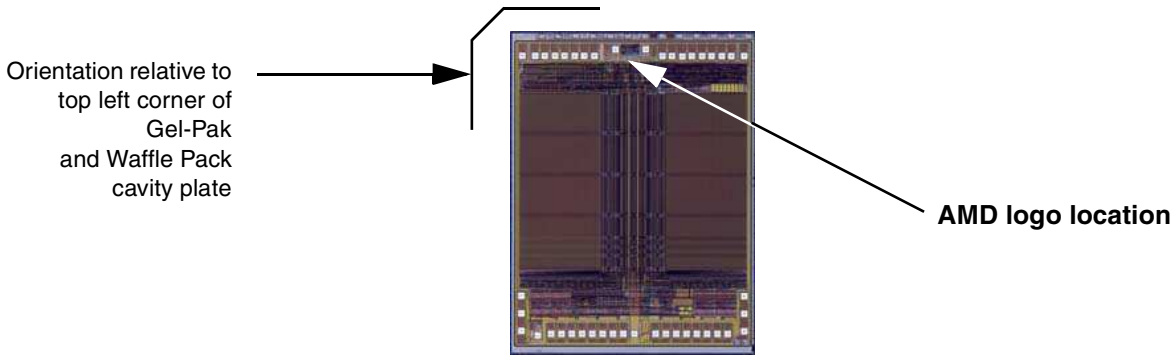
PACKAGING INFORMATION

Surftape Packaging



Gel-Pak and Waffle Pack Packaging



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PRODUCT TEST FLOW

Figure 1 provides an overview of AMD's Known Good Die test flow. For more detailed information, refer to the Am29LV400B product qualification database supplement for KGD. AMD implements quality assurance procedures throughout the product test flow. In addition, an off-line quality monitoring program (QMP) further guarantees AMD quality standards are met on Known Good Die products. These QA procedures also allow AMD to produce KGD products without requiring or implementing burn-in.

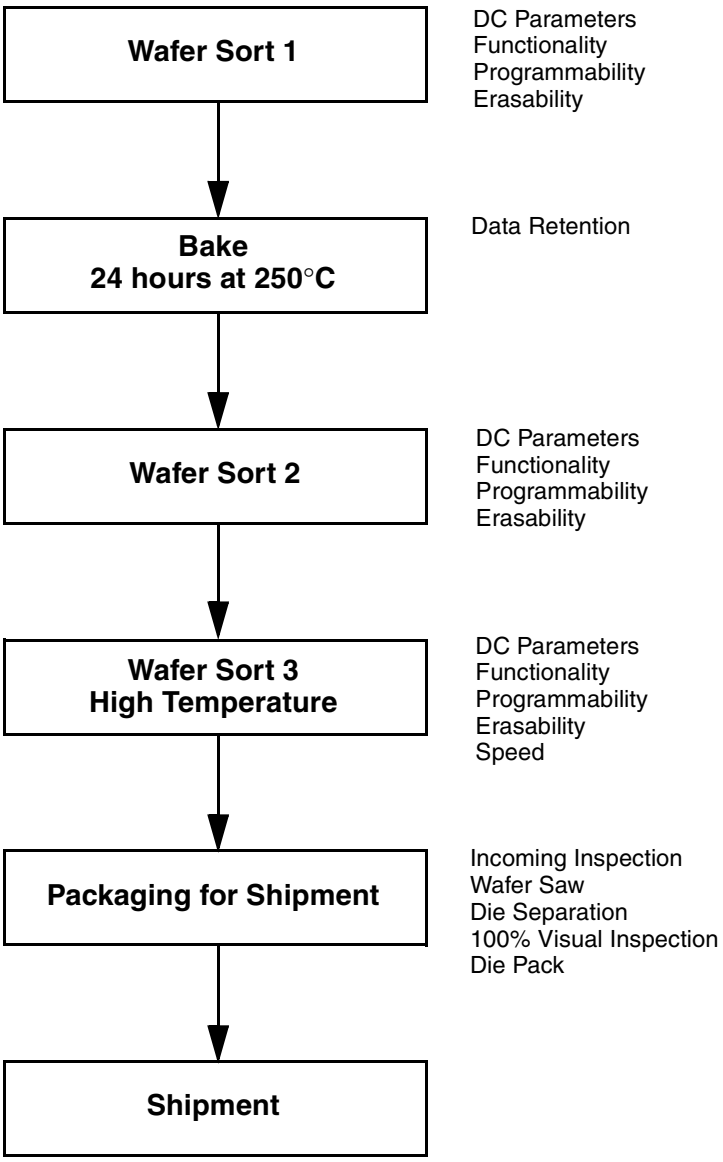

Figure 1. AMD KGD Product Test Flow

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PHYSICAL SPECIFICATIONS

Die dimensions . . . . . 185 mils x 140 mils
. . . . . 4.70 mm x 3.56 mm

Die Thickness. . . . . .500 µm

Bond Pad Size . . . . . 4.69 mils x 4.69 mils
. . . . . 115.9 µm x 115.9 µm

Pad Area Free of Passivation . . . . . .13.99 $mils^2$
. . . . . 9,025 μm^2

Pads Per Die 43

Bond Pad Metalization . . . . . Al/Cu

Die Backside . . . . . No metal, may be grounded (optional)

Passivation. . . . . Nitride/SOG/Nitride

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage) . . . . . .2.7 V to 3.6 V

Operating Temperature

Commercial . . . . . 0°C to +70°C

Industrial . . . . . –40°C to +85°C

Extended . . . . . –55°C to +125°C

MANUFACTURING INFORMATION

Manufacturing . . . . . .FASL

Test . . . . . Penang, Malaysia

Manufacturing ID (Top Boot) 98F03AK

(Bottom Boot). 98F03ABK

Preparation for Shipment . . . . . Penang, Malaysia

Fabrication Process CS39S

Die Revision 1

SPECIAL HANDLING INSTRUCTIONS

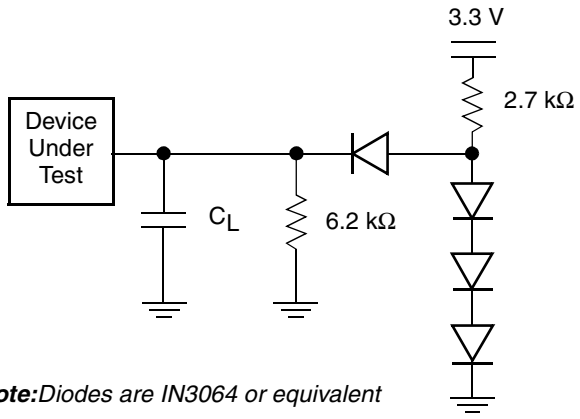
Processing

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

Figure 1. Test Setup

Test Condition	60R, 70, 80	90, 120	Unit
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

Table 1. Test Specifications

Test Condition	60R, 70, 80	90, 120	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V

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TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

All transactions relating to unpackaged die under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

AMD warrants unpackaged die of its manufacture ("Known Good Die" or "Die") against defective materials or workmanship for a period of one (1) year from date of shipment. This warranty does not extend beyond the first purchaser of said Die. Buyer assumes full responsibility to ensure compliance with the appropriate handling, assembly and processing of Known Good Die (including but not limited to proper Die preparation, Die attach, wire bonding and related assembly and test activities), and compliance with all guidelines set forth in AMD's specifications for Known Good Die, and AMD assumes no responsibility for environmental effects on Known Good Die or for any activity of Buyer or a third party that damages the Die due to improper use, abuse, negligence, improper installation, accident, loss, damage in transit, or unauthorized repair or alteration by a person or entity other than AMD ("Warranty Exclusions").

The liability of AMD under this warranty is limited, at AMD's option, solely to repair the Die, to send replacement Die, or to make an appropriate credit adjustment or refund in an amount not to exceed the original purchase price actually paid for the Die returned to AMD, provided that: (a) AMD is promptly notified by Buyer in writing during the applicable warranty period of any defect or nonconformity in the Known Good Die; (b) Buyer obtains authorization from AMD to return the defective Die; (c) the defective Die is returned to AMD by Buyer in accordance with AMD's shipping instructions set forth below; and (d) Buyer shows to AMD's satisfaction that such alleged defect or nonconformity actually exists and was not caused by any of the above-referenced Warranty Exclusions. Buyer shall ship such defective Die to AMD via AMD's carrier, collect. Risk of loss will transfer to AMD when the defective Die is provided to AMD's carrier. If Buyer fails to adhere to these warranty returns guidelines, Buyer shall assume all risk of loss and shall pay for all freight to AMD's specified location. The aforementioned provisions do not extend the original warranty period of any Known Good Die that has either been repaired or replaced by AMD.

WITHOUT LIMITING THE FOREGOING, EXCEPT TO THE EXTENT THAT AMD EXPRESSLY WARRANTS TO BUYER IN A SEPARATE AGREEMENT SIGNED BY AMD, AMD MAKES NO WARRANTY WITH RESPECT TO THE DIE'S PROCESSING OF DATE DATA, AND SHALL HAVE NO LIABILITY FOR DAMAGES OF ANY KIND, UNDER EQUITY, LAW, OR ANY OTHER THEORY, DUE TO THE FAILURE OF SUCH KNOWN GOOD DIE TO PROCESS ANY PARTICULAR DATA CONTAINING DATES, INCLUDING DATES IN AND AFTER THE YEAR 2000, WHETHER OR NOT AMD RECEIVED NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

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Buyer agrees that it will make no warranty representations to its customers which exceed those given by AMD to Buyer unless and until Buyer shall agree to indemnify AMD in writing for any claims which exceed AMD's warranty.

Known Good Die are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of the Die can reasonably be expected to result in a personal injury. Buyer's use of Known Good Die for use in life support applications is at Buyer's own risk and Buyer agrees to fully indemnify AMD for any damages resulting in such use or sale.

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REVISION SUMMARY

Revision A (December 10, 1999)

Initial release.

Revision B (December 10, 2001)

Added 60R, 70 speed options. Added test conditions section.

Revision B+1 (March 12, 2002)

Pad Description

Added table of pad locations relative to die center. Corrected X,Y orientation for pad locations relative to V_{CC}.

Manufacturing Information

Changed test facility to Penang, Malaysia (ACN2016).

Revision C (October 15, 2003)

Pad Description - Pad Locations Relative to Die Center

Modified Pad Center (mils), Y, #12 to 58.80, and Pad Center (millimeters), Y, #12 to 1.49.

Am29LV400B Features

Removed last sentence of 2nd paragraph (The device can also be programmed in standard EPROM programmers). Removed mention of “pin”.

Trademarks

Updated to 2003.

Trademarks

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Miami (Lakes) . . . . . (305)820-1113
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