AK4632

16-Bit ΔΣ Mono CODEC with ALC & MIC/SPK/Video-AMP

GENERAL DESCRIPTION

The AK4632 is a 16-bit mono CODEC with Microphone-Amplifier, Speaker-Amplifier and Video-Amplifier. Input circuits include a Microphone-Amplifier and an ALC (Automatic Level Control) circuit. Output circuits include a Speaker-Amplifier and Mono Line Output. Video circuits include a LPF and Video-Amplifier. The AK4632 suits a moving picture of Digital Still Camera and etc. This speaker-Amplifier supports a Piezo Speaker. The AK4632 is housed in a space-saving 32-pin QFN package.

FEATURE

1. 16-Bit Delta-Sigma Mono CODEC

2. Recording Function
- **1ch Mono Input**
- **1st MIC Amplifier: 0dB, 20dB, 26dB or 32dB**
- **2nd Amplifier with ALC: -8dB ~ +27.5dB, 0.5dB Step**
- **ADC Performance: S/(N+D): 80dB, DR, S/N: 85dB**

3. Playback Function
- **Digital Volume: +12dB ~ -115dB, 0.5dB Step, Mute**
- **Mono Line Output Performance: S/(N+D): 85dB, S/N: 93dB**
- **Mono Speaker-Amp**
  - **Speaker-Amp Performance: S/(N+D): 60dB, S/N: 90dB (150mW@ 8Ω)**
  - **BTL Output**
  - **ALC (Automatic Level Control) Circuit**
  - **Output Power: 400mW @ 8Ω, SVDD=3.3V**
    3.0Vrms@SVDD=5V
- **Beep Input**

4. Power Management

5. Video Function
- **A Composite Video Input**
- **Gain Control (-1.0dB ~ +10.5dB, 0.5dB Step)**
- **Low Pass Filter**
- **A Video-Amp for Composite Video Signal(+6dB)**
- **DC Direct Output or Sag Compensation Output**

6. Flexible PLL Mode:
- **Frequencies:**
  11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)
  1fs (FCK pin)
  16fs, 32fs or 64fs (BICK pin)

7. EXT Mode:
- **Frequencies: 256fs, 512fs or 1024fs (MCKI pin)**

8. Sampling Rate:
- **PLL Slave Mode (FCK pin) : 7.35kHz ~ 26kHz**
- **PLL Slave Mode (BICK pin) : 7.35kHz ~ 48kHz**
- **PLL Slave Mode (MCKI pin):**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **PLL Master Mode:**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz

- **EXT Slave Mode:**
  7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs), 7.35kHz ~ 13kHz (1024fs)

9. **Output Master Clock Frequency: 256fs**
10. **Serial μP Interface: 3-wire**
11. **Master / Slave Mode**
12. **Audio Interface Format: MSB First, 2's compliment**
    - **ADC: DSP Mode, 16bit MSB justified, I^2S**
    - **DAC: DSP Mode, 16bit MSB justified, 16bit LSB justified, I^2S**
13. **Ta = -10 ~ 70°C**
14. **Power Supply**
    - **CODEC: 2.6 ~ 3.6V (typ. 3.3V)**
    - **Speaker-Amp: 2.6 ~ 5.25V (typ. 3.3V/5.0V)**
    - **Video-Amp: 2.8 ~ 5.25V (typ. 3.3V/5.0V)**
15. **Power Supply Current: 23.5 mA (All Power ON)**
16. **Package: 32pin QFN**
17. **Register Compatible with AK4631**

■ Block Diagram

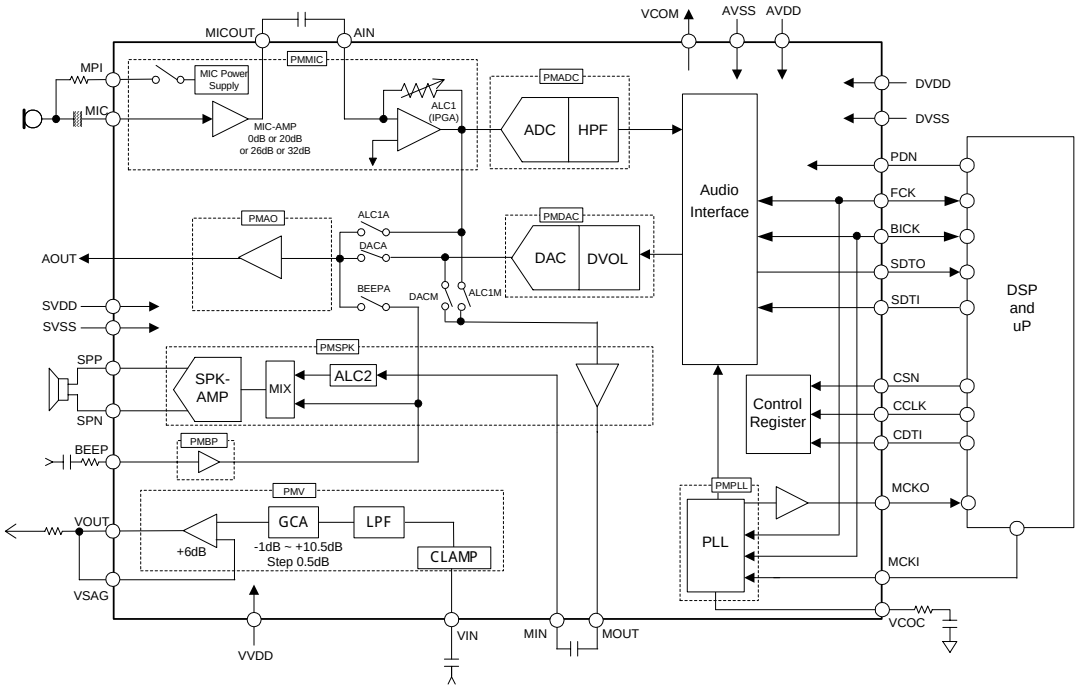
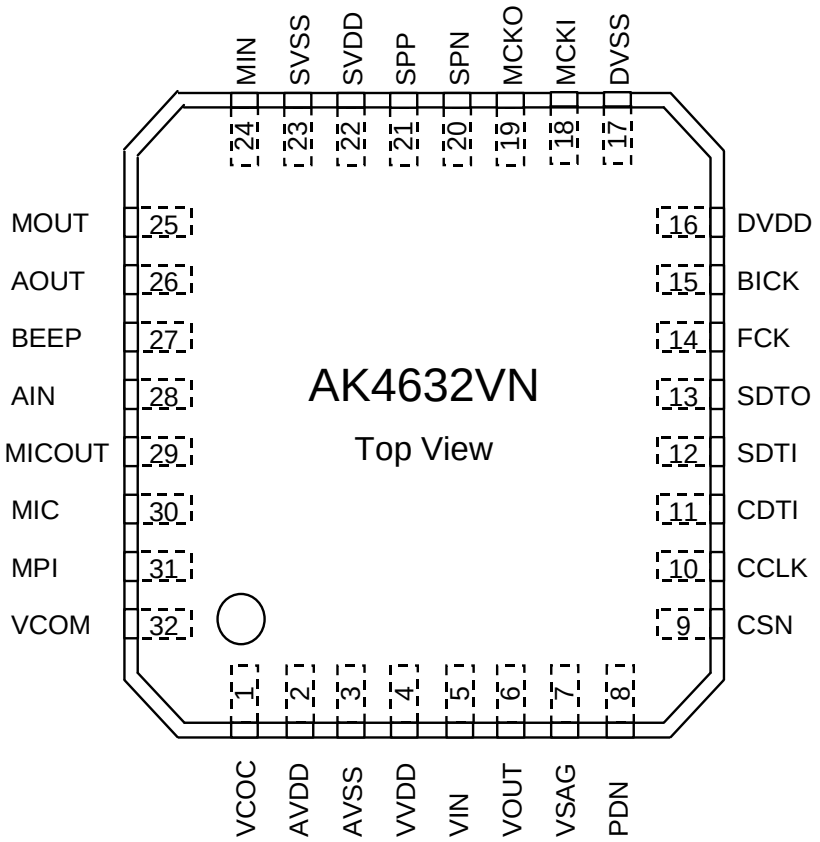


Figure 1. AK4632 Block Diagram

■ Ordering Guide

AK4632VN	–10 ~ +70°C	32pin QFN (0.5mm pitch)
AKD4632	Evaluation board for AK4632	

■ Pin Layout



■ Compare with AK4632

Function	AK4631	AK4632
Video Function	No	Yes
Package	28pin QFN (5.2mm x 5.2mm)	32pin QFN (5.0mm x 5.0mm)

The audio function of the AK4632 is compatible with that of the AK4631. Since the register map of audio function is the same as the AK4631's, the software of the audio function can run on the ak4632 without any change.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to AVSS with one resistor and capacitor in series.
2	AVDD	-	Analog Power Supply Pin
3	AVSS	-	Analog Ground Pin
4	VVDD	-	Video Block Power Supply Pin.
5	VIN	I	Composite Video Signal Input Pin
6	VOUT	O	Composite Video Signal Driver Pin
7	VSAG	I	Composite Video Signal Output Feedback Input Pin
8	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initialize the control register.
9	CSN	I	Chip Select Pin
10	CCLK	I	Control Data Clock Pin
11	CDTI	I	Control Data Input Pin
12	SDTI	I	Audio Serial Data Input Pin
13	SDTO	O	Audio Serial Data Output Pin
14	FCK	I/O	Frame Clock Pin
15	BICK	I/O	Audio Serial Data Clock Pin
16	DVDD	-	Digital Power Supply Pin
17	DVSS	-	Digital Ground Pin
18	MCKI	I	External Master Clock Input Pin (Internal Pull Down 25kΩ@PDN pin ="L")
19	MCKO	O	Master Clock Output Pin
20	SPN	O	Speaker Amp Negative Output Pin
21	SPP	O	Speaker Amp Positive Output Pin
22	SVDD	-	Speaker Amp Power Supply Pin
23	SVSS	-	Speaker Amp Ground Pin
24	MIN	I	ALC2 Input Pin
25	MOUT	O	Mono Analog Output Pin
26	AOUT	O	Mono Line Output Pin
27	BEEP	I	Beep Signal Input Pin
28	AIN	I	IPGA (ALC1) Input Pin
29	MICOUT	O	Microphone Analog Output Pin
30	MIC	I	Microphone Input Pin (Mono Input)
31	MPI	O	MIC Power Supply Pin for Microphone
32	VCOM	O	Common Voltage Output Pin. Common Voltage = 0.45 x AVDD Bias voltage of ADC inputs and DAC outputs.

Note : All input pins except analog input pins (MIC, AIN, MIN, BEEP and VIN pins) should not be left floating.
Note : The exposed pad on the bottom surface of the package must be open.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog Input	MIC, AIN, BEEP, MIN, VSAG	These pins should be open and each path should be switched off.
Analog Output	MICOUT, MPI, AOUT, MOUT, SPP, SPN, VOUT	These pins should be open.
Digital Input	MCKI, SDTI, FCK(when M/S bit = "0"), BICK(when M/S bit = "0")	These pins should be connected to DVSS.
Digital Output	MCKO, SDTO, FCK(when M/S bit = "1"), BICK(when M/S bit = "1")	These pins should be open.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS, SVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	6.0	V
	Speaker-Amp	SVDD	–0.3	6.0	V
	Video	VVDD	–0.3	6.0	V
	|AVSS – DVSS| (Note 2)	ΔGND1	-	0.3	V
	|AVSS – SVSS| (Note 2)	ΔGND2	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage(Audio) (Note 3)		VINA	–0.3	AVDD+0.3	V
Analog Input Voltage(Video) (Note 4)		VINV	–0.3	VVDD+0.3	V
Digital Input Voltage		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–10	70	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 5)		Pd	-	700	mW

Note 1. All voltages with respect to ground.
Note 2. AVSS, DVSS and SVSS must be connected to the same analog ground plane.
Note 3. MIC, AIN, BEEP, MIN pins
Note 4. VIN pin
Note 5. In case that PCB wiring density is 100%. This power is the AK4632 internal dissipation that does not include power of externally connected speaker.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS, SVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 6)	Analog	AVDD	2.6	3.3	3.6	V
	Digital	DVDD	2.6	3.3	3.6	V
	Speaker-Amp (Note 7)	SVDD	2.6	3.3 / 5.0	5.25	V
	Video (Note 8)	VVDD	2.8 or AVDD	3.3 / 5.0	5.25	V
	Difference	AVDD-DVDD	-0.3	0	0.3	V

Note 1. All voltages with respect to ground

Note 6. The power up sequence between AVDD, DVDD and SVDD is not critical.
When the power supplies are partially powered OFF, the AK4632 must be reset by bringing PDN pin "L" after these power supplies are powered ON again.

Note 7. SVDD = 2.6 ~ 3.6V when 8Ω dynamic speaker is connected to the AK4632. If SVDD is more than 3.6V when 8Ω dynamic speaker is connected to the AK4632, the output of Speaker-Amp should be restricted in consideration of maximum power dissipation as the following.

SPoMax : Maximum Output Power of SPK-Amp[mW]
SPKMPD : Maximum Power Dissipation of SPK-Amp[mW]
Rmin : Minimum Impedance of speaker[Ω]
Vmax : Maximum permission output voltage of SPK-Amp[Vrms]

SPKMPD = 700 – AVDD(max) x 17.5 – VVDD(max) x 12 – SVDD(max) x 27
A = 2 x sqrt(2) x SVDD(max) / π
B = A x A – 4 x Rmin x SPKMPD / 1000
Vmax= (A – sqrt(B)) / 2
SPoMax = 1000 x Vmax x Vmax / Rmin

Maximum Output Power of SPK-Amp at B < 0 : No limitation
Maximum Output Power of SPK-Amp at B ≥ 0: This power should be less than or equal to SPoMax[mW].
Regardless of the condition of B, the distortion of output signal increases, when SPK-Amp output power exceeds 240mW.

Note 8. Minimum value is higher value between 2.8V and AVDD[V].

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHRACTERISTICS

(Ta=25°C; AVDD, DVDD, SVDD, VVDD=3.3V; AVSS=DVSS=SVSS=0V; fs=8kHz, BICK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 3.4kHz; EXT Slave Mode; unless otherwise specified)

Parameter		min	typ	max	Units
MIC Amplifier					
Input Resistance		20	30	40	kΩ
Gain	(MGAIN1-0 bits = "00")	-	0	-	dB
	(MGAIN1-0 bits = "01")	-	20	-	dB
	(MGAIN1-0 bits = "10")	-	26	-	dB
	(MGAIN1-0 bits = "11")	-	32	-	dB
MIC Power Supply: MPI pin					
Output Voltage	(Note 9)	2.22	2.47	2.72	V
Load Resistance		2	-	-	kΩ
Load Capacitance		-	-	30	pF
Input PGA Characteristics:					
Input Resistance	(Note 10)	5	10	15	kΩ
Step Size		0.05	0.5	0.9	dB
Gain Control Range		–8	-	+27.5	dB
ADC Analog Input Characteristics: MIC → IPGA → ADC, MIC Gain=20dB, IPGA=0dB, ALC1=OFF					
Resolution		-	-	16	Bits
Input Voltage	(MIC Gain=20dB, Note 11)	0.168	0.198	0.228	Vpp
S/(N+D)	(–1dBFS) (Note 12)	68	80	-	dB
D-Range	(–60dBFS)	75	85	-	dB
S/N		75	85	-	dB
DAC Characteristics:					
Resolution		-	-	16	Bits
Mono Line Output Characteristics: AOUT pin, DAC → AOUT, R_L=10kΩ					
Output Voltage	(Note 13)	1.78	1.98	2.18	Vpp
S/(N+D)	(0dBFS) (Note 12)	73	85	-	dB
D-Range	(-60dBFS)	83	93	-	dB
S/N		83	93	-	dB
Load Resistance		10	-	-	kΩ
Load Capacitance		-	-	30	pF

Note 9. Output voltage is proportional to AVDD voltage. Vout = 0.75 x AVDD (typ)
Note 10. When IPGA Gain is changed, this typical value changes between 8kΩ and 11kΩ.
Note 11. Input voltage is proportional to AVDD voltage. Vin = 0.06 x AVDD (typ)
Note 12. When a PLL reference clock is FCK pin in PLL Slave Mode, S/(N+D) is 77dB (typ).
Note 13. Output voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ)

Parameter		min	typ	max	Units
Speaker-Amp Characteristics: SPP/SPN pins, MIN → SPP/SPN, ALC2=OFF, R_L=8Ω, BTL, SVDD=3.3V					
Output Voltage (Note 14)	SPKG1-0 bits = "00" (-0.5dBFS)	2.47	3.09	3.71	Vpp
	SPKG1-0 bits = "01" (-0.5dBFS)	3.10	4.00	4.80	Vpp
S/(N+D)	at 150mW Output	20	60	-	dB
	at 240mW Output	-	50	-	dB
	at 400mW Output	-	20	-	dB
S/N (Note 16)		80	90	-	dB
Load Resistance		8	-	-	Ω
Load Capacitance		-	-	30	pF
Speaker-Amp Characteristics: MIN → SPP/SPN pins, ALC2=OFF, C_L=3μF, R_{serial}=10Ω x 2, BTL, SVDD=5.0V					
Output Voltage (Note 14)	SPKG1-0 bits = "10"	-	6.72	-	Vpp
	SPKG1-0 bits = "11"	6.80	8.50	10.20	Vpp
S/(N+D) (Note 14) (Note 15)	SPKG1-0 bits = "10"	-	60	-	dB
	SPKG1-0 bits = "11"	20	50	-	dB
S/N (Note 15) (Note 16)		80	80	90	dB
Load Impedance (Note 17)		50	-	-	Ω
Load Capacitance		-	-	3	μF
BEEP Input: BEEP pin, External Input Resistance= 20kΩ					
Maximum Input Voltage (Note 18)		-	1.98	-	Vpp
Output Voltage (Input Voltage=0.6Vpp)					
	BEEP → SPP/SPN (SPKG1-0 bits = "00")	0.74	1.48	2.22	Vpp
	BEEP → AOUT	0.3	0.6	0.9	Vpp
Mono Input: MIN pin					
Maximum Input Voltage (Note 19)		-	2.18	-	Vpp
Input Resistance (Note 20)		12	24	36	kΩ
Mono Output: MOUT pin, DAC→ MOUT					
Output Voltage (Note 21)		1.78	1.98	2.18	Vpp
Load Resistance		10	-	-	kΩ
Load Capacitance		-	-	30	pF

Note 14. The full scale of Input signal of MIN pin is 1.98Vpp.
Note 15. In case of measuring between SPP pin and SPN pin directly.
Note 16. There are no relations with the setup of SPKG1-0 bits, and it is the same value.
Note 17. Load impedance is total impedance of series resistance and piezo speaker impedance at 1kHz in Figure 35. Load capacitance is capacitance of piezo speaker. When piezo speaker is used, 10Ω or more series resistors should be connected at both SPP and SPN pins, respectively.
Note 18. The maximum input voltage of the BEEP is proportional to AVDD voltage and external input resistance(Rin). Vout = 0.6 x AVDD x Rin/20kΩ(max).
Note 19. Maximum Input Voltage is proportional to AVDD voltage. Vin = 0.66 x AVDD (max)
Note 20. When ALC2 Gain is changed, this typical value changes between 22kΩ and 26kΩ.
Note 21. Output Voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ)

Parameter			min	typ	max	Units
Y Input Characteristics:						
Maximum Input Voltage (Note 22)			-	1.2	-	Vpp
Pull Down Current			-	2.0	-	μA
V Output Characteristics:						
Output Gain	VIN=100kHz (GCA=0dB)		5.0	6.0	7.0	dB
Maximum Output Voltage	at DC output		2.4	2.52	-	Vpp
	at Sag Compensation Output 100μF+2.2 uF, VVDD ≥ 3.135 V		-	2.4	-	Vpp
	at Sag Compensation Output 47μF+1.0uF, VVDD ≥ 3.135 V		-	2.4	-	Vpp
Clamp Voltage	at DC output		-	0.15	-	V
S/N	BW=100kH ~ 6MHz		-	66	-	dB
Secondary Distortion	VIN=3.58MHz, 1.0Vpp(Sin Wave) (Note 23)		-	-45	-	dB
Load Resistance			140	150	-	Ω
Load Capacitance	C1(See Figure 2)		-	-	15	pF
	C2(See Figure 2) (Note 24)		-	-	400	pF
LPF						
Frequency Response Input=1.26Vpp, Sin Wave (0dB at 100kHz)	Response at 6.75MHz		-3.0	-0.5	-	dB
	Response at 27MHz		-	-30	-20	dB
Group Delay	|GD3MHz –GD6MHz|		-	10	100	nsec
GCA Characteristics:						
Step Size	GCA = -1.0dB ~ +10.5dB		0.1	0.5	0.9	dB
Power Supplies						
Power Up (PDN = "H")						
All Circuit Power-up: (Note 25)						
AVDD+DVDD	fs=8kHz		-	9	-	mA
	fs=48kHz		-	11.5	17.5	mA
SVDD: Speaker-Amp Normal Operation (SPPS bit = "1", No Output)						
	SVDD=3.3V		-	7	-	mA
	SVDD=5.0V		-	9	27	mA
VVDD (Note 26)						
	VVDD=3.3V		-	7.5	-	mA
	VVDD=5.0V		-	8	12	mA
Power Down (PDN = "L") (Note 27)						
AVDD+DVDD+SVDD+VVDD			-	10	100	μA

Note 22. Input Voltage doesn't depend on VVDD.
Note 23. In the case of using Sag Compensation Circuit with 47μF+ 1.0uF and SAGC1-0 bits = "10"
Note 24. R1 and C2 compose of Low Pass Filter(LPF) in Figure 2. The cut off frequency of LPF is 10.6MHz at C2 = 400pF.

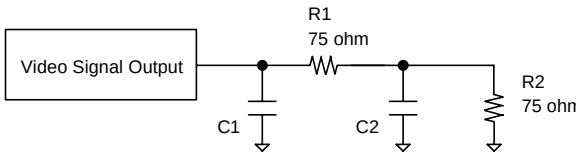


Figure 2. Load Capacitance C1 and C2

Note 25. PLL Master Mode (MCKI=12.288MHz) and PMV=PMMIC = PMADC = PMDAC = PMSPK = PMVCM = PMPLL = MCKO = PMAO = PMBP = MPWR = M/S ="1". And output current from MPI pin is 0mA. When the AK4632 is EXT mode (PMPLL = MCKO = M/S = "0"), "AVDD+DVDD" is typically 7mA@fs=8kHz, 9.5mA@fs=48kHz).

Note 26. This is the case of SAGC bits = "00" and no load resistance and capacitance. When SAGC bits = "10" and Black signal is output, this current is typ.8mA. In the case of DC Output, this current increases by DC voltage / 150 Ω. DC Output Voltage is 0V at PMV bit = "0", and then DC current doesn't flow. When any signal isn't input at using Sag Compensation Circuit, PMV bit should be set to "0".

Note 27. MCKI pin is fixed to DVSS and all digital inputs pins except MCKI pin are fixed to DVSS or DVSS.

FILTER CHRACTERISTICS

(Ta = 25°C; AVDD, DVDD = 2.6 ~ 3.6V; SVDD =2.6 ~ 5.25V; VVDD =2.8 ~ 5.25V; fs=8kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 28)	±0.16dB	PB	0	-	3.0	kHz
	−0.66dB		-	3.5	-	kHz
	−1.1dB		-	3.6	-	kHz
	−6.9dB		-	4.0	-	kHz
Stopband (Note 28)		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 29)		GD	-	17.1	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response (Note 28)	−3.0dB	FR	-	0.62	-	Hz
	−0.5dB		-	1.81	-	Hz
	−0.1dB		-	3.99	-	Hz
DAC Digital Filter:						
Passband (Note 28)	±0.1dB	PB	0	-	3.6	kHz
	−0.7dB		-	3.6	-	kHz
	−6.0dB		-	4.0	-	
Stopband (Note 28)		SB	4.6	-	-	kHz
Passband Ripple		PR	-	-	±0.01	dB
Stopband Attenuation		SA	59	-	-	dB
Group Delay (Note 29)		GD	-	16.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 3.4kHz		FR	-	±1.0	-	dB

Note 28. The passband and stopband frequencies are proportional to fs (system sampling rate).
For example, ADC is PB=0.45*fs (@-1.1dB). A reference of frequency response is 1kHz.

Note 29. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of a channel from the input register to the output register of the ADC. This time includes the group delay of the HPF. For the DAC, this time is from setting the 16-bit data of a channel from the input register to the output of analog signal.

DC CHRACTERISTICS

(Ta = 25°C; AVDD, DVDD = 2.6 ~ 3.6V; SVDD =2.6 ~ 5.25V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	70%DVDD	-	-	V
Low-Level Input Voltage		VIL	-	-	30%DVDD	V
High-Level Output Voltage	(Iout=−80μA)	VOH	DVDD−0.4	-	-	V
Low-Level Output Voltage	(Iout= 80μA)	VOL	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	μA

SWITING CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 2.6 ~ 3.6V; SVDD =2.6 ~ 5.25V ; VVDD =2.8 ~ 5.25V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
PLL Master Mode (PLL Reference Clock = MCKI pin) (Figure 3)					
MCKI Input: Frequency	fCLK	11.2896	-	27.0	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
MCKO Output:					
Frequency	fMCK	-	256 x fFCK	-	kHz
Duty Cycle except fs=29.4kHz, 32kHz	dMCK	40	50	60	%
fs=29.4kHz, 32kHz (Note 30)	dMCK	-	33	-	%
FCK Output: Frequency	fFCK	8	-	48	kHz
Duty Cycle	dFCK	-	50	-	%
BICK: Period (BCKO1-0 = "00")	tBCK	-	1/16fFCK	-	ns
(BCKO1-0 = "01")	tBCK	-	1/32fFCK	-	ns
(BCKO1-0 = "10")	tBCK	-	1/64fFCK	-	ns
Duty Cycle	dBCK	-	50	-	%
Audio Interface Timing					
DSP Mode: (Figure 4, Figure 5)					
FCK "↑" to BICK "↑" (Note 31)	tDBF	0.5 x tBCK -40	0.5 x tBCK	0.5 x tBCK + 40	ns
FCK "↑" to BICK "↓" (Note 32)	tDBF	0.5 x tBCK -40	0.5 x tBCK	0.5 x tBCK +40	ns
BICK "↑" to SDTO (BCKP = "0")	tBSD	-70	-	70	ns
BICK "↓" to SDTO (BCKP = "1")	tBSD	-70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Except DSP Mode: (Figure 6)					
BICK "↓" to FCK Edge	tBFCK	-40	-	40	ns
FCK to SDTO (MSB) (Except I^2S mode)	tFSD	-70	-	70	ns
BICK "↓" to SDTO	tBSD	-70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Parameter	Symbol	min	typ	max	Units
PLL Slave Mode (PLL Reference Clock: FCK pin) (Figure 7, Figure 8)					
FCK: Frequency	fFCK	7.35	8	26	kHz
DSP Mode: Pulse Width High	tFCKH	tBCK-60	-	1/fFCK-tBFCK	ns
Except DSP Mode: Duty Cycle	duty	45	-	55	%
BICK: Period	tBCK	1/64fFCK	-	1/16fFCK	ns
Pulse Width Low	tBCKL	240	-	-	ns
Pulse Width High	tBCKH	240	-	-	ns
PLL Slave Mode (PLL Reference Clock: BICK pin) (Figure 7, Figure 8)					
FCK: Frequency	fFCK	7.35	8	48	kHz
DSP Mode: Pulse width High	tFCKH	tBCK-60	-	1/fFCK-tBFCK	ns
Except DSP Mode: Duty Cycle	duty	45	-	55	%
BICK: Period (PLL3-0 = "0001")	tBCK	-	1/16fFCK	-	ns
(PLL3-0 = "0010")	tBCK	-	1/32fFCK	-	ns
(PLL3-0 = "0011")	tBCK	-	1/64fFCK	-	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns
PLL Slave Mode (PLL Reference Clock: MCKI pin) (Figure 9)					
MCKI Input: Frequency	fCLK	11.2896	-	27.0	MHz
Pulse Width Low	fCLKL	0.4/fCLK	-	-	ns
Pulse Width High	fCLKH	0.4/fCLK	-	-	ns
MCKO Output:					
Frequency	fMCK	-	256 x fFCK	-	kHz
Duty Cycle except fs=29.4kHz, 32kHz	dMCK	40	50	60	%
fs=29.4kHz, 32kHz (Note 30)	dMCK	-	33	-	%
FCK: Frequency	fFCK	8	-	48	kHz
DSP Mode: Pulse width High	tFCKH	tBCK-60	-	1/fFCK-tBFCK	ns
Except DSP Mode: Duty Cycle	duty	45	-	55	%
BICK: Period	tBCK	1/64fFCK	-	1/16fFCK	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns
Audio Interface Timing					
DSP Mode: (Figure 10,Figure 11)					
FCK "↑" to BICK "↑" (Note 31)	tFCKB	0.4 x tBCK	-	-	ns
FCK "↑" to BICK "↓" (Note 32)	tFCKB	0.4 x tBCK	-	-	ns
BICK "↑" to FCK "↑" (Note 31)	tBFCK	0.4 x tBCK	-	-	ns
BICK "↓" to FCK "↑" (Note 32)	tBFCK	0.4 x tBCK	-	-	ns
BICK "↑" to SDTO (BCKP = "0")	tBSD	-	-	80	ns
BICK "↓" to SDTO (BCKP = "1")	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Except DSP Mode: (Figure 13)					
FCK Edge to BICK "↑" (Note 33)	tFCKB	50	-	-	ns
BICK "↑" to FCK Edge (Note 33)	tBFCK	50	-	-	ns
FCK to SDTO (MSB) (Except I^2S mode)	tFSD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Parameter	Symbol	min	typ	Max	Units
EXT Slave Mode (Figure 12)					
MCKI Frequency: 256fs	fCLK	1.8816	2.048	12.288	MHz
512fs	fCLK	3.7632	4.096	13.312	MHz
1024fs	fCLK	7.5264	8.192	13.312	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
FCK Frequency (MCKI = 256fs)	fFCK	7.35	8	48	kHz
(MCKI = 512fs)	fFCK	7.35	8	26	kHz
(MCKI = 1024fs)	fFCK	7.35	8	13	kHz
Duty Cycle	duty	45	-	55	%
BICK Period	tBCK	312.5	-	-	ns
BICK Pulse Width Low	tBCKL	130	-	-	ns
Pulse Width High	tBCKH	130	-	-	ns
Audio Interface Timing (Figure 13)					
FCK Edge to BICK "↑" (Note 33)	tFCKB	50	-	-	ns
BICK "↑" to FCK Edge (Note 33)	tBFCK	50	-	-	ns
FCK to SDTO (MSB) (Except I^2S mode)	tFSD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Note 30. Duty Cycle = (the width of "L") / (the period of clock) × 100
Note 31. MSBS, BCKP bits = "00" or "11"
Note 32. MSBS, BCKP bits = "01" or "10"
Note 33. BICK rising edge must not occur at the same time as FCK edge.

Parameter	Symbol	min	typ	max	Units
Control Interface Timing:					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	150	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
Reset Timing					
PDN Pulse Width (Note 34)	tPD	150	-	-	ns
PMADC "↑" to SDTO valid (Note 35)	tPDV	-	1059	-	1/fs

Note 34. The AK4632 can be reset by the PDN pin = "L"
Note 35. This is the count of FCK "↑" from the PMADC = "1".

■ Timing Diagram

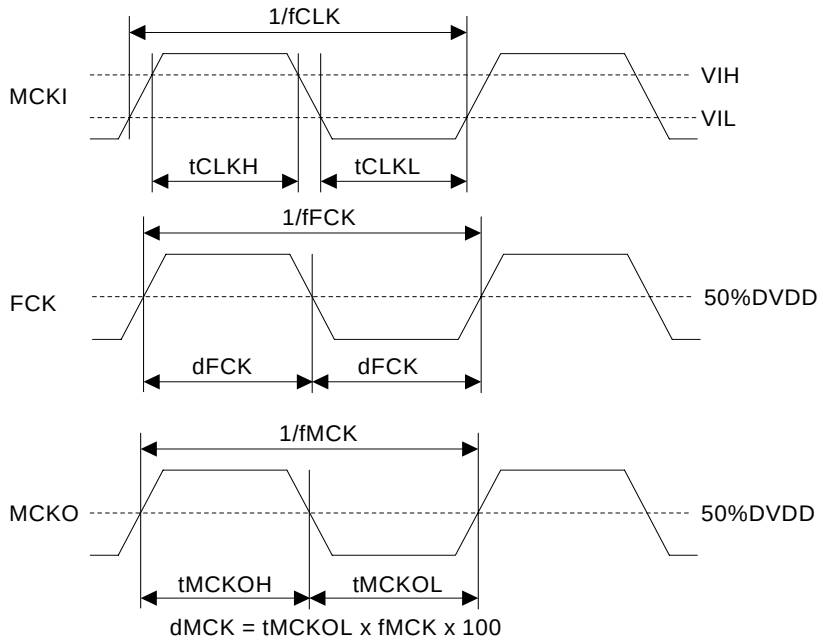


Figure 3. Clock Timing (PLL Master mode)

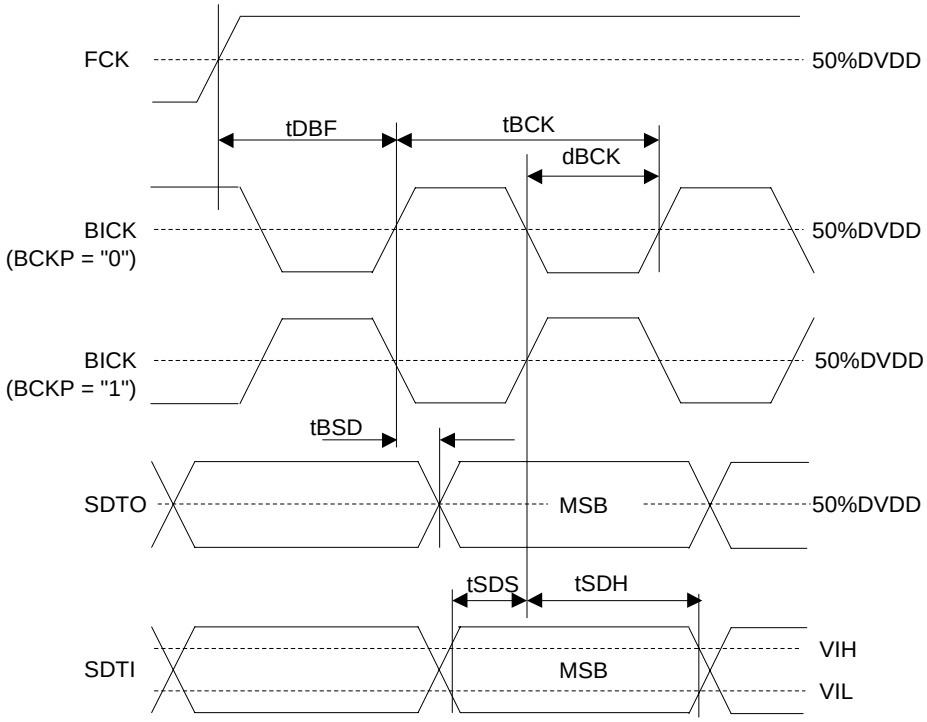


Figure 4. Audio Interface Timing (PLL Master mode & DSP mode: MSBS = “0”)

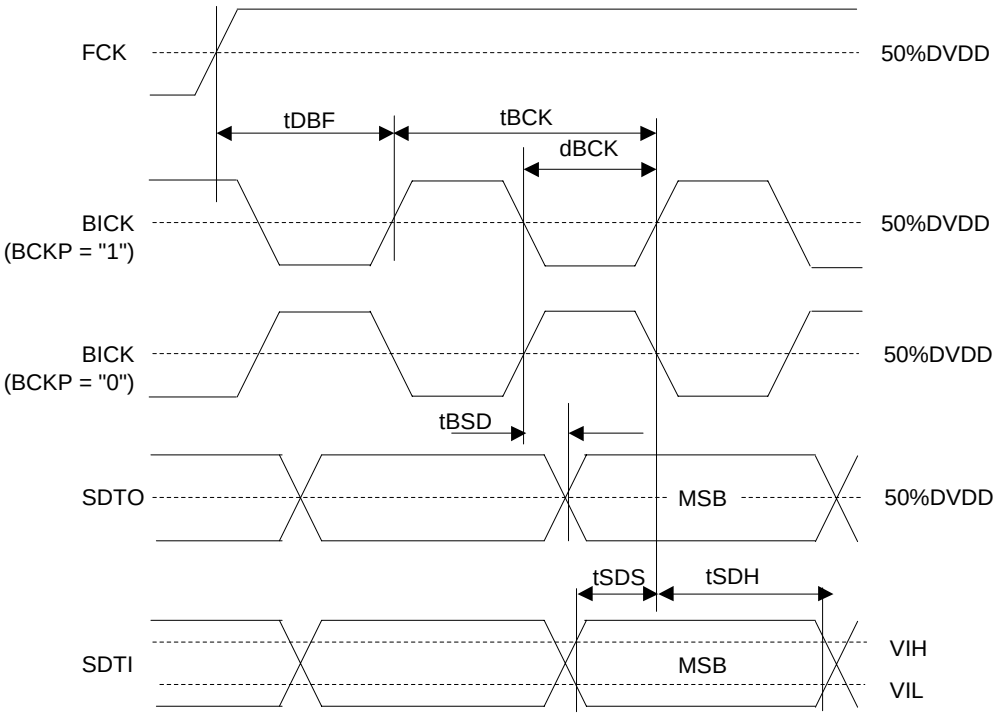


Figure 5. Audio Interface Timing (PLL Master mode & DSP mode: MSBS = "1")

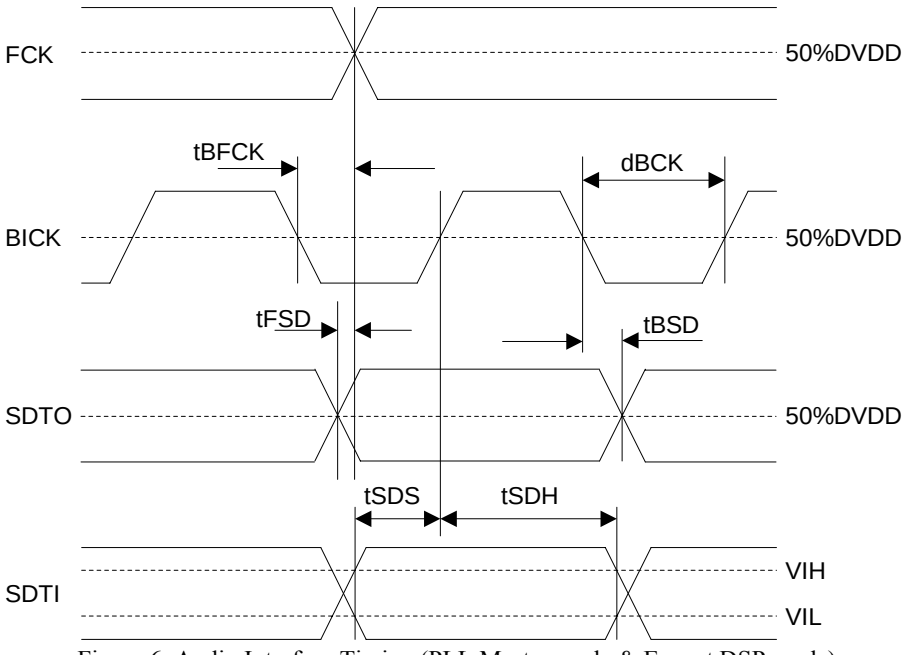


Figure 6. Audio Interface Timing (PLL Master mode & Except DSP mode)

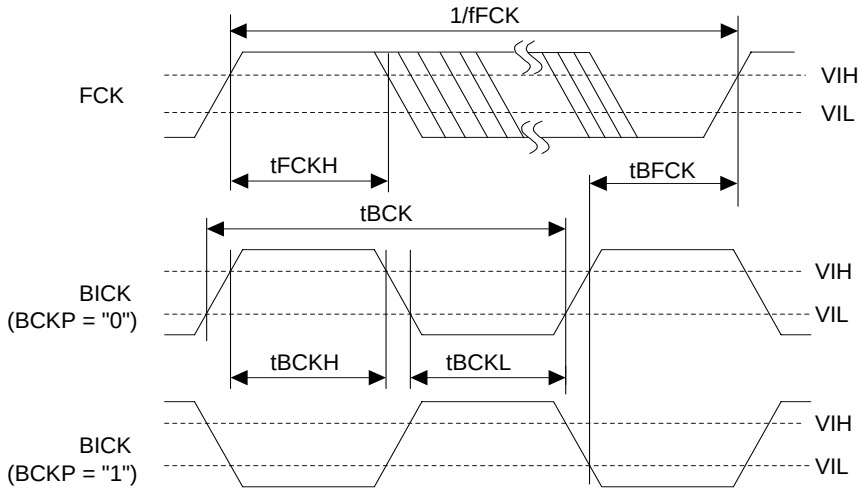


Figure 7. Clock Timing (PLL Slave mode**;** PLL Reference clock = FCK or BICK pin & DSP mode; MSBS = 0)

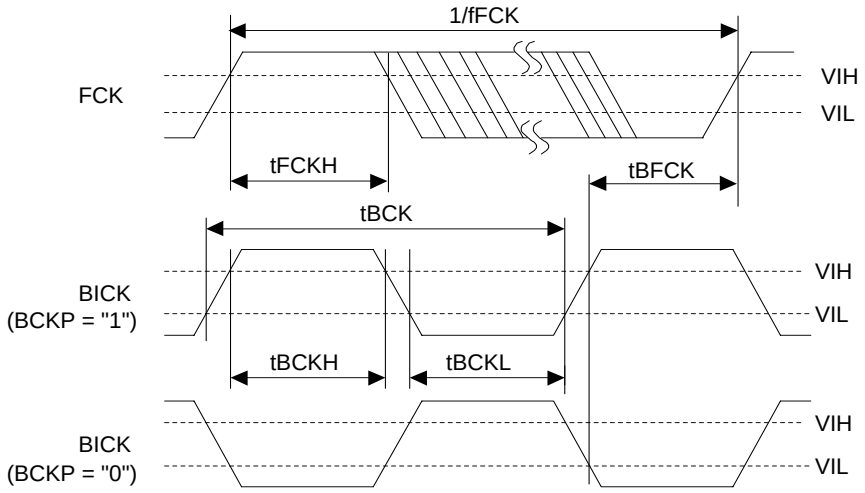


Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = FCK or BICK pin & DSP mode; MSBS = 1)

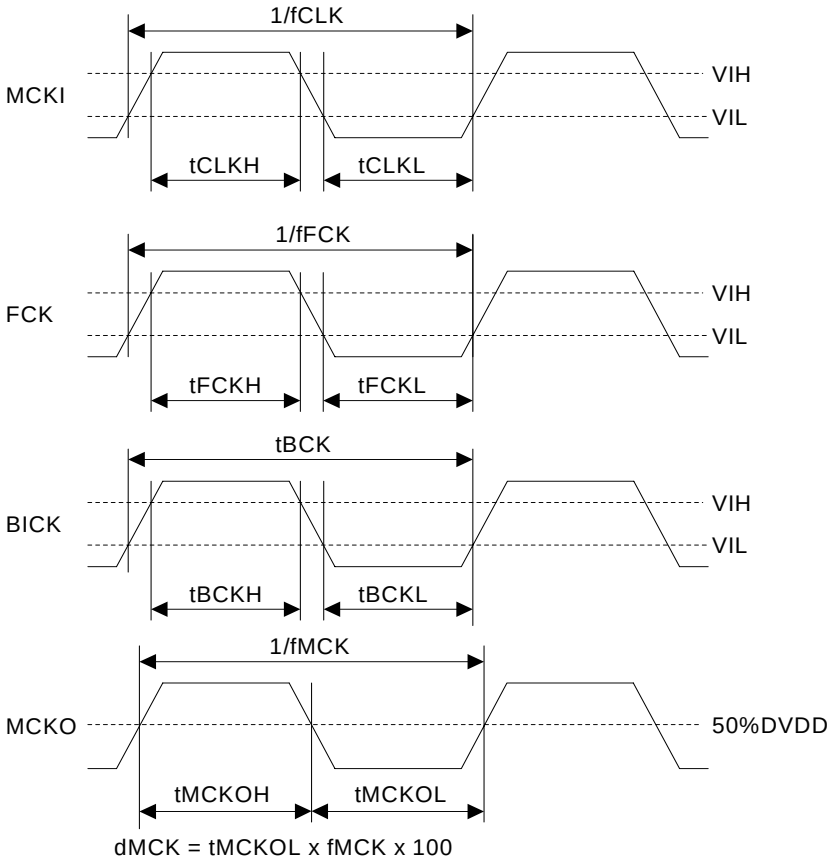


Figure 9. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin & Except DSP mode)

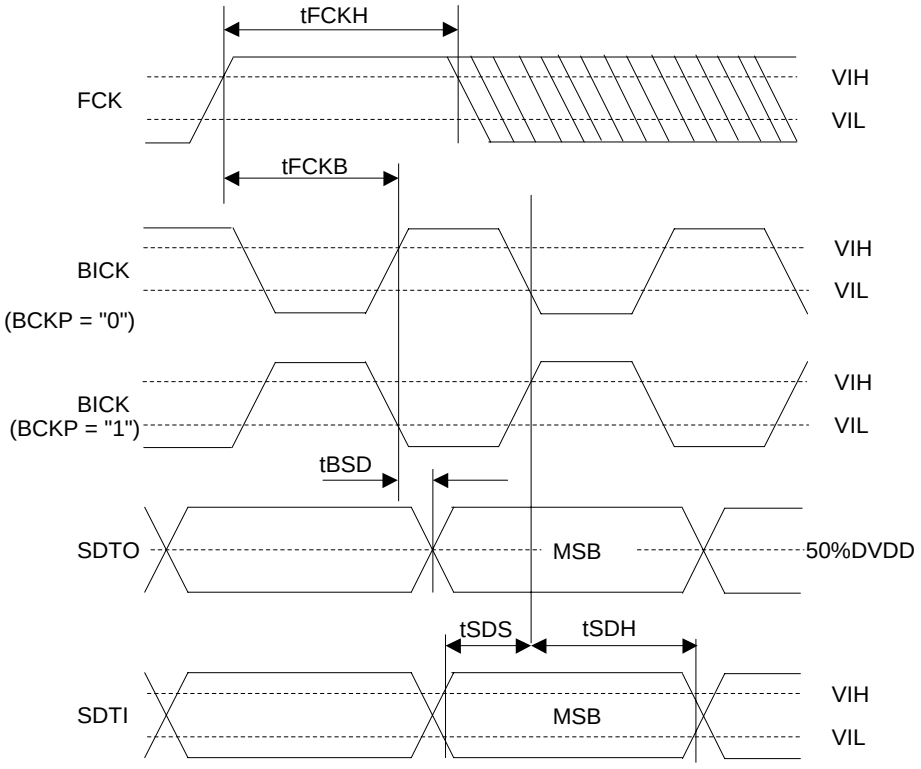


Figure 10. Audio Interface Timing (PLL Slave mode & DSP mode; MSBS = 0)

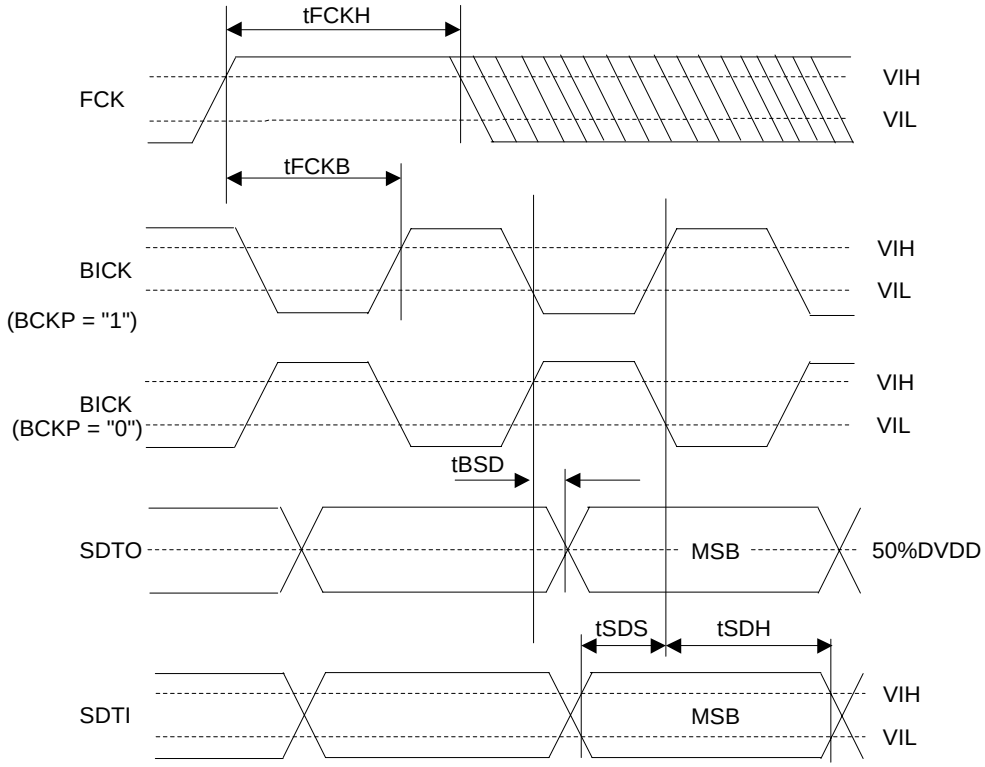


Figure 11. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = 1)

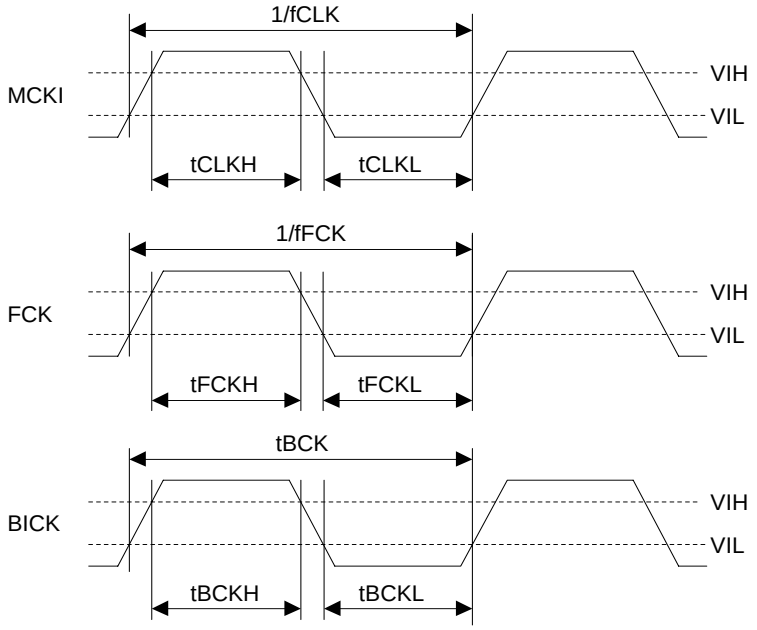


Figure 12. Clock Timing (EXT Slave mode)

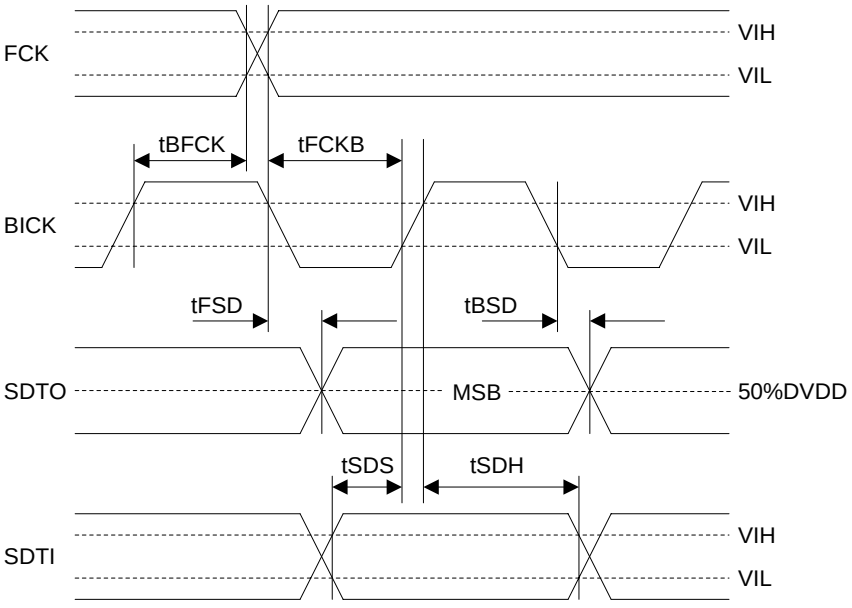


Figure 13. Audio Interface Timing (PLL, EXT Slave mode & Except DSP mode)

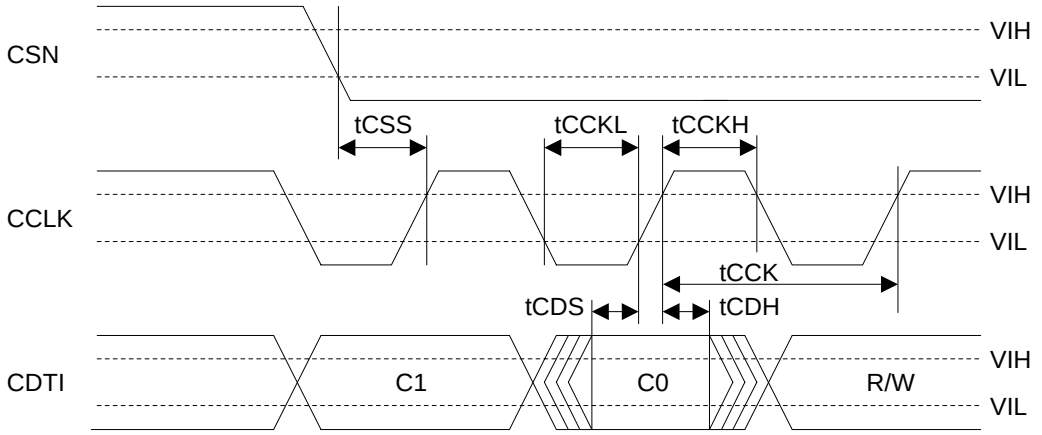


Figure 14. WRITE Command Input Timing

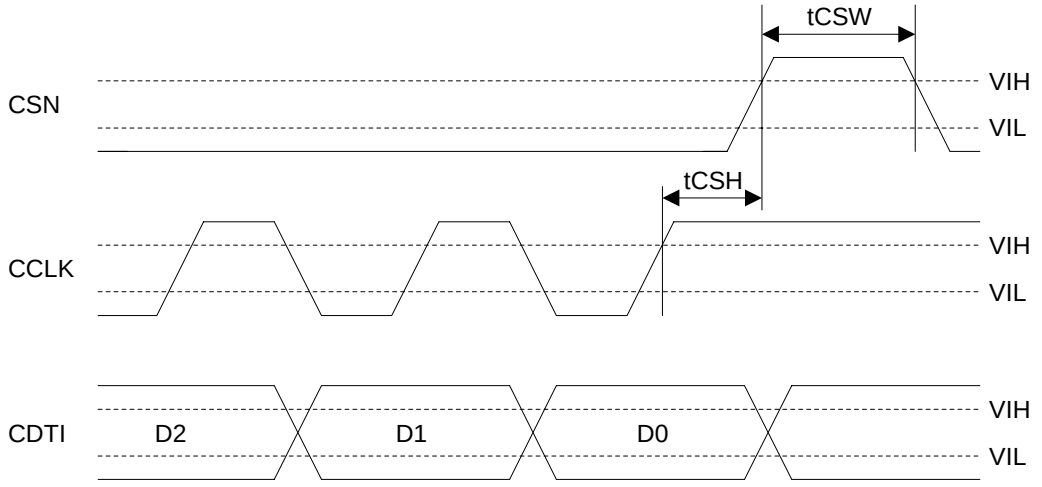


Figure 15. WRITE Data Input Timing

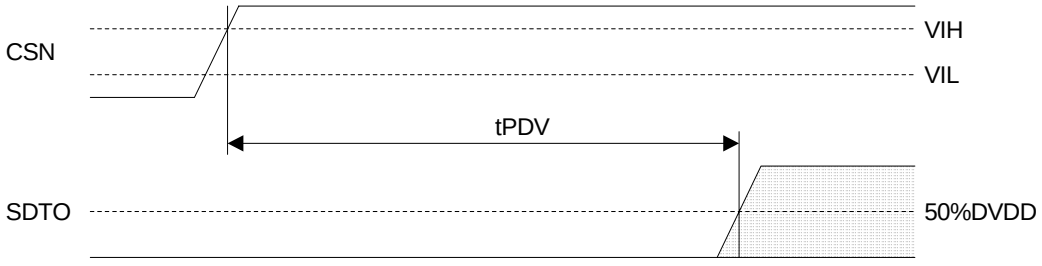


Figure 16. Power Down & Reset Timing 1

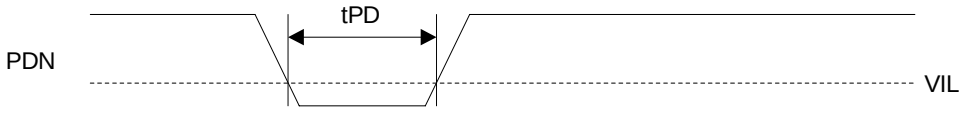


Figure 17. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following four clock modes to interface with external devices. (See Table 1 and Table 2)

Mode	PMPLL bit	M/S bit	PLL3-0 bit	MCKPD bit	Figure
PLL Master Mode	1	1	See Table 4	0	Figure 19
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	See Table 4	0	Figure 20
PLL Slave Mode 2 (PLL Reference Clock: FCK or BICK pin)	1	0	See Table 4	1	Figure 21
EXT Slave Mode	0	0	X	0	Figure 22
Invalid state (Note 36)	0	1	X	X	-

Table 1. Clock Mode Setting (X: Don't care)

Note 36. If this mode is selected, the invalid clocks are output from MCKO, FCK and BICK pins.

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	FCK pin
PLL Master Mode	0	"L" Output	Master Clock Input for PLL (Note 37)	16fs/32fs/64fs Output	1fs Output
	1	256fs Output			
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	0	"L" Output	Master Clock Input for PLL (Note 37)	16fs/32fs/64fs Input	1fs Input
	1	256fs Output			
PLL Slave Mode 2 (PLL Reference Clock: FCK or BICK pin)	0	"L" Output	GND	16fs/32fs/64fs Input	1fs Input
EXT Slave Mode	0	"L" Output	256fs/ 512fs/ 1024fs Input	≥ 32fs Input	1fs Input

Note 37. 11.2896MHz/12MHz/12.288MHz/13.5MHz/24MHz/27MHz
Table 2. Clock pins state in Clock Mode

[Pull-down resistor of MCKI pin]

When the master clock is input, MCKPD bit should be "0". When the MCKI pin is floating, the pin should be pulled-down by internal 25kΩ resistor at MCKPD bit = "1"(Default).

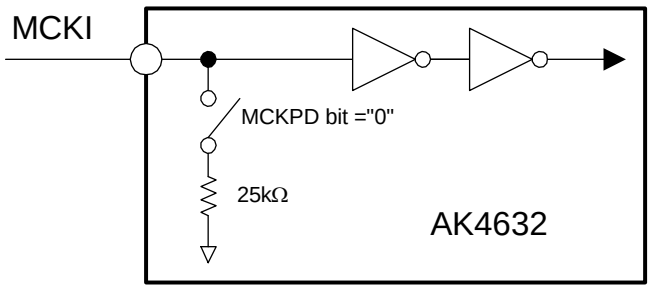


Figure 18. Pull-down resistor of MCKI pin

■ Master Mode/Slave Mode

The M/S bit selects either master or slave modes. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4632 is power-down mode (PDN pin = "L") and exits reset state, the AK4632 is slave mode. After exiting reset state, the AK4632 goes master mode by changing M/S bit = "1".

When the AK4632 is used by master mode, FCK and BICK pins are a floating state until M/S bit becomes "1". FCK and BICK pins of the AK4632 should be pulled-down or pulled-up by about 100kΩ resistor externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	Default
1	Master Mode	

Table 3. Select Master/Salve Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, whenever the AK4632 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency changes.

1) Setting of PLL Mode

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	FCK pin	1fs	6.8k	220n	160ms	Default
1	0	0	0	1	BICK pin	16fs	10k	4.7n	2ms	
2	0	0	1	0	BICK pin	32fs	10k	4.7n	2ms	
3	0	0	1	1	BICK pin	64fs	10k	4.7n	2ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10k	4.7n	40ms	
5	0	1	0	1	MCKI pin	12.288MHz	10k	4.7n	40ms	
6	0	1	1	0	MCKI pin	12MHz	10k	4.7n	40ms	
7	0	1	1	1	MCKI pin	24MHz	10k	4.7n	40ms	
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	40ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	40ms	
Others	Others				N/A					

Table 4. Setting of PLL Mode (*fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode.

When PLL2 bit is "1" (PLL reference clock input is MCKI pin), the sampling frequency is selected by FS2-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	Default
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
4	0	1	0	0	7.35kHz	
5	0	1	0	1	11.025kHz	
6	0	1	1	0	14.7kHz	
7	0	1	1	1	22.05kHz	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
14	1	1	1	0	29.4kHz	
15	1	1	1	1	44.1kHz	
Others	Others				N/A	

Table 5. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1"

When PLL2 bit is "0" (PLL reference clock input is FCK or BICK pin), the sampling frequency is selected by FS3, FS1-0 bits. (See Table 6)

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	Don't care	0	0	7.35kHz ≤ fs ≤ 8kHz	Default
1	0	Don't care	0	1	8kHz < fs ≤ 12kHz	
2	0	Don't care	1	0	12kHz < fs ≤ 16kHz	
3	0	Don't care	1	1	16kHz < fs ≤ 24kHz	
6	1	Don't care	1	0	24kHz < fs ≤ 32kHz	
7	1	Don't care	1	1	32kHz < fs ≤ 48kHz	
Others	Others				N/A	

Table 6. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL bit = "1"

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, irregular frequency clocks are output from FCK, BICK and MCKO pins after PMPLL bit = "0" → "1" or sampling frequency is changed. After that PLL is unlocked, BICK and FCK pins output "L" for a moment, and invalid frequency clock is output from MCKO pin at MCKO bit = "1". If MCKO bit is "0", MCKO pin is output to "L". (See Table 7)

After the PLL is locked, a first period of FCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

PLL State	MCKO pin		BICK pin	FCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After that PMPLL bit "0" → "1"	"L" Output	Invalid	Invalid	Invalid
PLL Unlock	"L" Output	Invalid	"L" Output	"L" Output
PLL Lock	"L" Output	256fs Output	See Table 9	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from MCKO pin after PMPLL bit = "0" → "1" or sampling frequency is changed. After that, 256fs is output from MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal should be muted by writing "0" to DACA and DACM bits in Addr=02H.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After that PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock	"L" Output	Invalid
PLL Lock	"L" Output	256fs Output

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz , 12.288MHz, 13.5MHz, 24MHz or 27MHz) is input to MCKI pin, the MCKO, BICK and FCK clocks are generated by an internal PLL circuit. The MCKO output frequency is fixed to 256fs, the output is enabled by MCKO bit. The BICK is selected among 16fs, 32fs or 64fs, by BCKO1-0 bits. (See Table 9)

When BICK output frequency is 16fs, the audio interface format supports only Mode 0 (DSP Mode).

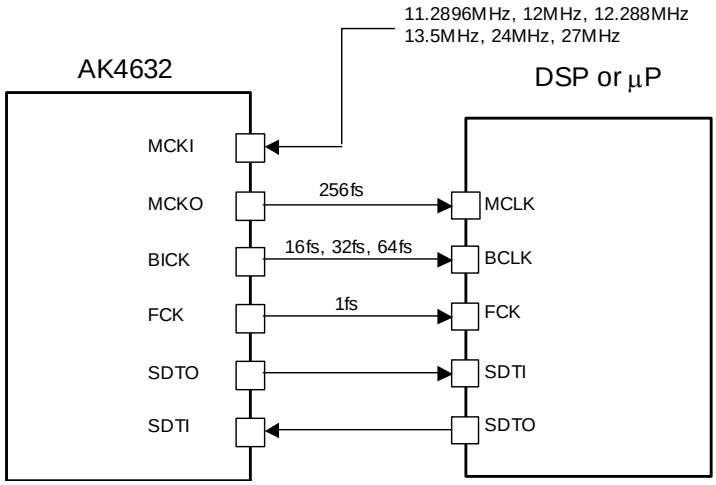


Figure 19. PLL Master Mode

Mode	BCKO1	BCKO0	BICK Output Frequency	
0	0	0	16fs	Default
1	0	1	32fs	
2	1	0	64fs	
3	1	1	N/A	

Table 9. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to MCKI, BICK or FCK pin. The required clock to the AK4632 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits. When BICK input frequency is 16fs, the audio interface format supports only Mode 0 (DSP Mode).

a) PLL reference clock: BICK or FCK pin

In the case of using BICK as PLL reference clock, the sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits. In the case of using FCK, the sampling frequency corresponds to 7.35kHz to 26kHz. (SeeTable 6)

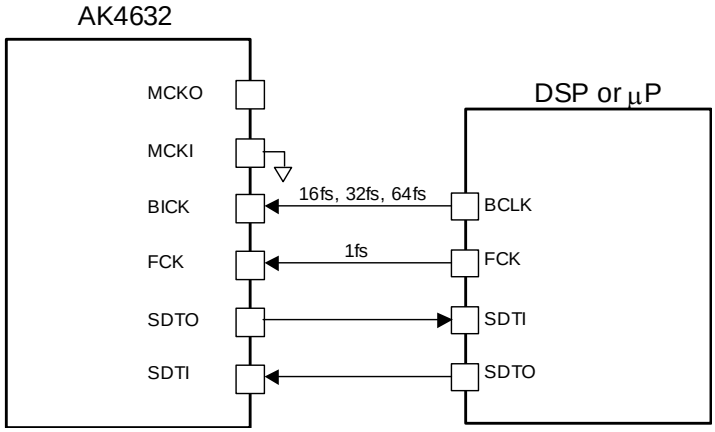


Figure 20. PLL Slave Mode 1 (PLL Reference Clock: FCK or BICK pin)

b) PLL reference clock: MCKI pin

BICK and FCK inputs should be synchronized with MCKO output. The phase between MCKO and FCK dose not matter. Sampling frequency can be selected by FS3-0 bits. (See Table 5)

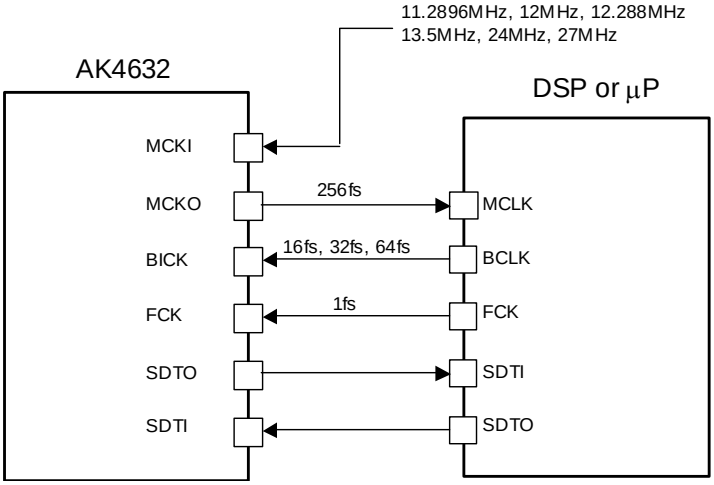


Figure 21. PLL Slave Mode 2 (PLL Reference Clock: MCKI pin)

The external clocks (MCKI, BICK and FCK) should always be present whenever the ADC or DAC is in operation (PMADC bit = "1" or PMDAC bit = "1"). If these clocks are not provided, the AK4632 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADC bit =PMDAC bit = "0").

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4632 becomes EXT mode. Master clock is input from MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 512fs or 1024fs), FCK (fs) and BICK (32fs~). The master clock (MCKI) should be synchronized with FCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS3-0 bits. (See Table 10)

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	Don't care	0	0	256fs	7.35kHz ≤ fs ≤ 48kHz	Default
1	Don't care	0	1	1024fs	7.35kHz < fs ≤ 13kHz	
2	Don't care	1	0	256fs	7.35kHz < fs ≤ 48kHz	
3	Don't care	1	1	512fs	7.35kHz < fs ≤ 26kHz	

Table 10. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

External Slave Mode does not support Mode 0 (DSP Mode) of Audio Interface Format.

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. When the out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through AOUT amp at fs=8kHz is shown in Table 11.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weight)
256fs	83dB
512fs	93dB
1024fs	93dB

Table 11. Relationship between MCKI and S/N of AOUT

The external clocks (MCKI, BICK and FCK) should always be present whenever the ADC or DAC is in operation (PMADC bit = "1" or PMDAC bit = "1"). If these clocks are not provided, the AK4632 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADC bit = PMDAC bit = "0").

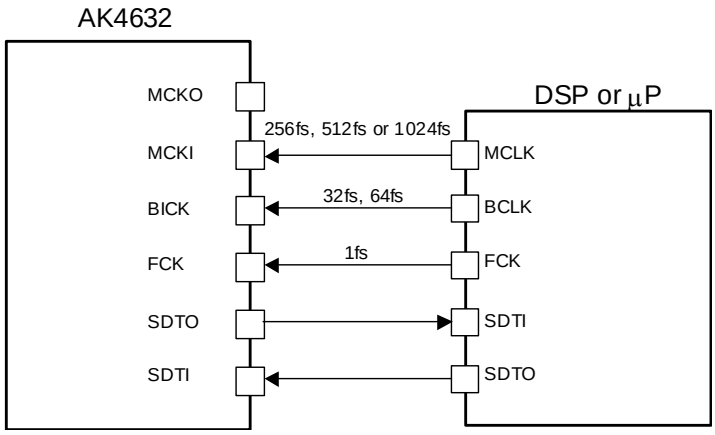


Figure 22. EXT Slave Mode

■ Audio Interface Format

Four types of data formats are available and are selected by setting the DIF1-0 bits. (See Table 12) In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. FCK and BICK are output from AK4632 in master mode, but must be input to AK4632 in slave mode.

In Mode 1-3, the SDTO is clocked out on the falling edge of BICK and the SDTI is latched on the rising edge.

Mode	DIF1	DIF0	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	DSP Mode	DSP Mode	≥ 16fs	See Table 13	
1	0	1	MSB justified	MSB justified	≥ 32fs	Figure 27	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 28	Default
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 29	

Table 12. Audio Interface Format

In Mode0 (DSP mode), the audio I/F timing is changed by BCKP and MSBS bits.

When BCKP bit is "0", SDTO data is output by rising edge of BICK, SDTI data is latched by falling edge of BICK.
When BCKP bit is "1", SDTO data is output by falling edge of BICK, SDTI data is latched by rising edge of BICK.

MSB data position of SDTO and SDTI can be shifted by MSBS bit. The shifted period is a half of BICK.

MSBS bit	BCKP bit	Audio Interface Format	
0	0	Figure 23	Default
0	1	Figure 24	
1	0	Figure 25	
1	1	Figure 26	

Table 13. Audio Interface Format in Mode 0

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, "–1" at 16bit data is converted to "–1" at 8-bit data. And when the DAC playbacks this 8-bit data, "–1" at 8-bit data will be converted to "–256" at 16-bit data and this is a large offset. This offset can be removed by adding the offset of "128" to 16-bit data before converting to 8-bit data.

■ System Reset

Upon power-up, reset the AK4632 by bringing the PDN pin = "L". This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle that starts when the PMADC bit is changed from "0" to "1". The initialization cycle time is 1059/fs, or 133ms@fs=8kHz. During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's compliment, "0". The ADC output reflects the analog input signal after the initialization cycle is complete. The DAC does not require an initialization cycle.

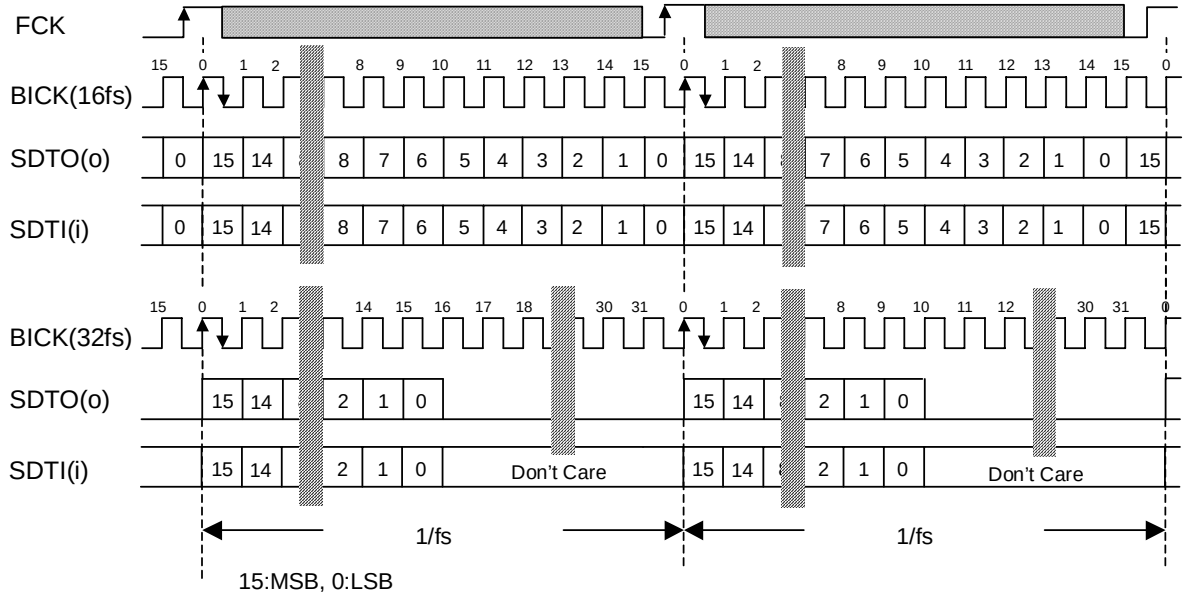


Figure 23. Mode 0 Timing (BCKP = "0", MSBS = "0")

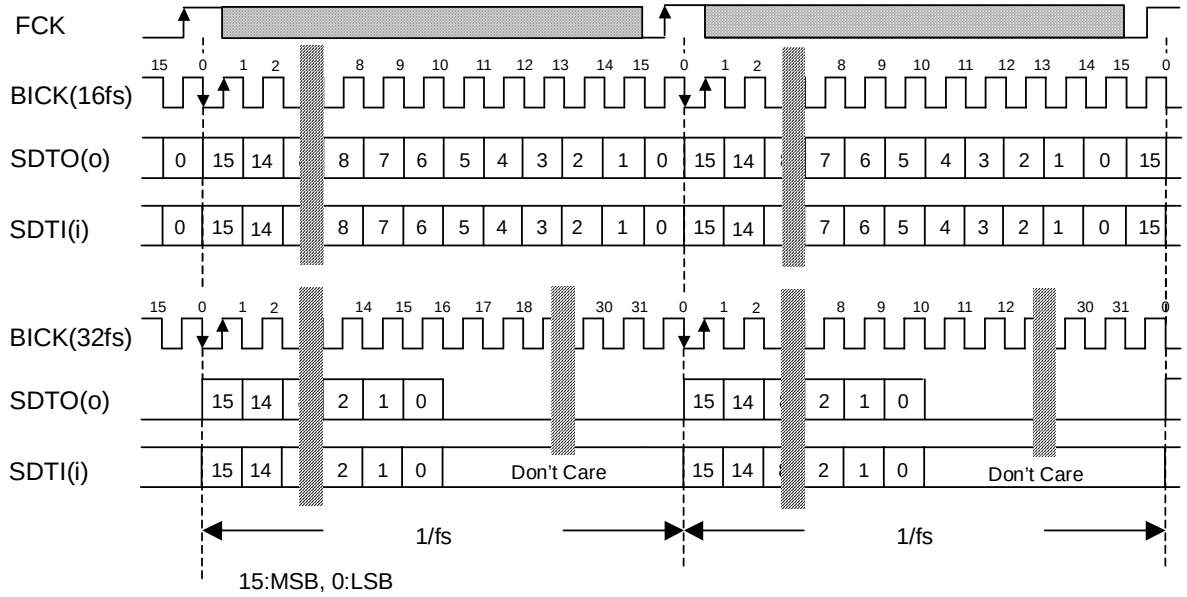


Figure 24. Mode 0 Timing (BCKP = "1", MSBS = "0")

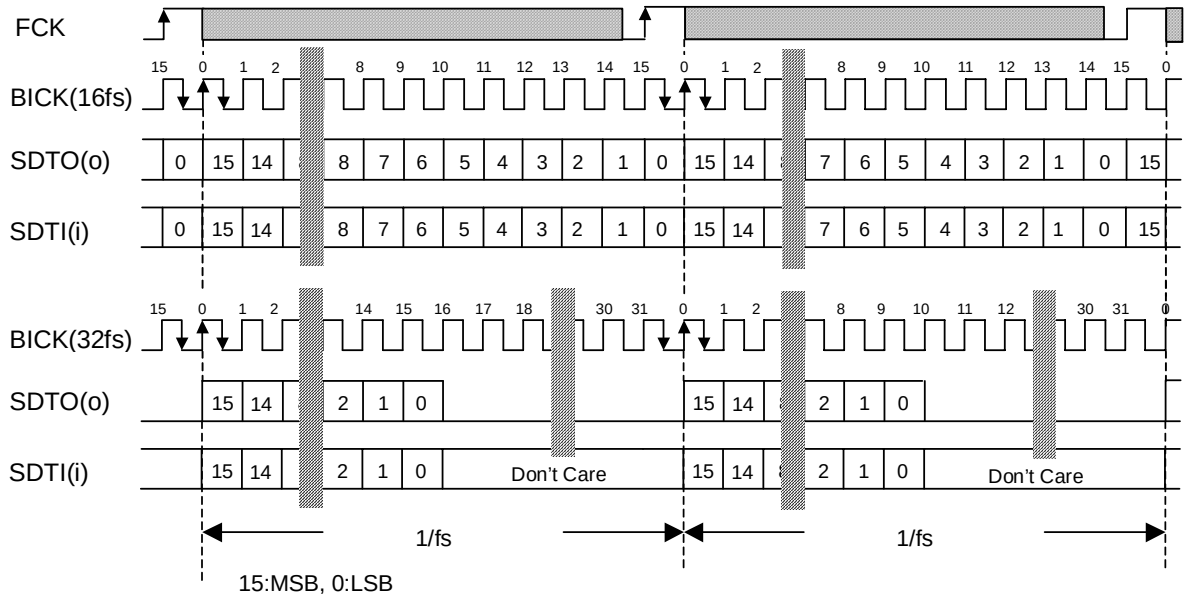


Figure 25. Mode 0 Timing (BCKP = "0", MSBS = "1")

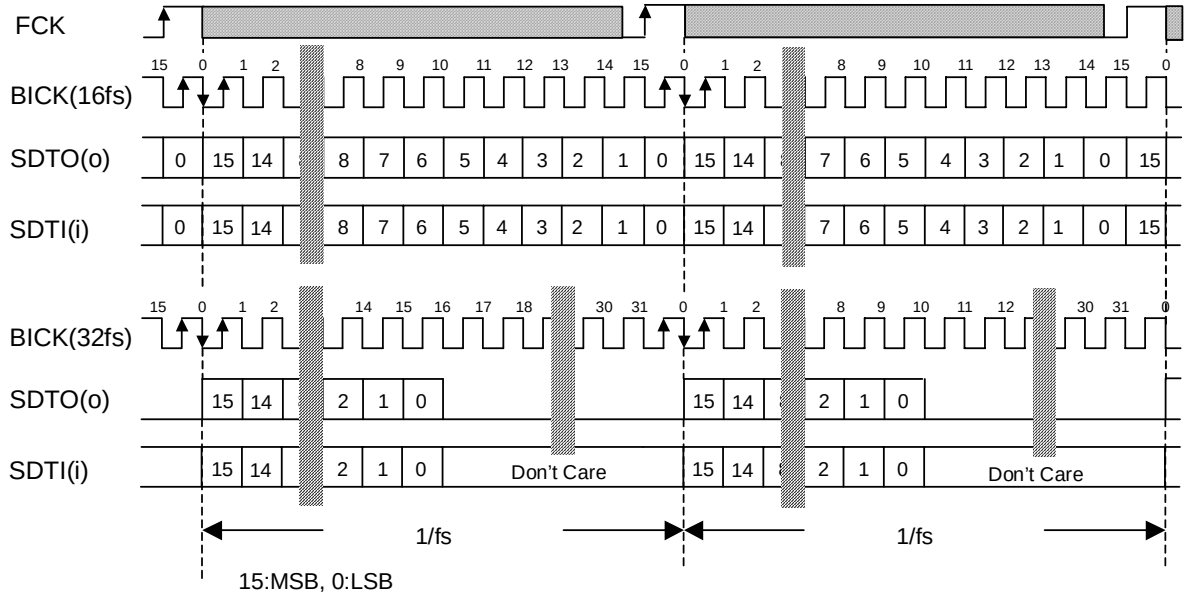


Figure 26. Mode 0 Timing (BCKP = "1", MSBS = "1")

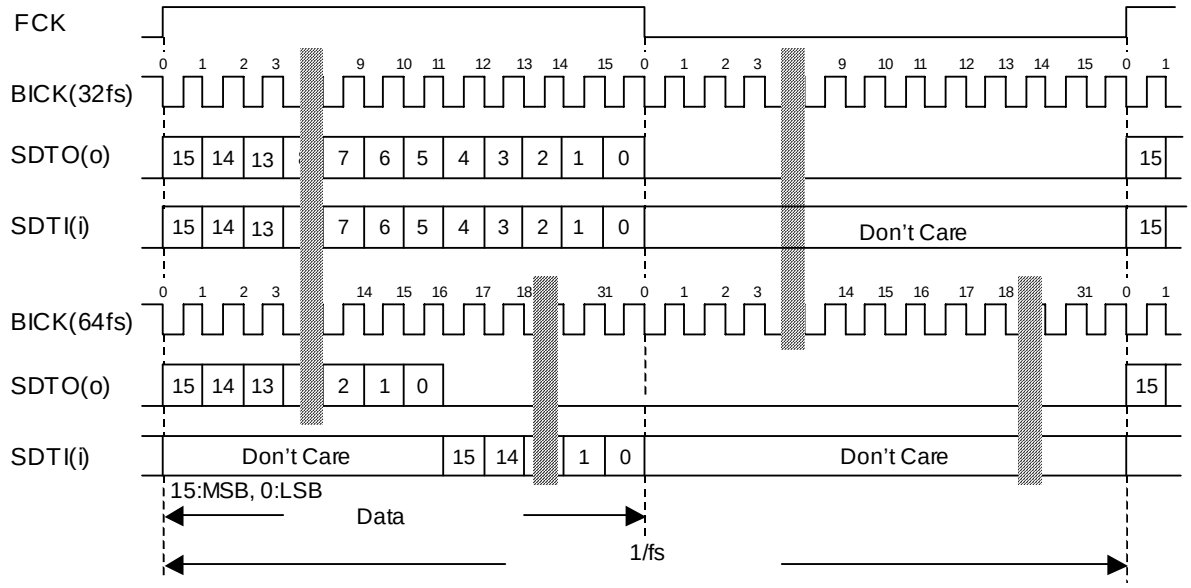


Figure 27. Mode 1 Timing

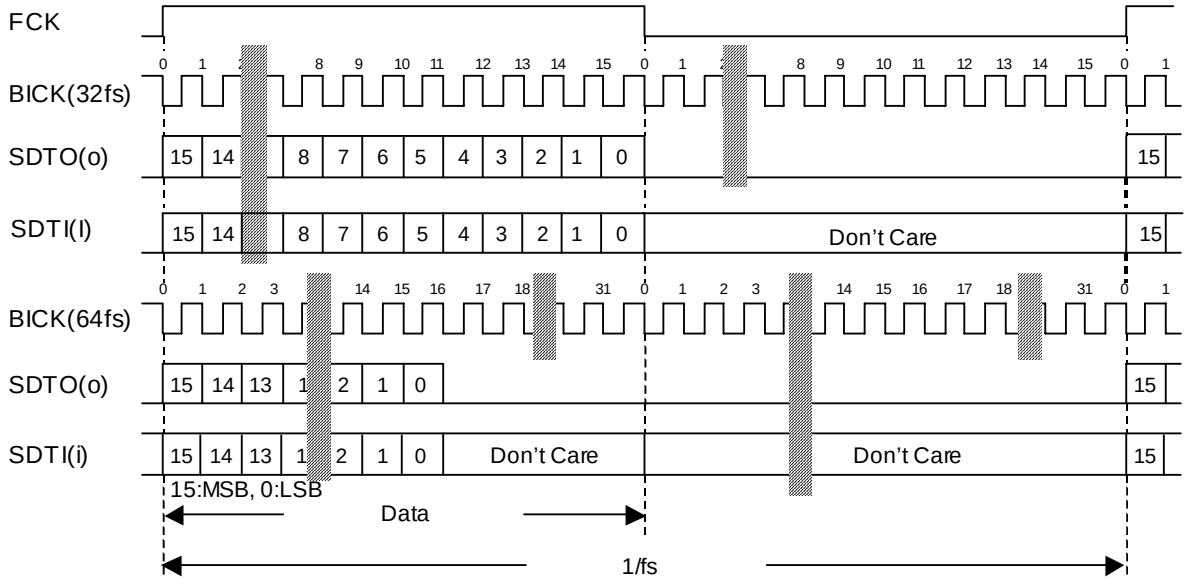


Figure 28. Mode 2 Timing

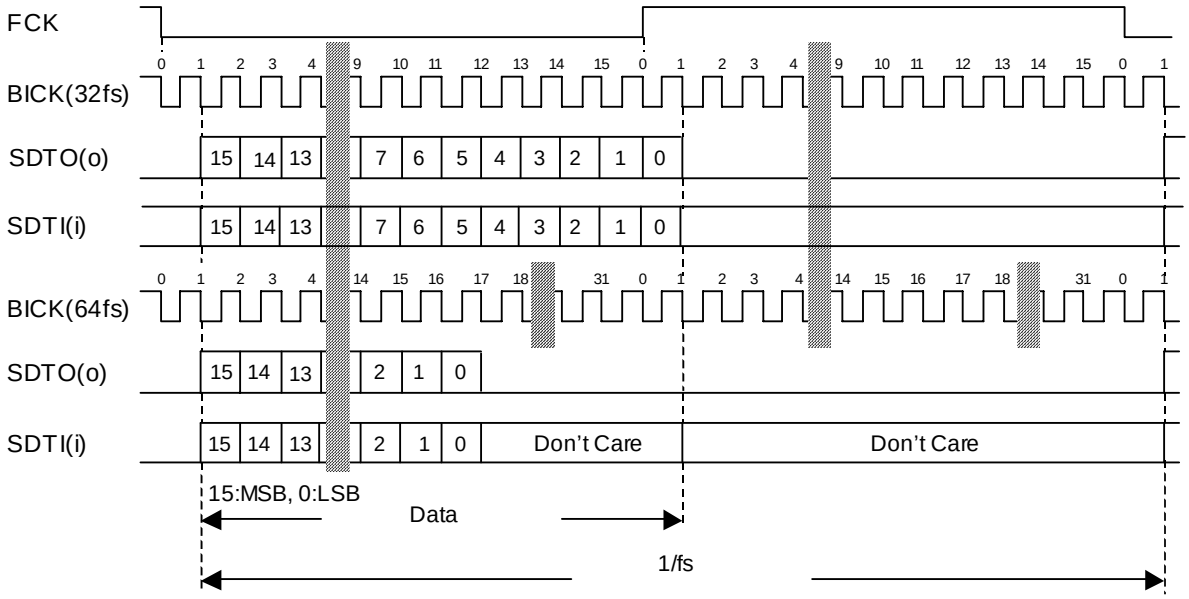


Figure 29. Mode 3 Timing

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.25Hz (@fs=8kHz) and scales with sampling rate (fs).

■ MIC Gain Amplifier

The AK4632 has a Gain Amplifier for Microphone input. This gain is 0dB, +20dB, +26dB or +32dB, selected by the MGAIN1-0 bit. The typical input impedance is 30kΩ.

MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0dB	
0	1	+20dB	Default
1	0	+26dB	
1	1	+32dB	

Table 14. Input Gain

■ MIC Power

The MPI pin supplies power for the Microphone. This output voltage is typically 0.75 x AVDD and the load resistance is minimum 2kΩ. No capacitor must not be connected directly to MPI pin. (See Figure 30)

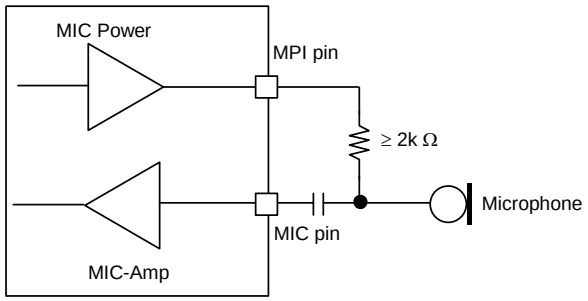


Figure 30. MIC Block Circuit

■ Manual Mode

The AK4632 becomes a manual mode at ALC1 bit = "0". This mode is used in the case shown below.

1. After exiting reset state, set up the registers for the ALC1 operation (ZTM1-0, LMTH and etc)
2. When the registers for the ALC1 operation (Limiter period, Recovery period and etc) are changed. For example; When the change of the sampling frequency.
3. When IPGA is used as a manual volume.

When IPGA6-0 bits are written at manual mode, the counter for zero cross time out is reset and restart. The IPGA6-0 bits value are reflected to IPGA at zero cross or zero cross time out. The time of zero cross time out is set by ZTM1-0 bits.

When writing to IPGA6-0 bits continually, the control register should be written by an interval of more than zero crossing timeout.

■ MIC-ALC Operation

The ALC (Automatic Level Control) of MIC input is done by ALC1 block when ALC1 bit is "1".

[1] ALC1 Limiter Operation

When the ALC1 limiter is enabled, and IPGA output exceeds the ALC1 limiter detection level (LMTH), the IPGA value is attenuated by the amount defined in the ALC1 limiter ATT step (LMAT1-0 bits) automatically.

When the ZELM bit = "1", the timeout period is set by the LTM1-0 bits. The operation for attenuation is done continuously until the input signal level becomes LMTH or less. If the ALC1 bit does not change into "0" after completing the attenuation, the attenuation operation repeats while the input signal level equals or exceeds LMTH.

When the ZELM bit = "0", the timeout period is set by the ZTM1-0 bits. This enables the zero-crossing attenuation function so that the IPGA value is attenuated at the zero-detect points of the waveform.

[2] ALC1 Recovery Operation

The ALC1 recovery refers to the amount of time that the AK4632 will allow a signal to exceed a predetermined limiting value prior to enabling the limiting function. The ALC1 recovery operation uses the WTM1-0 bits to define the wait period used after completing an ALC1 limiter operation. If the input signal does not exceed the "ALC1 Recovery Waiting Counter Reset Level", the ALC1 recovery operation starts. The IPGA value increases automatically during this operation up to the reference level (REF6-0 bits). The ALC1 recovery operation is done at a period set by the WTM1-0 bits. Zero crossing is detected during WTM1-0 period, the ALC1 recovery operation waits WTM1-0 period and the next recovery operation starts.

During the ALC1 recovery operation, when input signal level exceeds the ALC1 limiter detection level (LMTH), the ALC1 recovery operation changes immediately into an ALC1 limiter operation.
In the case of "(Recovery waiting counter reset level) ≤ IPGA Output Level < Limiter detection level" during the ALC1 recovery operation, the wait timer for the ALC1 recovery operation is reset. Therefore, in the case of "(Recovery waiting counter reset level) > IPGA Output Level", the wait timer for the ALC1 recovery operation starts.

The ALC1 operation corresponds to the impulse noise. When the impulse noise is input, the ALC1 recovery operation becomes faster than a normal recovery operation.

[3] Example of ALC1 Operation

Table 15 shows the example of the ALC1 setting. In case of this example, ALC1 operation starts from 0dB.

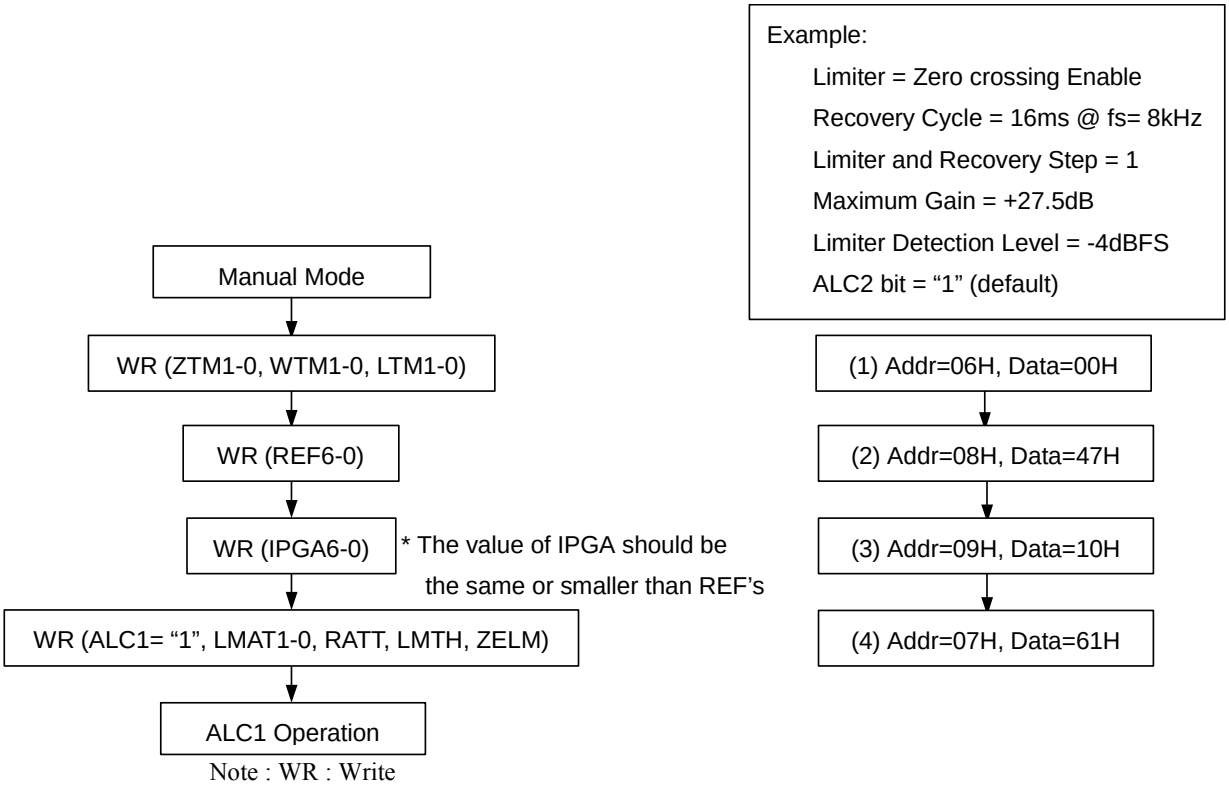
Register Name	Comment	fs=8kHz		fs=16kHz	
		Data	Operation	Data	Operation
LMTH	Limiter detection Level	1	-4dBFS	1	-4dBFS
LTM1-0	Limiter operation period at ZELM = 1	00	Don't use	00	Don't use
ZELM	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	00	16ms	01	16ms
WTM1-0	Recovery waiting period *WTM1-0 bits should be the same data as ZTM1-0 bits	00	16ms	01	16ms
REF6-0	Maximum gain at recovery operation	47H	+27.5dB	47H	+27.5dB
IPGA6-0	IPGA gain at the start of ALC1 operation	10H	0dB	10H	0dB
LMAT1-0	Limiter ATT Step	00	1 step	00	1 step
RATT	Recovery GAIN Step	0	1 step	0	1 step
ALC1	ALC1 Enable bit	1	Enable	1	Enable

Table 15. Examples of the ALC1 Setting

The following registers should not be changed during the ALC1 operation. These bits should be changed, after the ALC1 operation is finished by ALC1 bit = "0" or PMMIC bit = "0".

- **LTM1-0, LMTH, LMAT1-0, WTM1-0, ZTM1-0, RATT, REF6-0, ZELM bits**

When setting IPGA gain at the start of ALC1 operation, IPGA6-0 bits should be set while PMMIC bit is "1" and ALC1 bit is "0". When PMMIC bit = "1", IPGA6-0 bits value aren't reflected to IPGA. When ALC1 bit is changed from "1" to "0", IPGA holds the last gain value set automatically by ALC1 operation.



Note : WR : Write

Figure 31. Registers set-up sequence at the ALC1 operation

■ Digital Output Volume

The AK4632 has a digital output volume (256 levels, 0.5dB step, Mute). The volume can be set by the DVOL7-0 bits. The volume is included in front of a DAC block, a input data of DAC is changed from +12 to –115dB with MUTE. This volume has a soft transition function. It takes 1061/fs or 256/fs from 00H to FFH.

DVOL7-0	Gain	
00H	+12.0dB	
01H	+11.5dB	
02H	+11.0dB	
•	•	
18H	0dB	Default
•	•	
FDH	–114.5dB	
FEH	–115.0dB	
FFH	MUTE (–∞)	

Table 16. Digital Output Volume Code Table

DVTM bit	The transition time from 00H to FFH of DVOL7-0 bits		
	Transition Time	fs=8kHz	fs=22.05kHz
0	1061/fs	133msec	48msec
1	256/fs	32msec	12msec

Table 17.Setting of transition time

■ BEEP Input

When the PMBP bit is set to “1”, the beep input is powered-up. And when the BEEPS bit is set to “1”, the input signal from the BEEP pin is output to Speaker-Amp. When the BEEPA bit is set to “1”, the input signal from the BEEP pin is output to the mono line output amplifier. The external resister Ri adjusts the signal level of BEEP input. The gains are shown in Table 18, when Ri = 20kΩ. These gain are in inverse proportion to Ri.

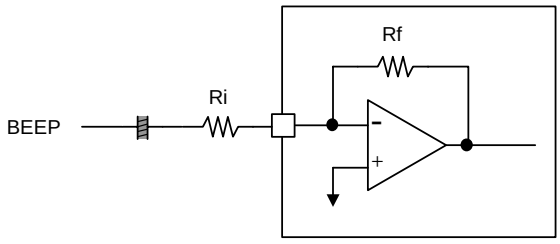


Figure 32. Block Diagram of BEEP pin

SPKG1-0 bits	BEEP → SPP/SPN Gain	BEEP → AOUT Gain
00	+7.89dB	0dB
01	+9.93dB	0dB
10	+14.11dB	0dB
11	+16.15dB	0dB

Table 18. Beep input gain at R_i = 20kΩ

■ MONO LINE OUTPUT (AOUT pin)

A signal of DAC is output from AOUT pin. When the DACA bit is "0", this output is OFF. The load resistance is 10kΩ(min). When PMAO bit is "0" and AOPSN bit is "0", the mono line output enters power-down and is pulled down by 100Ω(typ). If PMAO bit is controlled at AOPSN bit = "1", POP noise will be reduced at power-up and down. Then, this line should be pulled down by 20kΩ of resister after C-coupling shown in Figure 33. This rising and falling time is max 300 ms at C=1.0μF . When PMAO bit is "1" and AOPSN bit is "0", the mono line output enters power-up state.

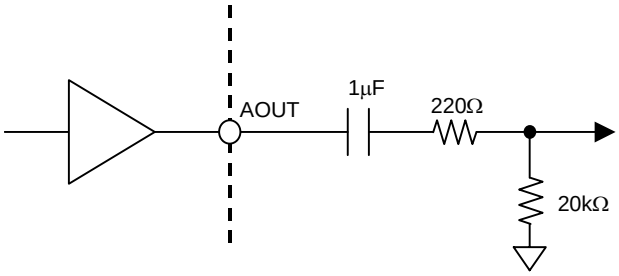


Figure 33. AOUT external circuit in case of using POP Reduction function.

AOUT Control Sequence in case of using POP Reduction Circuit

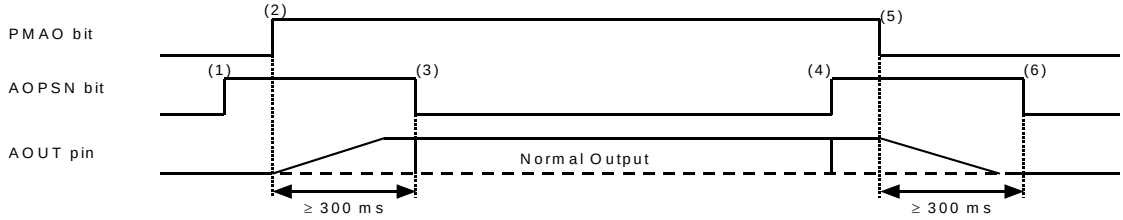


Figure 34. Mono Line Output Control Sequence in case of using POP Reduction function..

(1) Set AOPSN bit = "1". Mono line output enters the power-save mode.
(2) Set PMAO bit = "1". Mono line output exits the power-down mode.
AOUT pin rises up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF.
(3) Set AOPSN bit = "0" after AOUT pin rises up. Mono line output exits the power-save mode.
Mono line output is enabled.
(4) Set AOPSN bit = "1". Mono line output enters power-save mode.
(5) Set PMAO bit = "1". Mono line output enters power-down mode.
AOUT pin falls down to AVSS. Fall time is 200ms (max 300ms) at C=1μF.
(6) Set AOPSN bit = "0" after AOUT pin falls down. Mono line output exits the power-save mode.

■ Speaker Output

The power supply voltage for Speaker-Amp SVDD can be set to from 2.6V to 5.25V. However, SVDD should be set to from 2.6V to 3.6V, when the load resistance is less than 50Ω(ex. a dynamic speaker).

The output signal from DAC is input to the Speaker-amp via the ALC2 circuit. This Speaker-amp is a mono output controlled by BTL and a gain of the Speaker-Amp is set by SPKG1-0 bit. In the case of ALC2 OFF, the output voltage depends on AVDD and SPKG1-0 bits. In the case of ALC2 ON, the output voltage depends on SVDD and SPKG1-0 bits. The output level of ALC2 is proportional to SVDD.

SPKG1-0 bits	Gain
00	0dB
01	+2.04dB
10	+6.22dB
11	+8.26dB

(Note) These Gain from the level at SPKG1-0bits= "00".
Table 19. Gain of Speaker-Amp at ALC2 OFF

SPKG1-0 bits	AVDD	SVDD	Output Voltage from Speaker-Amp at ALC2 OFF and DAC Input=0dBFS	Output Voltage from Speaker-Amp at ALC ON
00	3.3V	3.3V	3.27Vpp, 167mW@8Ω	3.09Vpp, 150mW@8Ω
01	3.3V	3.3V	4.15Vpp, 269mW@8Ω	3.92Vpp, 240mW@8Ω
10	3.3V	3.3V	6.91Vpp (Note)	Not Available
11	3.3V	3.3V	8.50Vpp (Note)	Not Available
00	3.3V	5.0V	3.27Vpp	Not Available
01	3.3V	5.0V	4.15Vpp	Not Available
10	3.3V	5.0V	6.91Vpp	6.34Vpp
11	3.3V	5.0V	8.50Vpp	8.02Vpp

(Note) This output voltage is assumed that the signal is not clipped. In actual, the signal will be clipped when DAC outputs 0dBFS signal. The output power is 400mW@8Ω, SVDD=3.3V.
Table 20. Speaker-Amp Output Voltage

[Caution for using Piezo Speaker]

When a piezo speaker (load capacitance > 30pF) is used, resistances more than 10Ω should be inserted between SPP/SPN pins and speaker in series, respectively, as shown in Figure 35. Zener diodes should be inserted between speaker and GND as shown in Figure 35, in order to protect SPK-Amp of AK4632 from the power that the piezo speaker outputs when the speaker is pressured. Zener diodes of the following Zener voltage should be used.

92% of SVDD ≤ Zener voltage of Zener diodo(ZD of Figure 35) ≤ SVDD+0.3V
Ex) In case of SVDD = 5.0V : 4.6V ≤ ZD ≤ 5.3V
For example, Zener diode which Zener voltage is 5.1V(Min :4.97V, Max 5.24V) can be used.

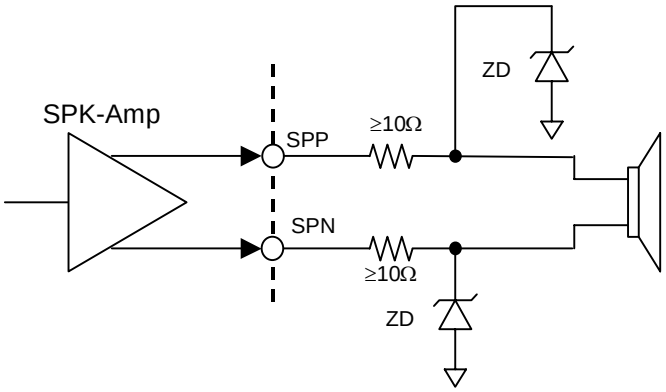


Figure 35. Circuit of Speaker Output(Load Capacitance > 30pF)

<Control Sequence of Speaker Amp>

Speaker blocks (MOUT, ALC2 and Speaker-amp) can be powered-up/down by controlling the PMSPK bit. When the PMSPK bit is "0", the MOUT, SPP and SPN pins are placed in a Hi-Z state.

When the PMSPK bit is "1" and SPPS bit is "0", the Speaker-amp enters power-save-mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to SVDD/2 voltage. And then the Speaker output gradually changes to the SVDD/2 voltage and this mode can reduce pop noise at power-up. When the AK4632 is powered-down, pop noise can be also reduced by first entering power-save-mode.

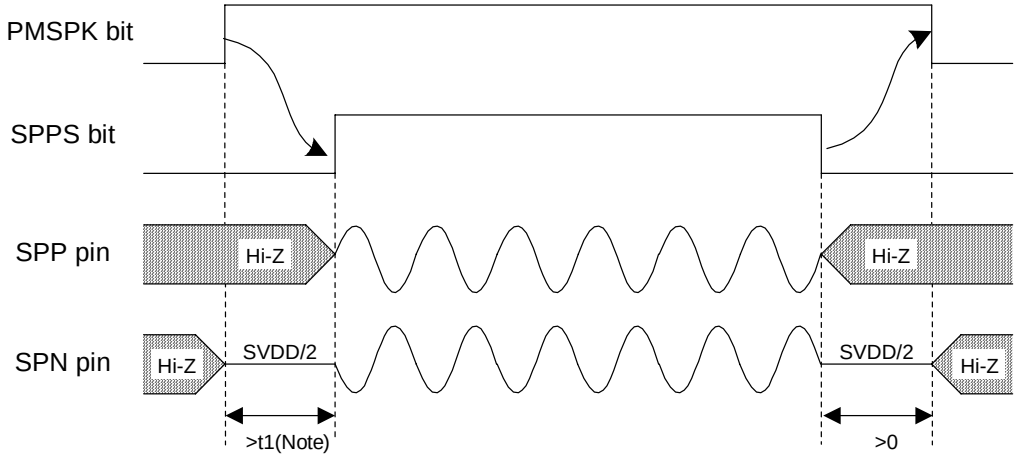


Figure 36. Power-up/Power-down Timing for Speaker-Amp

(Note)

"t1" depends on the time constant of input resistance of MIN and capacitor between MOUT pin and MIN pin. If Speaker-Amp output is enabled before MIN-Amp (ALC2) becomes stable, pop noise may occur.

Ex) C of MOUT pin – MIN pin = 0.1 μF, Input resistance of MIN pin = 36kΩ(Max) : t1 = 5τ = 18ms
C of MOUT pin – MIN pin and the Input resistance(Rin) of MIN pin compose of HPF which cut off frequency(fc) are the followings.
fc = 66Hz@Rin=24kΩ(typ), 133Hz@Rin=12kΩ(min), 44Hz@Rin=36kΩ(max)

■ SPK-ALC Operation

The ALC (Automatic Level Control) operation of speaker output is done by ALC2 block when ALC2 bit is "1". Input resistance of the ALC2 is 24kΩ (typ) and centered around VCOM voltage. The ALC2 level diagram is shown in Figure 37 ~Figure 40.

The limiter detection level is proportional to SVDD voltage. The output level is limited by the ALC2 circuit when the input signal exceeds –7.1dBV (@SPKG1 bit = "0", SVDD=3.3V or @SPKG1 bit = "1", SVDD = 5V). When a continuous signal of –7.1dBV or greater is input to the ALC2 circuit, the change period of the ALC2 limiter operation is 250µs (=2/fs@fs=8kHz) and the attenuation level is 0.5dB/step.

The ALC2 recovery operation uses zero crossings and gains of 1dB/step. The ALC2 recovery operation is done until the input level of the Speaker-amp goes to –9.1dBV (@SPKG1 bit = "0", SVDD=3.3V or @SPKG1 bit = "1", SVDD = 5V). Maximum gain of the ALC2 recovery operation is set by RFS5-0 bits.

When the input signal is between –9.1dBV and –7.1dBV, the ALC2 limiter or recovery operations are not done.

When the PMSPK bit changes from "0" to "1", the initilization cycle (512/fs = 64ms @fs=8kHz at ROTM bit = "0") starts. The ALC2 is disabled (The ALC2 gain is fixed to "-3.5dB".) during the initilization cycle and the ALC2 starts from "–2dB" after completing the initilization cycle. The ROTM bit and RFS5-0 bits set during the PMSPK bit = "0".

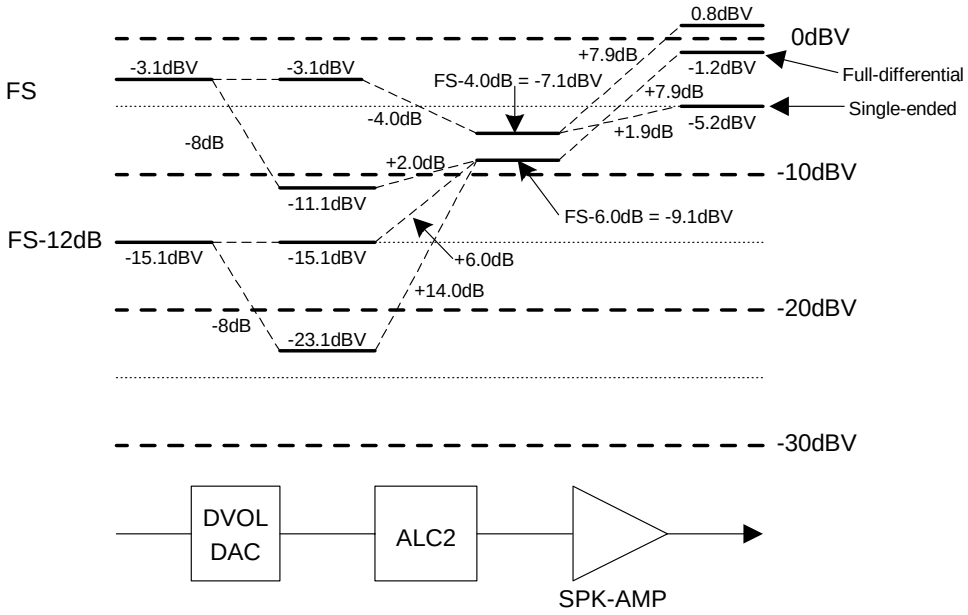
When the ALC2 is disable, a gain of the ALC2 block is fixed to -3.5dB. Therefore, a gain of internal speaker block is shown in Table 22.

Parameter		ALC2 Limiter operation	ALC2 Recovery operation
Operation Start Level		–5.2dBV	–7.2dBV
Period	fs=8kHz	2/fs = 250µs	512/fs=64ms
	fs=16kHz	2/fs = 125µs	512/fs=32ms
Zero-crossing Detection		No	Yes (Timeout = Period Time)
ATT/GAIN		0.5dB step	1dB step

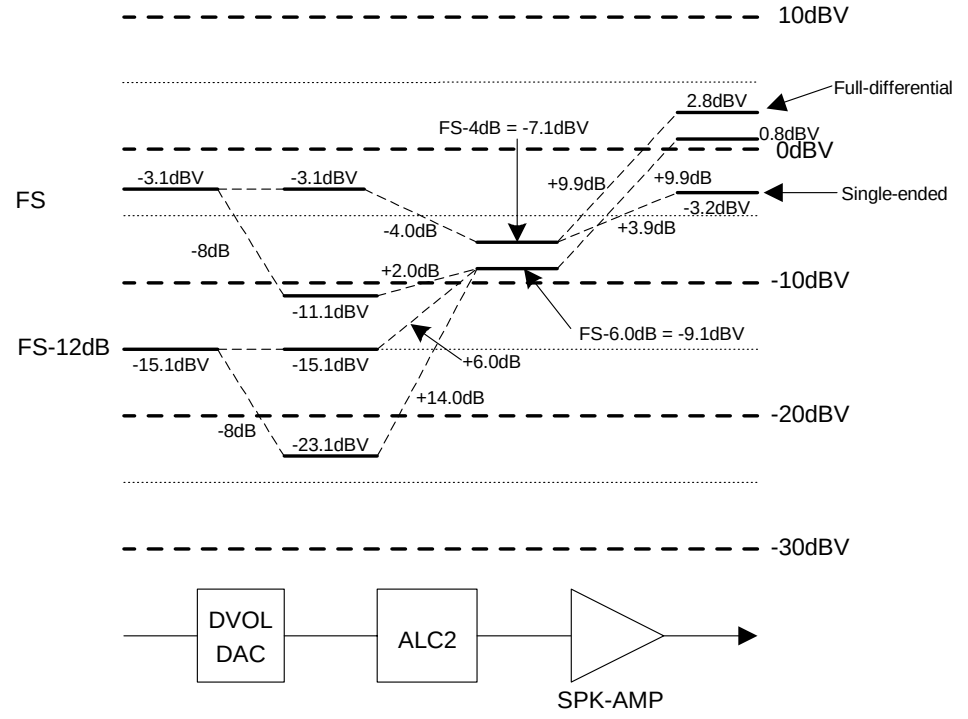
Table 21. Limiter /Recovery of ALC2 (ROTM bit = "0")

SPKG1-0 bits	Gain
00	+4.4dB
01	+6.4dB
10	+10.6dB
11	+12.7dB

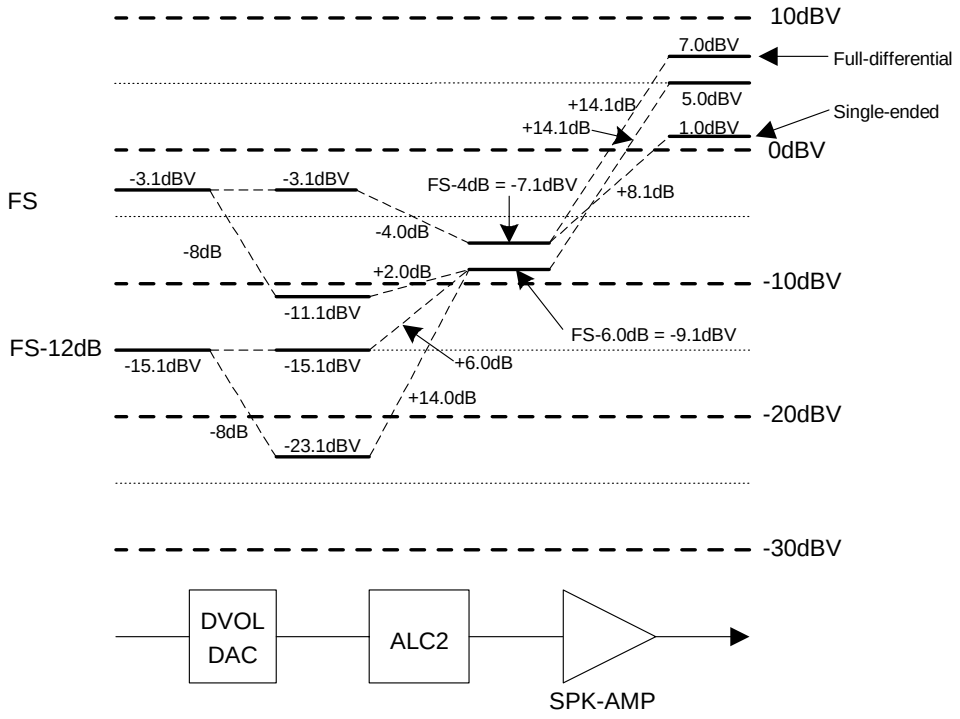
Table 22. Gain of Speaker-Amp at ALC2 OFF(Full-differential Output)



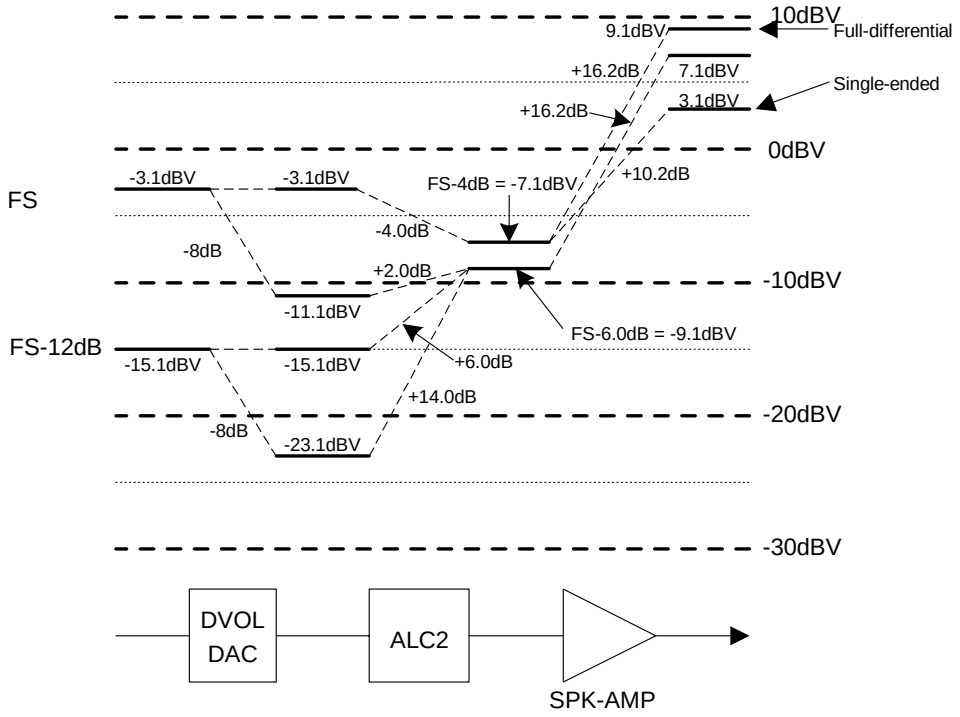
(AVDD=3.3V, SVDD=3.3V, DVOL=–8.0dB/0dB, SPKG1-0 bit = “00”,) * FS = Full Scale
Figure 37. Speaker-Amp Output Level Diagram



(AVDD=3.3V, SVDD=3.3V, DVOL=–8.0dB/0dB, SPKG1-0 bit = “01”,) * FS = Full Scale
Figure 38. Speaker-Amp Output Level Diagram



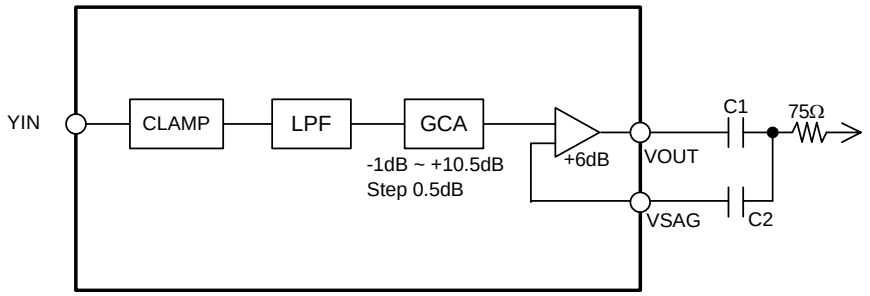
(AVDD=3.3V, SVDD=5.0V, DVOL=–8.0dB/0dB, SPKG1-0 bit = “10”,) * FS = Full Scale
Figure 39. Speaker-Amp Output Level Diagram



(AVDD=3.3V, SVDD=5.0V, DVOL=–8.0dB/0dB, SPKG1-0 bit = “11”,) * FS = Full Scale
Figure 40. Speaker-Amp Output Level Diagram

■ Video Block

Video-Amp has a drivability for a load resistance of 150Ω. The AK4632 has a composite input and output. A Low Pass Filter(LPF) and Gain Control Amp(GCA) are integrated and both DC output and Sag Compensation circuit are supported as shown in Figure 41 and Figure 42. The capacitance for Sag Compensation circuit is 100μ F+2.2μ F or 47μ F+1.0μ F. When DC output is used, VOUT pin and VSAG pin must be shorted. The output clamp voltage is 150mV(typ) at DC output. SAGC1-0 bits and VVDD voltage should be set as shown in Table 23. Table 25 shows the gain and step of the gain control. The gain is set by VGCA4-0 bits. PMV bit controls the power up and down of the video block. VOUT pin outputs AVSS level at PMV bit = "1".



(C1=100μ F, C2=2.2μ F) or (C1=47μ F, C2=1.0μ F)

Figure 41. Video block (using Sag Compensation circuit)

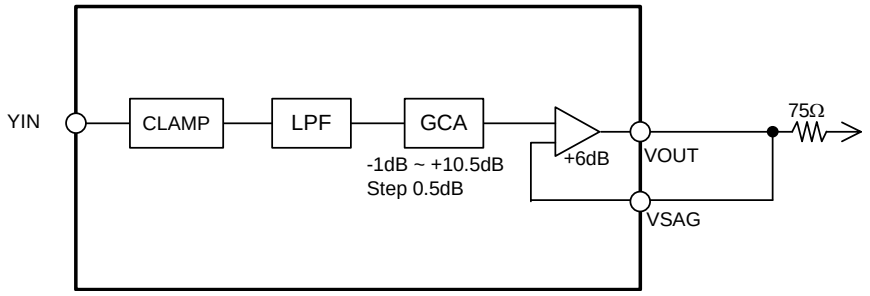


Figure 42. Video block (at DC Output))

SAGC1 bit	SAGC0 bit	VVDD voltage	Output Circuit	
0	0	2.8 V ≤ VVDD ≤ 3.6V	DC output	Default
0	1	Not Available		
1	0	2.85V ≤ VVDD < 4.75V	Sag compensation	
1	1	4.5 V ≤ VVDD < 5.25V	Sag compensation	

Table 23. Setting of VVDD and video output circuit.

Output Circuit		VVDD voltage	GCA setting
DC output		2.8 V ≤ VVDD ≤ 3.6V	0dB
Sag compensation	100μ F+2.2μ F	3.135 V ≤ VVDD ≤ 5.25V	0dB
		2.85V ≤ VVDD < 3.135 V	-1dB (Note)
Sag compensation	47μ F+1.0μ F	3.135 V ≤ VVDD ≤ 5.25V	0dB
		2.85V ≤ VVDD < 3.135 V	-1dB (Note)

Note : When the sag compensation circuit is used at less than 3.135V of VVDD, the GCA should be set to -1dB in order to avoid clipping of output video signal. Note that the video will become dark at that time.

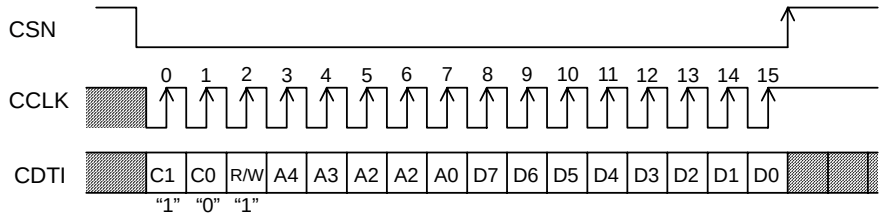
Table 24. Gain compensation

VGCA4-0 bits	GAIN(dB)	STEP	
17H	+10.5dB	0.5dB	
16H	+10.0dB		
15H	+9.5dB		
:	:		
04H	+1.0dB		
03H	+0.5dB		
02H	0.0dB		Default
01H	-0.5dB		
00H	-1.0dB		

Table 25. Setting of GCA

■ Serial Control Interface

Internal registers may be written by using the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of a 2-bit Chip address (Fixed to "10"), Read/Write (Fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. The clock speed of CCLK is 5MHz (max). The value of internal registers is initialized at PDN pin = "L".



C1-C0: Chip Address (C1 = "1", C0 = "0"); Fixed to "10"
R/W: READ/WRITE ("1": WRITE, "0": READ); Fixed to "1"
A4-A0: Register Address
D7-D0: Control data

Figure 43. Serial Control I/F Timing

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMVCM	PMBP	PMSPK	PMAO	PMDAC	PMMIC	PMADC
01H	Power Management 2	PMV	0	0	0	M/S	MCKPD	MCKO	PMPLL
02H	Signal Select 1	SPPS	BEEPS	ALC2S	DACA	DACM	MPWR	MICAD	MGAIN0
03H	Signal Select 2	0	AOPSN	MGAIN1	SPKG1	SPKG0	BEEPA	ALC1M	ALC1A
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO1	BCKO0	DIF1	DIF0
05H	Mode Control 2	0	0	FS3	MSBS	BCKP	FS2	FS1	FS0
06H	Timer Select	DVTM	ROTM	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
07H	ALC Mode Control 1	0	ALC2	ALC1	ZELM	LMAT1	LMAT0	RATT	LMTH
08H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
09H	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
0AH	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
0BH	ALC2 Mode Control	0	0	RFS5	RFS4	RFS3	RFS2	RFS1	RFS0
0CH	Video Mode Control	0	SAGC1	SAGC0	VGCA4	VGCA3	VGCA2	VGCA1	VGCA0

The PDN pin = “L” resets the registers to their default values.

Note: Unused bits must contain a “0” value.
Note: Only write to address 00H to 0CH.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMVCM	PMBP	PMSPK	PMAO	PMDAC	PMMIC	PMADC
Default		0	0	0	0	0	0	0	0

PMADC: ADC Block Power Control
0: Power down (Default)
1: Power up
When the PMADC bit changes from "0" to "1", the initialization cycle (1059/fs=133ms@8kHz) starts. After initializing, digital data of the ADC is output.

PMMIC: MIC In Block (MIC-Amp and ALC1) Power Control
0: Power down (Default)
1: Power up

PMDAC: DAC Block Power Control
0: Power down (Default)
1: Power up

PMAO: Mono Line Out Power Control
0: Power down (Default)
1: Power up

PMSPK: Speaker Block Power Control
0: Power down (Default)
1: Power up

PMBP: BEEP In Power Control
0: Power down (Default)
1: Power up
Even if PMBP bit is "0", the path is still connected between BEEP and AOUT/SPK-Amp. BEEPS and BEEPA bits should be set to "0" to disconnect these paths.

PMVCM: VCOM Block Power Control
0: Power down (Default)
1: Power up

Each block can be powered-down respectively by writing "0" in each bit. When the PDN pin is "L", all blocks are powered-down.

When PMPLL and MCKO bits and all bits in 00H address are "0", all blocks are powered-down. Though the IPGA resisters are initialized, the other registers remain unchanged. (refer to the IPGA6-0 bits description)

When any of the blocks are powered-up, the PMVCM bit must be set to "1". When PMPLL and MCKO bits and all bits in 00H address are "0", PMVCM bit can write to "0".

When BEEP signal is output from Speaker-Amp (Signal path: BEEP pin → SPP/SPN pins) or Mono Lineout-Amp (Signal path: BEEP pin → AOUT pin) only, the clocks may not be present. When ADC, DAC, ALC1 or ALC2 is in operation, the clocks must always be present.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	PMV	0	0	0	M/S	MCKPD	MCKO	PMPLL
Default		0	0	0	0	0	1	0	0

PMPLL: PLL Block Power Control Select
0: PLL is Power down and External is selected. (Default)
1: PLL is Power up and PLL Mode is selected.

MCKO: Master Clock Output Enable
0: "L" Output (Default)
1: 256fs Output

MCKPD: MCKI pin pull down control
0: Master Clock input enable
1: Pull down by 25kΩ (typ.) (Default)

M/S: Select Master / Slave Mode
0: Slave Mode (Default)
1: Master Mode

PMV: Video Block Power Control
0: Power down (Default)
1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select 1	SPPS	BEEPS	ALC2S	DACA	DACM	MPWR	MICAD	MGAIN0
Default		0	0	0	0	0	0	0	1

MGAIN1-0 : 1st MIC-amp Gain control(See Table 26)
MGAIN 1 bit is located at D6 bit of 03H

MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0dB	
0	1	+20dB	Default
1	0	+26dB	
1	1	+32dB	

Table 26. Input Gain

MICAD: Switch Control from MIC In to ADC.
0: OFF (Default)
1: ON
When MICAD bit is "1", the ALC1 output signal is input to ADC.

MPWR: Power Supply Control for Microphone
0: OFF (Default)
1: ON
When PMMIC bit is "1", MPWR bit is enabled.

DACM: Switch Control from DAC to mono amp.
0: OFF (Default)
1: ON
When PMSPK bit is "1", DACM bit is enabled. When PMSPK bit is "0", MOUT pin is Hi-Z state.

DACA: Switch Control from DAC to mono line amp
0: OFF (Default)
1: ON
When PMAO bit is "1", DACA bit is enabled. When PMAO bit is "0", the AOUT pin is AVSS.

ALC2S: ALC2 output to Speaker-Amp Enable
0: OFF (Default)
1: ON
When ALC2S bit is "1", the ALC2 output signal is input to Speaker-Amp.

BEEPS: BEEP pin to Speaker-Amp Enable
0: OFF (Default)
1: ON
When BEEPS bit is "1", the beep signal is input to Speaker-Amp.

SPPS: Speaker-amp Power-Save-Mode
0: Power Save Mode (Default)
1: Normal Operation
When SPPS bit is "1", the Speaker-amp is in power-save-mode and the SPP pin becomes Hi-z and SPN pin is set to SVDD/2 voltage. When the PMSPK bit = "1", this bit is valid. After the PDN pin changes from "L" to "H", the PMSPK bit is "0", which powers down Speaker-amp.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	0	0	MGAIN1	SPKG1	SPKG0	BEEPA	ALC1M	ALC1A
Default		0	0	0	0	0	0	0	0

ALC1A: Switch Control from ALC1 output signal to mono line output amp.
0: OFF (Default)
1: ON
When PMAO bit is "1", ALC1A bit is enabled. When PMAO bit is "0", the AOUT pin is AVSS.

ALC1M: Switch Control from ALC1 output signal to mono amp.
0: OFF (Default)
1: ON
When PMSPK bit is "1", ALC1M is enabled. When PMSPK bit is "0", the MOUT pin goes Hi-Z state.

BEEPA: Switch Control from beep signal to mono line output amp.
0: OFF (Default)
1: ON
When PMAO bit is "1", BEEPA is enabled. When PMAO bit is "0", the AOUT pin is AVSS.

SPKG1-0: Select Speaker-Amp Output Gain (See Table 27)

SPKG1-0 bits	Gain
00	0dB
01	+2.2dB
10	+4.4dB
11	+8.7dB

Table 27. Gain of Speaker-Amp

MGAIN1: Mic-Amplifier Gain Control(See Table 26)

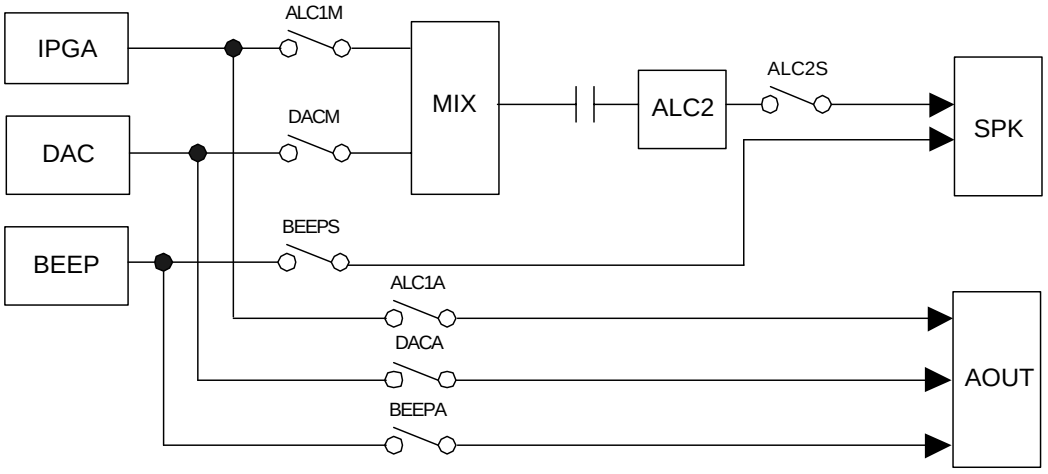


Figure 44. Speaker and Mono Lineout-Amps switch control

AOPSN: Mono Line Output Power-Save Mode

0: Normal Operation

1: Power-Save Mode (Default)

Power-save mode is enable at AOPSN bit = "1". POP noise at power-up/down can be reduced by changing at AOPSN bit = "1". (See Figure 34)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO1	BCKO0	DIF1	DIF0
Default		0	0	0	0	0	0	1	0

DIF1-0: Audio Interface Format (See Table 28)

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	DSP Mode	DSP Mode	≥ 16fs	See Table 34	
1	0	1	MSB justified	LSB justified	≥ 32fs	Figure 27	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 28	Default
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 29	

Table 28. Audio Interface Format

BCKO1-0: Select BICK output frequency at Master Mode (See Table 29)

Mode	BCKO1 bit	BCKO0 bit	BICK Output Frequency	
0	0	0	16fs	Default
1	0	1	32fs	
2	1	0	64fs	
3	1	1	N/A	

Table 29. BICK Output Frequency at Master Mode

PLL3-0: Select input frequency at PLL mode (See Table 30)

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	
0	0	0	0	0	FCK pin	1fs	Default
1	0	0	0	1	BICK pin	16fs	
2	0	0	1	0	BICK pin	32fs	
3	0	0	1	1	BICK pin	64fs	
4	0	1	0	0	MCKI pin	11.2896MHz	
5	0	1	0	1	MCKI pin	12.288MHz	
6	0	1	1	0	MCKI pin	12MHz	
7	0	1	1	1	MCKI pin	24MHz	
12	1	1	0	0	MCKI pin	13.5MHz	
13	1	1	0	1	MCKI pin	27MHz	
Others	Others				N/A		

Table 30. Setting of PLL Mode (*fs: Sampling Frequency)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 2	0	0	FS3	MSBS	BCKP	FS2	FS1	FS0
Default		0	0	0	0	0	0	0	0

FS3-0: Setting of Sampling Frequency (See Table 31 and Table 32) and MCKI Frequency (See Table 33)
These bits are selected to sampling frequency at PLL mode and MCKI frequency at EXT mode.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	Default
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
4	0	1	0	0	7.35kHz	
5	0	1	0	1	11.025kHz	
6	0	1	1	0	14.7kHz	
7	0	1	1	1	22.05kHz	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
14	1	1	1	0	29.4kHz	
15	1	1	1	1	44.1kHz	
Others	Others				N/A	

Table 31. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1"

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	Don't care	0	0	7.35kHz ≤ fs ≤ 8kHz	Default
1	0	Don't care	0	1	8kHz < fs ≤ 12kHz	
2	0	Don't care	1	0	12kHz < fs ≤ 16kHz	
3	0	Don't care	1	1	16kHz < fs ≤ 24kHz	
6	1	Don't care	1	0	24kHz < fs ≤ 32kHz	
7	1	Don't care	1	1	32kHz < fs ≤ 48kHz	
Others	Others				N/A	

Table 32. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL bit = "1"

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	Don't care	0	0	256fs	7.35kHz ≤ fs ≤ 48kHz	Default
1	Don't care	0	1	1024fs	7.35kHz < fs ≤ 13kHz	
2	Don't care	1	0	256fs	7.35kHz < fs ≤ 48kHz	
3	Don't care	1	1	512fs	7.35kHz < fs ≤ 26kHz	

Table 33. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

BCKP, MSBS: "00" (Default) (See Table 34)

MSBS bit	BCKP bit	Audio Interface Format	
0	0	Figure 23	Default
0	1	Figure 24	
1	0	Figure 25	
1	1	Figure 26	

Table 34. Audio Interface Format in Mode 0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Timer Select	DVTM	ROTM	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
Default		0	0	0	0	0	0	0	0

LTM1-0: ALC1 limiter operation period at zero crossing disable (ZELM bit = "1") (See Table 35)

The IPGA value is changed immediately. When the IPGA value is changed continuously, the change is done by the period specified by the LTM1-0 bits. Default is "00" (0.5/fs).

LTM1 bit	LTM0 bit		ALC1 Limiter Operation Period		
			8kHz	16kHz	
0	0	0.5/fs	63μs	31μs	Default
0	1	1/fs	125μs	63μs	
1	0	2/fs	250μs	125μs	
1	1	4/fs	500μs	250μs	

Table 35. ALC1 Limiter Operation Period at zero crossing disable (ZELM bit="1")

WTM1-0: ALC1 Recovery Waiting Period (See Table 36)

A period of recovery operation when any limiter operation does not occur during the ALC1 operation. Default is "00" (128/fs).

WTM1 bit	WTM0 bit		ALC1 Recovery Operation Waiting Period		
			8kHz	16kHz	
0	0	128/fs	16ms	8ms	Default
0	1	256/fs	32ms	16ms	
1	0	512/fs	64ms	32ms	
1	1	1024/fs	128ms	64ms	

Table 36. ALC1 Recovery Operation Waiting Period

ZTM1-0: ALC1 Zero crossing timeout Period (See Table 37)

When the IPGA perform zero crossing or timeout, the IPGA value is changed by the μP WRITE operation, ALC1 recovery operation or ALC1 limiter operation (ZELM bit = "0"). Default is "00" (128/fs).

ZTM1 bit	ZTM0 bit		Zero Crossing Timeout Period		
			8kHz	16kHz	
0	0	128/fs	16ms	8ms	Default
0	1	256/fs	32ms	16ms	
1	0	512/fs	64ms	32ms	
1	1	1024/fs	128ms	64ms	

Table 37. Zero Crossing Timeout Period

ROTM: Period time for ALC2 Recovery operation, ALC2 Zero Crossing Timeout and ALC2 initializing cycle.

0: 512/fs (Default)

1: 1024/fs

The ROTM bit is set during the PMSPK bit = "0".

DVTM : Digital Volume Soft Transition Time Control

0: 1061/fs (Default)

1: 256/fs

This is the time to FFH from 00H of DVOL7-0 bits.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	ALC Mode Control 1	0	ALC2	ALC1	ZELM	LMAT1	LMAT0	RATT	LMTH
Default		0	1	0	0	0	0	0	0

LMTH: ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level (See Table 38)

The ALC1 limiter detection level and the ALC1 recovery counter reset level may be offset by about ±2dB. Default is "0".

LMTH bit	ALC1 Limiter Detection Level	ALC1 Recovery Waiting Counter Reset Level	
0	ADC Input ≥ –6.0dBFS	–6.0dBFS > ADC Input ≥ –8.0dBFS	Default
1	ADC Input ≥ –4.0dBFS	–4.0dBFS > ADC Input ≥ –6.0dBFS	

Table 38. ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level

RATT: ALC1 Recovery GAIN Step (See Table 39)

During the ALC1 recovery operation, the number of steps changed from the current IPGA value is set. For example, when the current IPGA value is 30H and RATT bit = "1" is set, the IPGA changes to 32H by the ALC1 recovery operation and the output signal level is gained up by 1dB (=0.5dB x 2). When the IPGA value exceeds the reference level (REF6-0 bits), the IPGA value does not increase.

RATT bit	GAIN STEP	
0	1	Default
1	2	

Table 39. ALC1 Recovery Gain Step Setting

LMAT1-0: ALC1 Limiter ATT Step (See Table 40)

During the ALC1 limiter operation, when IPGA output signal exceeds the ALC1 limiter detection level set by LMTH, the number of steps attenuated from the current IPGA value is set. For example, when the current IPGA value is 47H and the LMAT1-0 bits = "11", the IPGA transition to 43H when the ALC1 limiter operation starts, resulting in the input signal level being attenuated by 2dB (=0.5dB x 4). When the attenuation value exceeds IPGA = "00" (–8dB), it clips to "00".

LMAT1 bit	LMAT0 bit	ATT STEP	
0	0	1	Default
0	1	2	
1	0	3	
1	1	4	

Table 40. ALC1 Limiter ATT Step Setting

ZELM: Enable zero crossing detection at ALC1 Limiter operation

0: Enable (Default)

1: Disable

When the ZELM bit = "0", the IPGA of each L/R channel perform a zero crossing or timeout independently and the IPGA value is changed by the ALC1 operation. The zero crossing timeout is the same as the ALC1 recovery operation. When the ZELM bit = "1", the IPGA value is changed immediately.

ALC1: ALC1 Enable
0: ALC1 Disable (Default)
1: ALC1 Enable
When ALC1 bit is "1", the ALC1 operation is enabled.

ALC2: ALC2 Enable
0: ALC2 Disable
1: ALC2 Enable (Default)
After completing the initializing cycle (512/fs = 64ms @fs=8kHz at ROTM bit = "0"), the ALC2 operation is enabled. When the PMSPK bit changes from "0" to "1" or PDN pin changes from "L" to "H", the initilization cycle starts.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
Default		0	0	1	1	0	1	1	0

REF6-0: Reference value at ALC1 Recovery Operation (See Table 41)
During the ALC1 recovery operation, if the IPGA value exceeds the setting reference value by gain operation, then the IPGA does not become larger than the reference value. For example, when REF7-0 = "30H", RATT = 2step, IPGA = 2FH, even if the input signal does not exceed the "ALC1 Recovery Waiting Counter Reset Level", the IPGA does not change to 2FH + 2step = 31H, and keeps 30H. Default is "36H".

DATA (HEX)	GAIN (dB)	STEP	
47	+27.5	0.5dB	
46	+27.0		
45	+26.5		
:	:		
36	+19.0		Default
:	:		
10	+0.0		
:	:		
06	−5.0		
05	−5.5		
04	−6.0		
03	−6.5		
02	−7.0		
01	−7.5		
00	−8.0		

Table 41. Setting Reference Value at ALC1 Recovery Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
Default		0	0	0	1	0	0	0	0

IPGA6-0: Input Analog PGA (See Table 42)

Default: "10H" (0dB)

When IPGA gain is changed, IPGA6-0 bits should be written while PMMIC bit is "1" and ALC1 bit is "0". IPGA6-0 bits should be set at 2/fs(250μs@fs=8kHz) after PMMIC bit is set to "1". IPGA gain is reset when PMMIC bit is "0", and then IPGA operation starts from the default value when PMMIC bit is changed to "1". When ALC1 bit is changed from "1" to "0", IPGA holds the last gain value set automatically by ALC1 operation.

In a manual mode, IPGA can be set to any values in Table 42.The ZTM1-0 bits set zero crossing timeout period when IPGA value is changed. When the control register is written from the μP, the zero crossing counter is reset and its counter starts. When the signal zero crossing or zero crossing timeout, the written value from the μP becomes valid.

DATA (HEX)	GAIN (dB)	STEP	
47	+27.5	0.5dB	
46	+27.0		
45	+26.5		
:	:		
36	+19.0		
:	:		
10	+0.0		Default
:	:		
06	–5.0		
05	–5.5		
04	–6.0		
03	–6.5		
02	–7.0		
01	–7.5		
00	–8.0		

Table 42. Input Gain Setting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
Default		0	0	0	1	1	0	0	0

DVOL7-0: Output Digital Volume (See Table 43)

The AK4632 has a digital output volume (256 levels, 0.5dB step, Mute). The gain can be set by the DVOL7-0 bits. The volume is included in front of a DAC block, a input data of DAC is changed from +12 to –115dB with MUTE. This volume has a soft transition function. It takes 1061/fs (=133ms @ fs = 8kHz) or 256/fs (=32ms @ fs = 8kHz) from 00H to FFH. Soft Transition Time is set by DVTM bit.

DVOL7-0	Gain	
00H	+12.0dB	
01H	+11.5dB	
02H	+11.0dB	
•	•	
18H	0dB	Default
•	•	
FDH	–114.5dB	
FEH	–115.0dB	
FFH	MUTE (–∞)	

Table 43. Digital Volume Code Table

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC2 Mode Control	0	0	RFS5	RFS4	RFS3	RFS2	RFS1	RFS0
Default		0	0	1	1	1	1	0	0

RFS6-0: Reference value at ALC2 Recovery Operation (See Table 44)

REFS5-0 bits	Volume[dB]	Step	
3F	+19.5	0.5dB	
3E	+19.0		
3D	+18.5		
3C	+18.0		Default
:	:		
19	+0.5		
18	+0.0		
17	-0.5		
:	:		
03	-10.5		
02	-11.0		
01	-11.5		
00	-12.0		

Table 44. Setting Reference Value at ALC2 Recovery Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Video Mode Control	0	SAGC1	SAGC0	VGCA4	VGCA3	VGCA2	VGCA1	VGCA0
Default		0	0	0	0	0	0	1	0

VGCA4-0: Gain Control of Video output(See Table 25)

SAGC1-0: Select Video Output Circuit (See Table 23)

SYSTEM DESIGN

Figure 45 shows the system connection diagram. An evaluation board [AKD4632] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

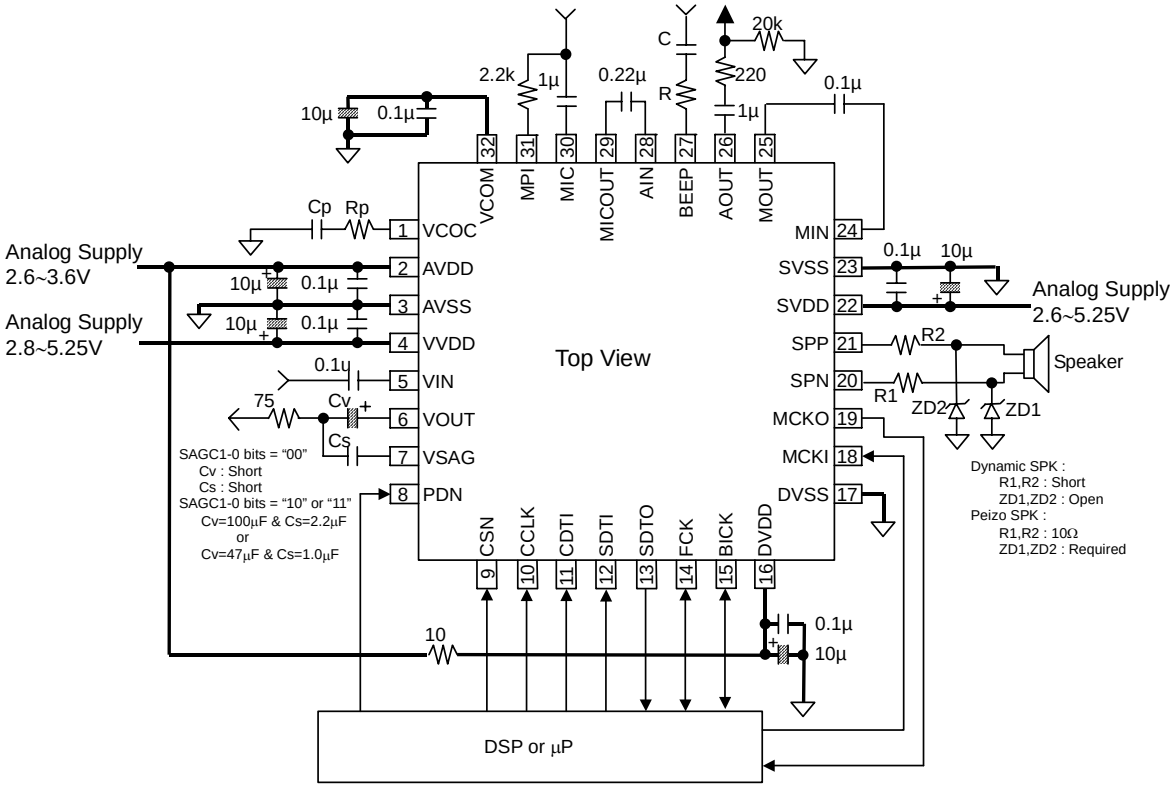


Figure 45. Typical Connection Diagram

Notes:

- AVSS, DVSS and SVSS of the AK4632 should be distributed separately from the ground of external controllers.
- The exposed pad on the bottom surface of the package must be open.
- All digital input pins except pull-down pin should not be left floating.
- Value of R and C of BEEP pin should depend on system.
- When the AK4632 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of VCOC pin is not needed.
- When the AK4632 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of VCOC pin is shown in Table 45.
- Input resistance of AIN pin and Capacitance between MICOUT pin and AIN pin compose of HPF. When the capacitance is 0.22µF, the cut off frequency is typ.72Hz(typ)(min. 48Hz, max. 145Hz).

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	Rp and Cp of VCOC pin		PLL Lock Time (max)	
							Rp[Ω]	Cp[F]		
0	0	0	0	0	FCK pin	1fs	6.8k	220n	160ms	Default
1	0	0	0	1	BICK pin	16fs	10k	4.7n	2ms	
2	0	0	1	0	BICK pin	32fs	10k	4.7n	2ms	
3	0	0	1	1	BICK pin	64fs	10k	4.7n	2ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10k	4.7n	40ms	
5	0	1	0	1	MCKI pin	12.288MHz	10k	4.7n	40ms	
6	0	1	1	0	MCKI pin	12MHz	10k	4.7n	40ms	
7	0	1	1	1	MCKI pin	24MHz	10k	4.7n	40ms	
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	40ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	40ms	
Others	Others				N/A					

Table 45. Setting of PLL Mode (*fs: Sampling Frequency)

1. Grounding and Power Supply Decoupling

The AK4632 requires careful attention to power supply and grounding arrangements. AVDD, DVDD, SVDD and VVDD are usually supplied from the system's analog supply. If AVDD, DVDD, SVDD and VVDD are supplied separately, the correct power up sequence should be observed. AVSS, DVSS and SVSS of the AK4632 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4632 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4632.

3. Analog Inputs

The Mic and Beep inputs are single-ended. The input signal range scales with nominally at 0.06 x AVDD Vpp for the Mic input and 0.6 x AVDD Vpp for the Beep input, centered around the internal common voltage (approx. 0.45 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is $fc = (1/2\pi RC)$. The AK4632 can accept input voltages from AVSS to AVDD.

4. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). Mono output from the MOUT pin and Mono Line Output from the AOUT pin are centered at 0.45 x AVDD (typ). The Speaker-Amp output is centered at SVDD/2.

CONTROL SEQUENCE

■ Clock Set up

When ADC, DAC, ALC1, ALC2 and IPGA are used, the clocks must be supplied.

1. In case of PLL Master Mode.

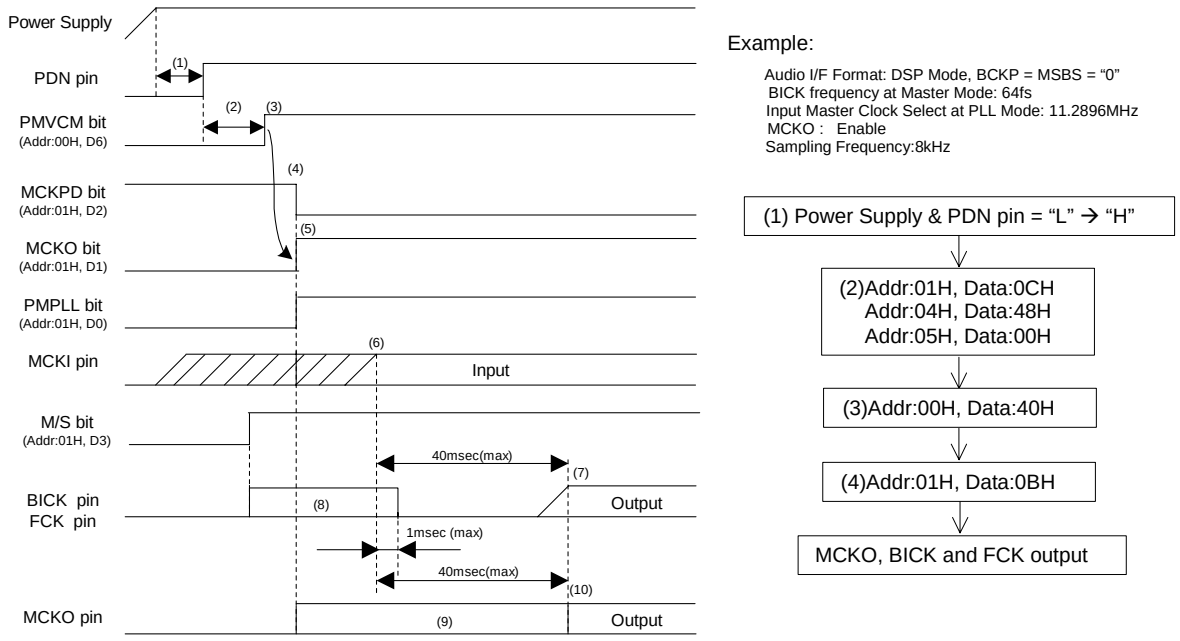


Figure 46. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin = "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4632.
(2) DIF1-0, PLL3-0, FS3-0, BCKO1-0, MSBS, BCKP and M/S bits should be set during this period.
(3) Power UpVCOM: PMVCM bit = "0" → "1"
VCOM should first be powered-up before the other block operates.
(4) Release the pull-down resistor of the MCKI pin: MCKPD bit = "1" → "0"
(5) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"
(6) PLL lock time is 40ms(max) after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source.
(7) The AK4632 starts to output the FCK and BICK clocks after the PLL becomes stable. The normal operation of the block which a clock is necessary for becomes possible.
(8) The invalid frequencies are output from FCK and BICK pins during this period.
(9) The invalid frequency is output from MCKO pin during this period.
(10) The normal clock is output from MCKO pin after the PLL is locked.

2. When the external clocks (FCK or BICK pin) are used in PLL Slave Mode.

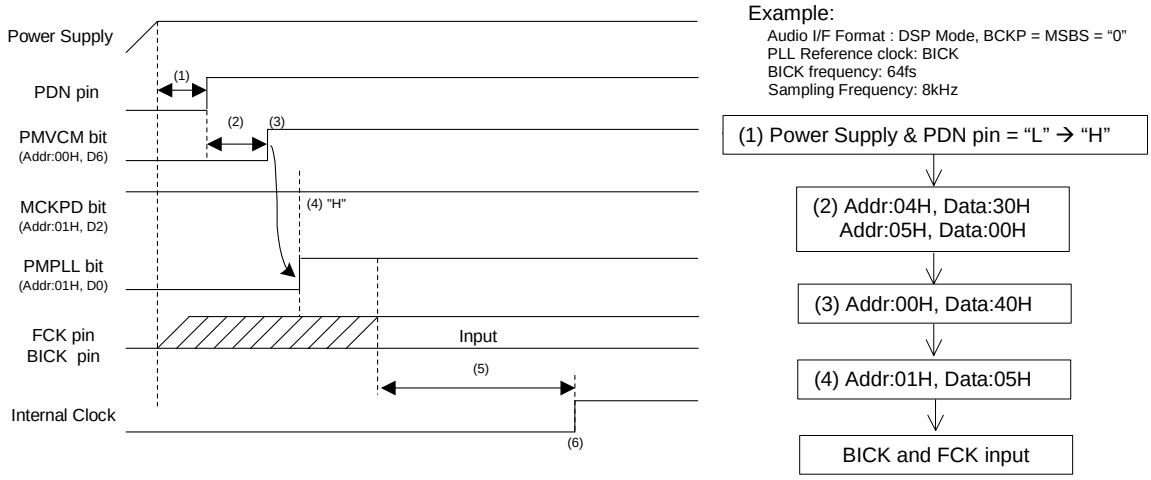


Figure 47. Clock Set Up Sequence (2)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4632.

(2) DIF1-0, FS3-0, PLL3-0, MSBS and BCKP bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) Pull down of the MCKI pin: MCKPD bit = "1"

(5) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (FCK or BICK pin) is supplied. PLL lock time is 160ms(max) when FCK is a PLL reference clock. And PLL lock time is 2ms(max) when BICK is a PLL reference clock.

(6) Normal operation stats after the PLL is locked.

3. When the external clock (MCKI pin) is used in PLL Slave Mode.

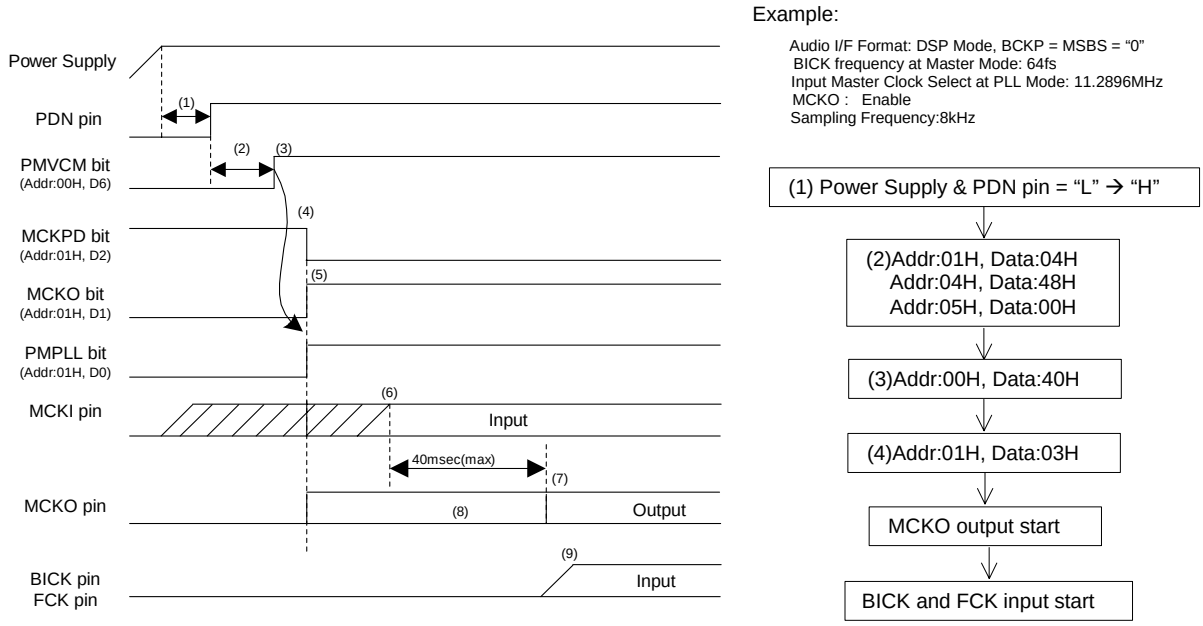


Figure 48. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4632.
(2) DIF1-0, PLL3-0, FS3-0, BCKO1-0, MSBS, BCKP and M/S bits should be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
(4) Release the pull-down resistor of the MCKI pin: MCKPD bit = "1" → "0"
(5) Enable MCKO output: MCKO bit = "1"
(6) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied. PLL lock time is 40ms(max).
(7) The normal clock is output from MCKO after PLL is locked.
(8) The invalid frequency is output from MCKO during this period.
(9) BICK and FCK clocks should be synchronized with MCKO clock.

4. EXT Slave Mode

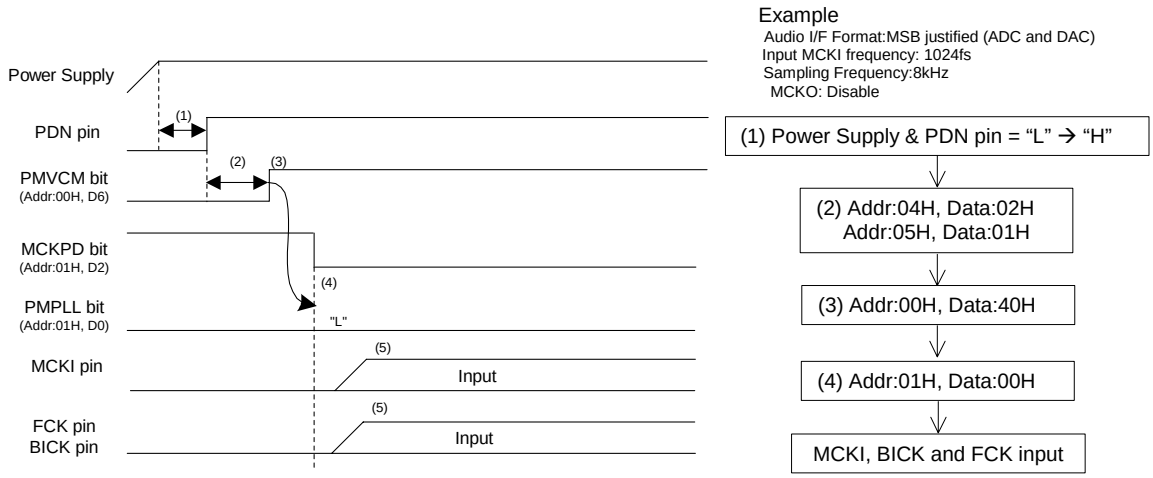


Figure 49. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4632.

(2) DIF1-0 and FS1-0 bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) Release the pull-down resistor of the MCKI pin: MCKPD bit = "1" → "0"
Power down PLL: PMPLL bit = "0"

(5) Normal operation starts after the MCKI, FCK and BICK are supplied.

■ MIC Input Recording

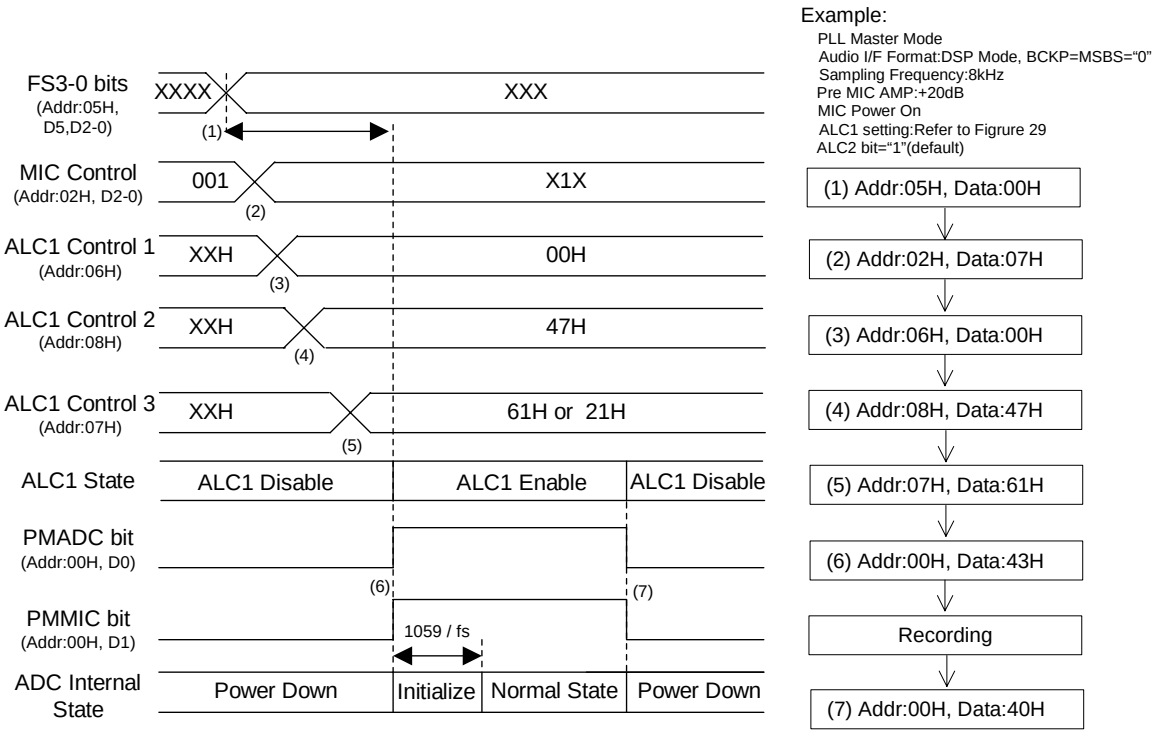


Figure 50. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at s=8kHz. If the parameter of the ALC1 is changed, please refer to "Figure 31. Registers set-up sequence at the ALC1 operation"

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bit). When the AK4632 is PLL mode, MIC and ADC should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up MIC input (Addr: 02H)

(3) Set up Timer Select for ALC1 (Addr: 06H)

(4) Set up REF value for ALC1 (Addr: 08H)

(5) Set up LMTH, RATT, LMAT1-0 and ALC1 bits (Addr: 07H)

(6) Power Up MIC and ADC: PMMIC bit = PMADC bit = "0" → "1"
The initialization cycle time of ADC is 1059/fs=133ms@fs=8kHz.
After the ALC1 bit is set to "1" and MIC block is powered-up, the ALC1 operation starts from IPGA default value (0dB).

(7) Power Down MIC and ADC: PMMIC bit = PMADC bit = "1" → "0"
When the registers for the ALC1 operation are not changed, ALC1 bit may be keeping "1". The ALC1 operation is disabled because the MIC block is powered-down. If the registers for the ALC1 operation are also changed when the sampling frequency is changed, it should be done after the AK4632 goes to the manual mode (ALC1 bit = "0") or MIC block is powered-down (PMMIC bit = "0"). IPGA gain is reset when PMMIC bit is "0", and then IPGA operation starts from the default value when PMMIC bit is changed to "1".

■ Speaker-amp Output

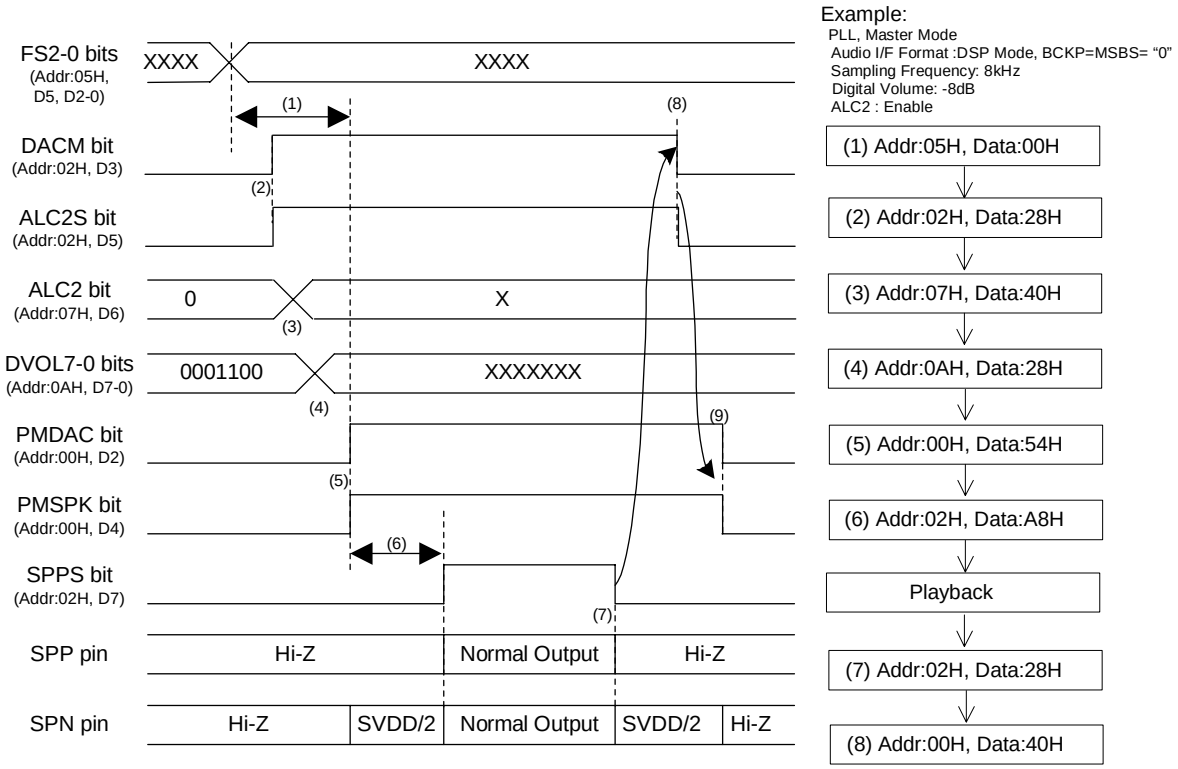


Figure 51. Speaker-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4632 is PLL mode, DAC and Speaker-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up the path of "DAC → SPK-Amp"
DACM = ALC2S bit: "0" → "1"

(3) Set up the ALC2 Enable/Disable

(4) Set up the digital volume (Addr: 0AH)
After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.

(5) Power Up of DAC and Speaker-Amp: PMDAC bit = PMSPK bit = "0" → "1"
When ALC2 bit = "1", the ALC2 is disabled (ALC2 gain is fiexed to "–2dB") during the initilization cycle (512/fs = 64ms @ fs=8kHz, ROTM bit = "0") and the ALC2 starts from "–2dB" after completing the initilization cycle.

(6) Exit the power-save-mode of Speaker-Amp: SPPS bit = "0" → "1"
"(6)" time depends on the time constant of input impedance of MIN pin and capacitor between MIN pin and MOUT pin. If Speaker-Amp output is enabled before MIN-Amp (ALC2) becomes stable, pop noise may occur.
e.g. Input Impedance of MIN pin =36kΩ (max), C=0.1μF: Recommended wait time is more than 5τ = 18ms.

(7) Enter the power-save-mode of Speaker-Amp: SPPS bit = "1" → "0"

(8) Disable the path of "DAC → SPK-Amp"
DACM = ALC2S bit: "1" → "0"

(9) Power Down DAC and Speaker-Amp: PMDAC bit = PMSPK bit = "1" → "0"

■ BEEP signal output from Speaker-Amp

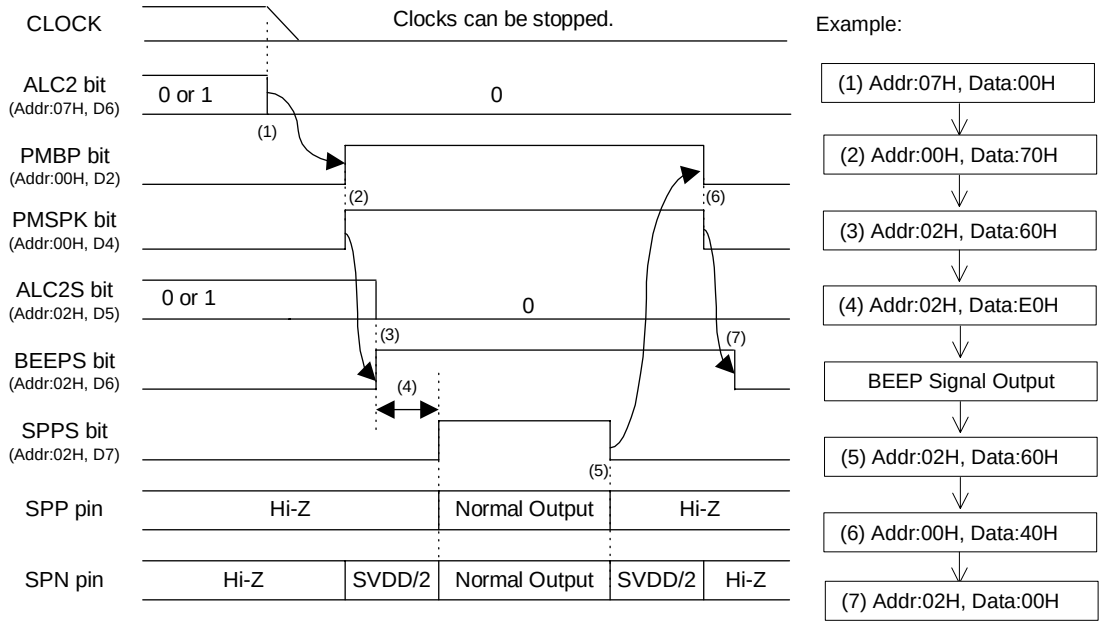


Figure 52. "BEPP-Amp → Speaker-Amp" Output Sequence

<Example>

The clocks can be stopped when only BEEP-Amp and Speaker-Amp are operating. However ALC2 must be disabled.

(1) ALC2 Disable: ALC2 bit = "0"
(2) Power Up BEEP-Amp and Speaker-Amp: PMBP bit = PMSPK bit = "0" → "1"
(3) Disable the path of "ALC2 → SPK-Amp": ALC2S bit = "0"
Enable the path of "BEEP → SPK-Amp": BEEPS bit = "0" → "1"
(4) Exit the power-save-mode of Speaker-Amp: SPPS bit = "0" → "1"
"(4)" time depends on the time constant of external resistor and capacitor connected to BEEP pin. If Speaker-Amp output is enabled before input of BEEP-Amp becomes stable, pop noise may occur.
e.g. R=20k, C=0.1μF: Recommended wait time is more than 5τ = 10ms.
(5) Enter the power-save-mode of Speaker-Amp: SPPS bit = "1" → "0"
(6) Power Down BEEP-Amp and Speaker-Amp: PMBP bit = PMSPK bit = "1" → "0"
(7) Disable the path of "BEEP → SPK-Amp": BEEPS bit = "1" → "0"

■ MONO LINEOUT

1. In case of using an external mute circuit.(Compatible with AK4536/AK4630)

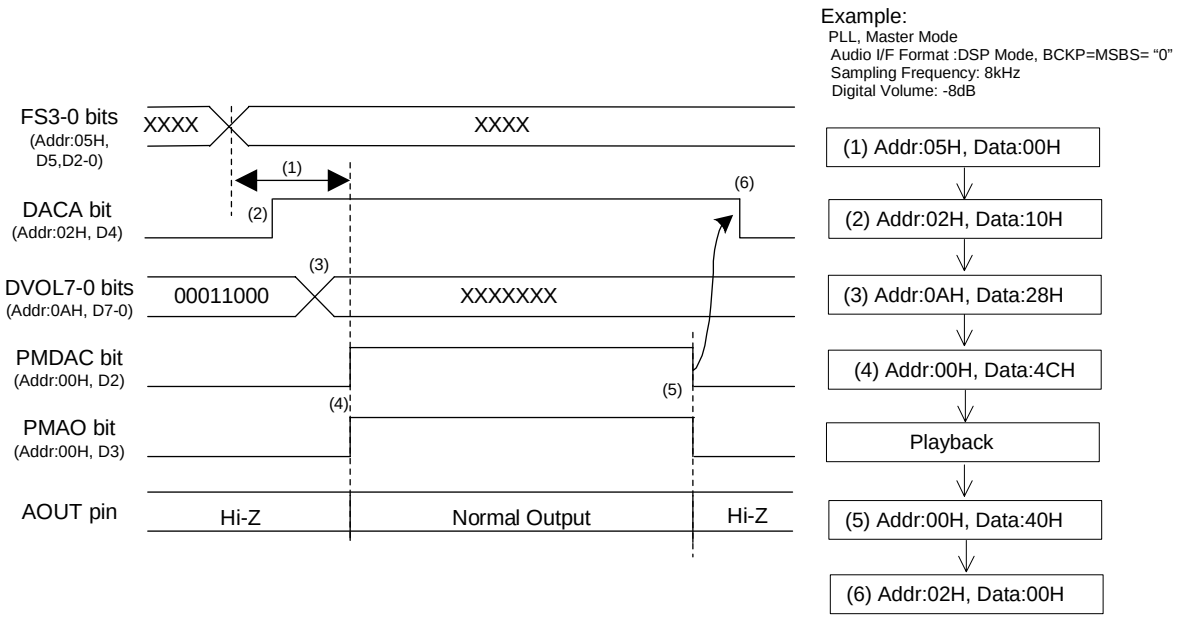


Figure 53. Mono Lineout Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4632 is PLL mode, DAC and Mono Line Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up the path of "DAC → Mono Line Amp"
DACA bit: "0" → "1"

(3) Set up the digital volume (Addr: 0AH)
After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.

(4) Power Up of DAC and Mono Line Amp: PMDAC bit = PMAO bit = "0" → "1"
When DAC and Mono Line Amp are powered-up, the pop noise occurs from AOUT pin. Therefore AOUT pin should be muted by external circuit.

(5) Power Down of DAC and Mono Line Amp: PMDAC bit = PMAO bit = "1" → "0"
When DAC and Mono Line Amp are powered-down, the pop noise occurs from AOUT pin. Therefore AOUT pin should be muted by external circuit.

(6) Disable the path of "DAC → Mono Line Amp"
DACA bit: "1" → "0"

2. In case of using POP reduction circuit of AK4632.

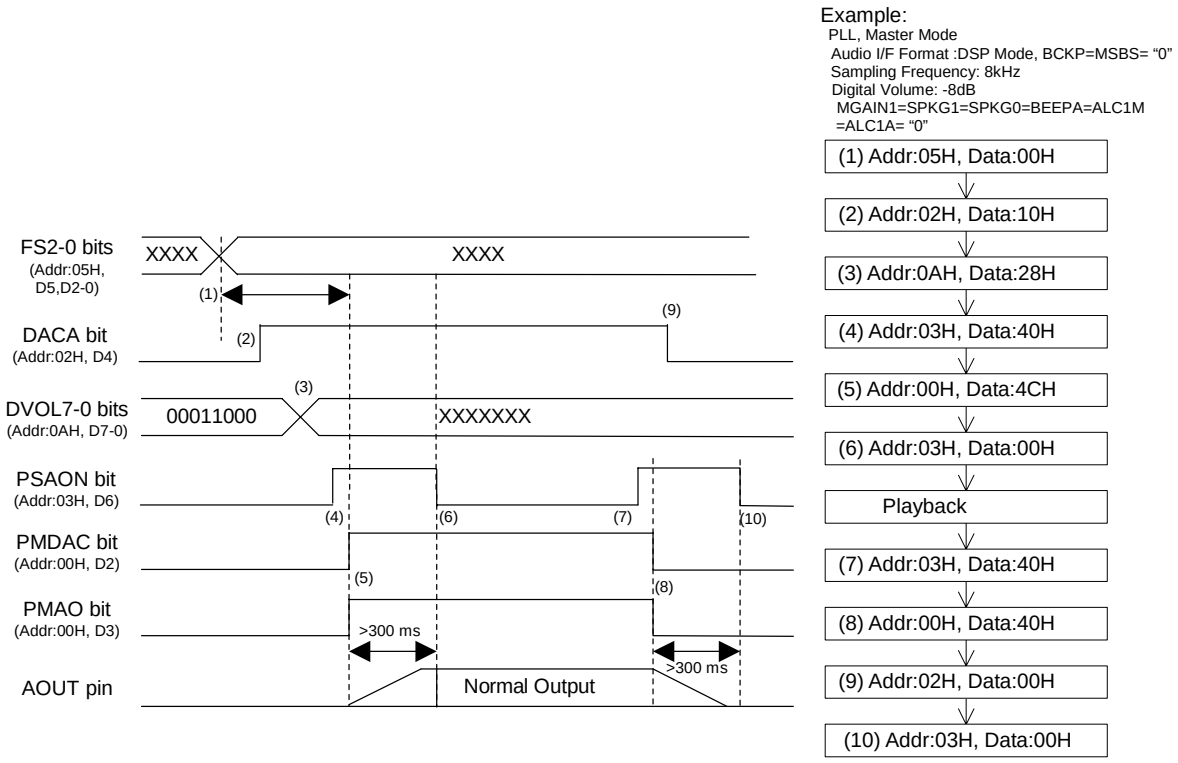


Figure 54. Mono Lineout Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4632 is PLL mode, DAC and Mono Line Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up the path of "DAC → Mono Line Amp" : DACA bit: "0" → "1"

(3) Set up the digital volume (Addr: 0AH)
After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.

(4) Enter power-save mode of Mono Line Amp: AOPSN bit = "0" → "1"

(5) Power Up of DAC and Mono Line Amp: PMDAC bit = PMAO bit = "0" → "1"
AOUT pin rises up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF.

(6) Exit power-save mode of Mono Line Amp after AOUT pin rises up. : AOPSN bit = "1" → "0"
Mono Line Amp goes to normal operation.

(7) Enter power-save mode of Mono Line Amp: AOPSN bit = "0" → "1"

(8) Power Down of DAC and Mono Line Amp: PMDAC bit = PMAO bit = "1" → "0"
AOUT pin falls down to AVSS. Fall time is 200ms (max 300ms) at C=1μF.

(9) Disable the path of "DAC → Mono Line Amp" : DACA bit: "1" → "0"

(10) Exit power-save mode of Mono Line Amp after AOUT pin falls down. : AOPSN bit = "1" → "0"

■ Video Signal Input and Output

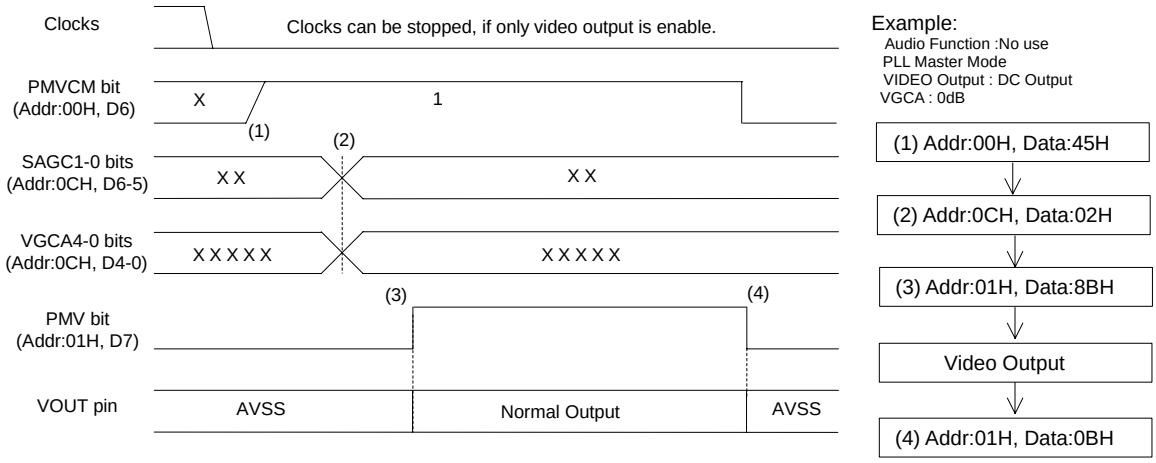


Figure 55. Video Output Sequence

<Example>

When the only video function is used, the clocks are not needed to input.

(1) Power Up of VCOM : PMVCM bit = "0" → "1"

(2) Set up the output circuit(SAGC1-0bits) and GCA(VGCA4-0 bits)

(3) Power Up of Video-Amp : PMV bit = "0" → "1"

The video signal that is input to VIN pin starts output from VOUT pin.

(4) Power Down of Video-Amp : PMV bit = "1" → "0"

The output from VOUT pin stops. VOUT pin goes to AVSS.

If any audio functions are not used, VCOM can be powered-down(PMVCM bit ="0")

■ Stop of Clock

Master clock can be stopped when ADC, DAC, ALC1, ALC2 and IPGA don't operate.

1. In case of PLL Master Mode

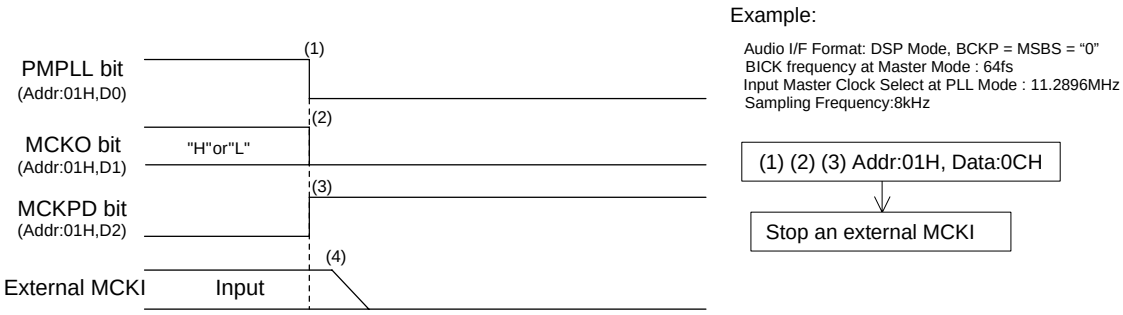


Figure 56. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Pull down the MCKI pin: MCKPD bit = "0" → "1"
When the external master clock becomes Hi-Z, MCKI pin should be pulled down.
(4) Stop an external master clock.

2. When an external clocks (FCK or BICK pins) are used in PLL Slave Mode.

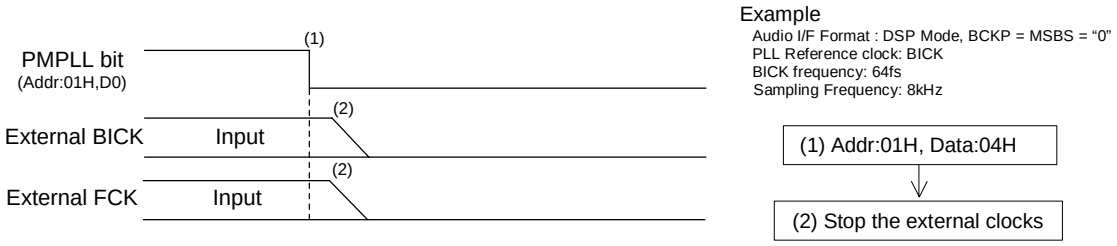


Figure 57. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external BICK and FCK clocks

3. When an external clock (MCKI pin) is used in PLL Slave Mode.

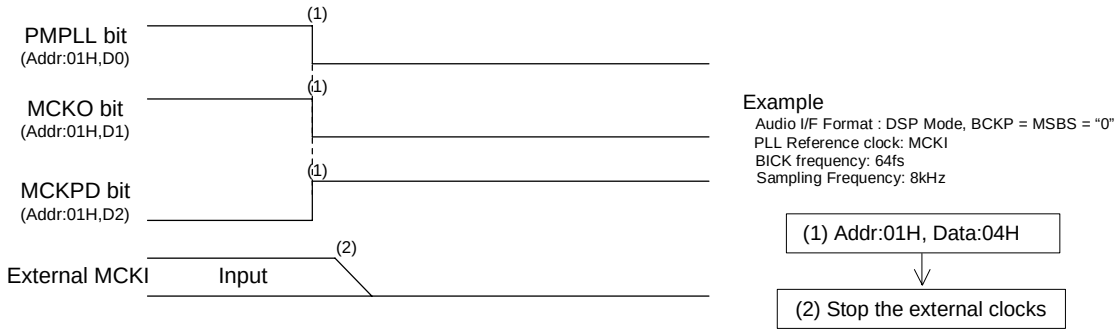


Figure 58. Clock Stopping Sequence (3)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
Stop MCKO output: MCKO bit = "1" → "0"
Pull down the MCKI pin: MCKPD bit = "0" → "1"
When the external master clock becomes Hi-Z, MCKI pin should be pulled down.
(2) Stop the external master clock.

4. EXT Slave Mode

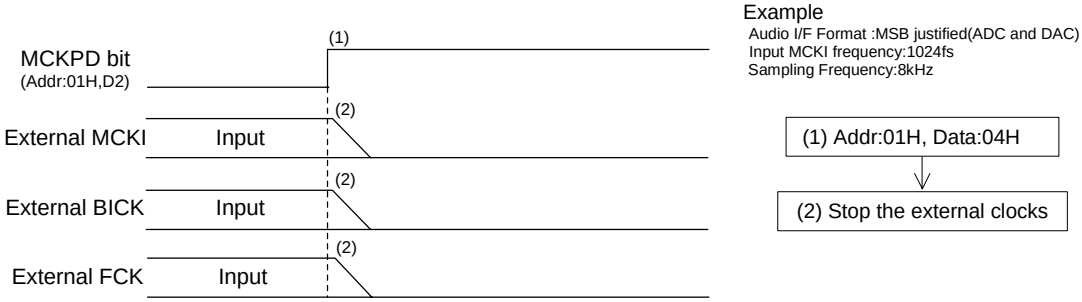


Figure 59. Clock Stopping Sequence (4)

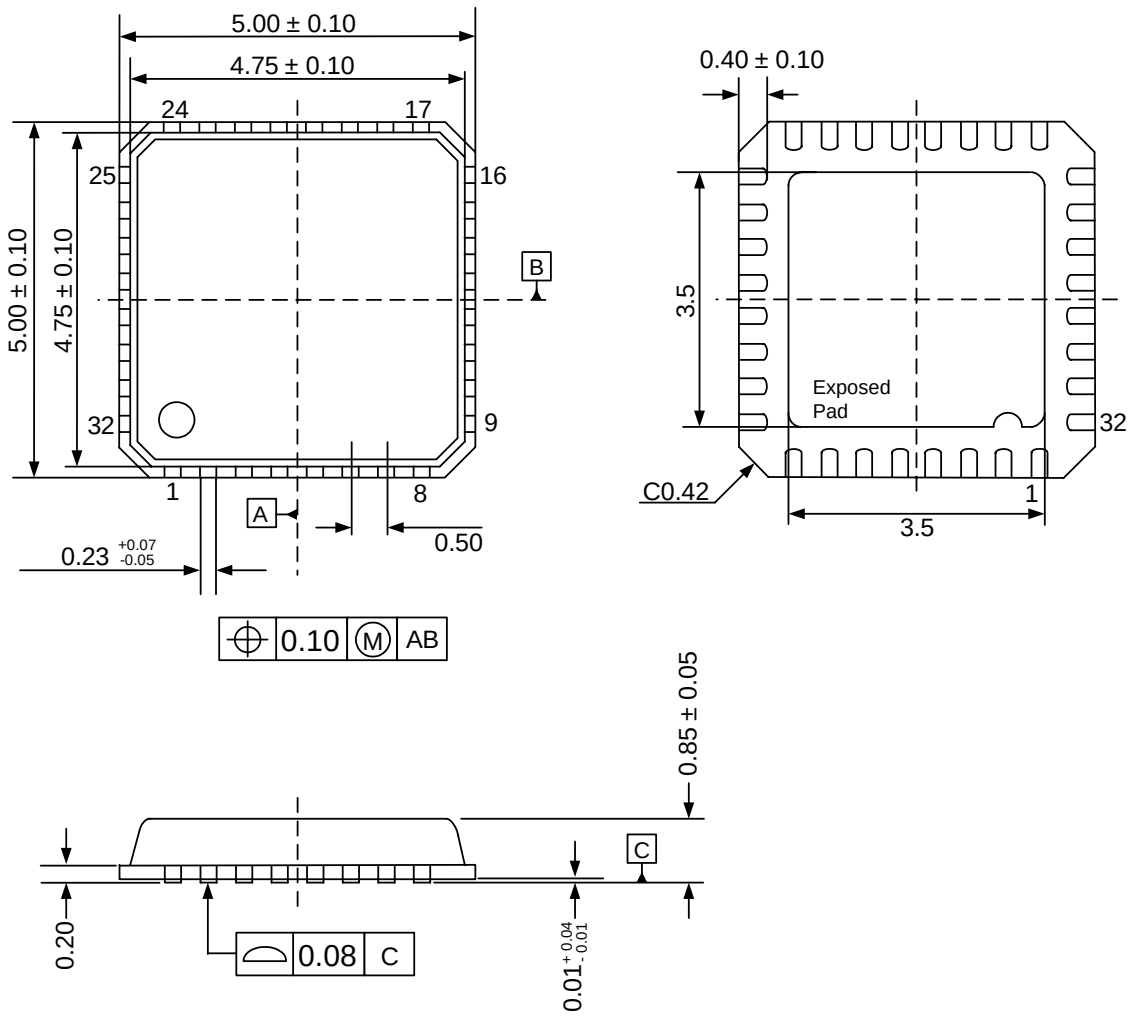
<Example>
(1) Pull down the MCKI pin: MCKPD bit = "0" → "1"
When the external master clock becomes Hi-Z, MCKI pin should be pulled down.
(2) Stop the external MCKI, BICK and FCK clocks.

■ Power down

If the clocks are supplied, power down VCOM (PMVCM bit: "1" → "0") after all blocks except for VCOM are powered-down and a master clock stops. The AK4632 is also powered-down by PDN pin = "L". When PDN pin = "L", the registers are initialized.

PACKAGE

● 32pin QFN (Unit: mm)

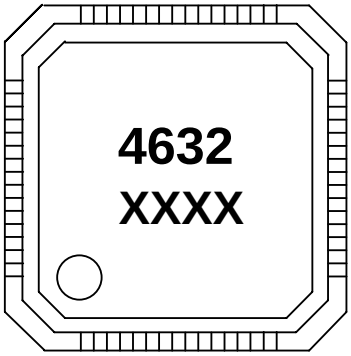


Note) The exposed pad on the bottom surface of the package must be open.

■ **Material & Lead finish**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXX : Date code identifier (4 digits)

Revision History

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