High Speed, Low Cost, Op Amp

Preliminary Technical Data

ADA4860-1

FEATURES

High speed
- **800 MHz, −3 dB bandwidth**
- **790 V/µs slew rate**
- **8 ns settling time to 0.5%**

Wide supply range: 5 V to 12 V
Low power: 6 mA
0.1 dB flatness: 125 MHz
Differential gain: 0.02%
Differential phase: 0.02°
Low voltage offset: 3.5 mV (typ)
High output current: 25 mA
Power down

APPLICATIONS

Consumer video
Professional video
Broadband video
ADC buffers
Active filters

PIN CONFIGURATION

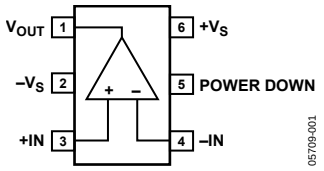

Figure 1. 6-Lead SOT-23 (RJ-6)

GENERAL DESCRIPTION

The ADA4860-1 is a low cost, high speed, current feedback op amp that provides excellent overall performance. The 800 MHz, −3 dB bandwidth, and 790 V/µs slew rate make this amplifier well suited for many high speed applications. With its combination of low price, excellent differential gain (0.02%), differential phase (0.02°), and 0.1 dB flatness out to 125 MHz, this amplifier is ideal for both consumer and professional video applications.

The ADA4860-1 is designed to operate on supply voltages as low as +5 V and up to ±5 V using only 6 mA of supply current. To further reduce power consumption, the amplifier is equipped with a power-down feature that lowers the supply current to 0.25 mA.

The ADA4860-1 is available in a 6-lead SOT-23 package and is designed to work over the extended temperature range of −40°C to +105°C.

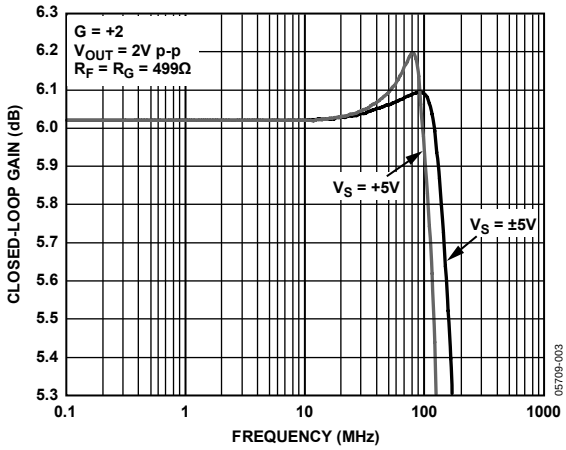

Figure 2. 0.1 dB Flatness

Rev. PrC

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REVISION HISTORY

1/06—Revision PrC: Preliminary Version

SPECIFICATIONS

V_S = +5 V (@ T_A = 25°C, G = +2, R_L = 150 Ω, C_L = 4 pF, unless otherwise noted). For G = +2, R_F = R_G = 499 Ω and for G = +1, R_F = 550 Ω.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.2 V p-p		460		MHz
	V_O = 2 V p-p		165		MHz
	V_O = 0.2 V p-p, R_L = 75 Ω		430		MHz
	G = +1, V_O = 0.2 V p-p		650		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p		58		MHz
	V_O = 2 V p-p, R_L = 75 Ω		45		MHz
+Slew Rate (Rising Edge)	V_O = 2 V p-p		695		V/µs
−Slew Rate (Falling Edge)	V_O = 2 V p-p		560		V/µs
Settling Time to 0.5%	V_O = 2 V step		8		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion HD2/HD3	f_C = 1 MHz, V_O = 2 V p-p		−90/−102		dBc
Harmonic Distortion HD2/HD3	f_C = 5 MHz, V_O = 2 V p-p		−70/−76		dBc
Input Voltage Noise	f = 100 kHz		4.0		nV/√Hz
Input Current Noise	f = 100 kHz, +IN/−IN		1.5/7.7		pA/√Hz
Differential Gain	R_L = 150 Ω		0.02		%
Differential Phase	R_L = 150 Ω		0.03		Degrees
DC PERFORMANCE					
Input Offset Voltage			−4.25		mV
+Input Bias Current			−1		µA
−Input Bias Current			+1.0		µA
Open-Loop Transresistance			650		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+IN		10		MΩ
	−IN		85		Ω
Input Capacitance	+IN		1.5		pF
Input Common-Mode Voltage Range			1.2 to 3.7		V
Common-Mode Rejection Ratio	V_{CM} = 2 V to 3 V		−56		dB
POWER DOWN PIN					
Input Voltage	Enabled		0.5		V
	Power down		1.8		V
Bias Current	Enabled		−200		nA
	Power down		60		µA
Turn-On Time			200		ns
Turn-Off Time			3.5		µs
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rise/Fall)	V_{IN} = +2.25 V to −0.25 V		60/100		ns
Output Voltage Swing	R_L = 75 Ω		1.2 to 3.8		V
	R_L = 150 Ω		1 to 4		V
	R_L = 1 kΩ		0.8 to 4.2		V
Short-Circuit Current	Sinking and sourcing		45		mA
POWER SUPPLY					
Operating Range					V
Total Quiescent Current	Enabled		5.2		mA
Quiescent Current	POWER DOWN pin = +V_S		0.2		mA
Power Supply Rejection Ratio					
+PSR	+V_S = 4 V to 6 V, −V_S = 0 V		−62		dB

V_S = ±5 V (@ T_A = 25°C, G = +2, R_L = 150 Ω, C_L = 4 pF, unless otherwise noted). For G = +2, R_F = R_G = 499 Ω and for G = +1, R_F = 550 Ω.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.2 V p-p		520		MHz
	V_O = 2 V p-p		230		MHz
	V_O = 0.2 V p-p, R_L = 75 Ω		480		MHz
	G = +1, V_O = 0.2 V p-p		800		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p		125		MHz
	V_O = 2 V p-p, R_L = 75 Ω		70		MHz
+Slew Rate (Rising Edge)	V_O = 2 V p-p		980		V/µs
−Slew Rate (Falling Edge)	V_O = 2 V p-p		790		V/µs
Settling Time to 0.5%	V_O = 2 V step		8		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion HD2/HD3	f_C = 1 MHz, V_O = 2 V p-p		−90/−102		dBc
Harmonic Distortion HD2/HD3	f_C = 5 MHz, V_O = 2 V p-p		−77/−94		dBc
Input Voltage Noise	f = 100 kHz		4.0		nV/√Hz
Input Current Noise	f = 100 kHz, +IN/−IN		1.5/7.7		pA/√Hz
Differential Gain	R_L = 150 Ω		0.02		%
Differential Phase	R_L = 150 Ω		0.02		Degrees
DC PERFORMANCE					
Input Offset Voltage			−3.5		mV
+Input Bias Current			−1.0		µA
−Input Bias Current			+1.5		µA
Open-Loop Transresistance			700		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+IN		12		MΩ
	−IN		90		Ω
Input Capacitance	+IN		1.5		pF
Input Common-Mode Voltage Range			−3.8 to +3.7		V
Common-Mode Rejection Ratio	V_{CM} = ±2 V		−58		dB
POWER DOWN PIN					
Input Voltage	Enabled		−4.4		V
	Power down		−3.2		V
Bias Current	Enabled		−250		nA
	Power down		130		µA
Turn-On Time			200		ns
Turn-Off Time			3.5		µs
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rise/Fall)	V_{IN} = ±3.0 V		45/90		ns
Output Voltage Swing	R_L = 75 Ω		±2		V
	R_L = 150 Ω		±3.1		V
	R_L = 1 kΩ		±4.1		V
Short-Circuit Current	Sinking and sourcing		85		mA
POWER SUPPLY					
Operating Range					V
Total Quiescent Current	Enabled		6		mA
Quiescent Current	POWER DOWN pin = +V_S		0.25		mA
Power Supply Rejection Ratio					
+PSR	+V_S = +4 V to +6 V, −V_S = −5 V		−64		dB
−PSR	+V_S = +5 V, −V_S = −4 V to −6 V, POWER DOWN pin = −V_S		−61		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$-V_S$ + 1 V to $+V_S$ − 1 V
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature	JEDEC J-STD-20
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
6-lead SOT-23	170	°C/W

Maximum Power Dissipation

The maximum safe power dissipation for the ADA4860-1 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a junction temperature of 150°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) for a sine wave and a resistor load is the total power consumed from the supply minus the load power.

$$P_D = Total\ Power\ Consumed - Load\ Power$$

$$P_D = \left(V_{SUPPLY\ VOLTAGE} \times I_{SUPPLY\ CURRENT}\right) - \frac{V_{OUT}{}^2}{R_L}$$

RMS output voltages should be considered.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads and through holes under the device reduces θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 6-lead SOT-23 (170°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

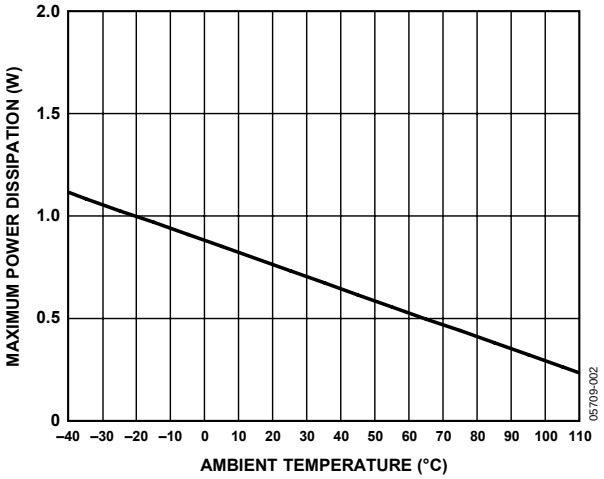


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

R_L = 150 Ω and C_L = 4 pF, unless otherwise noted.

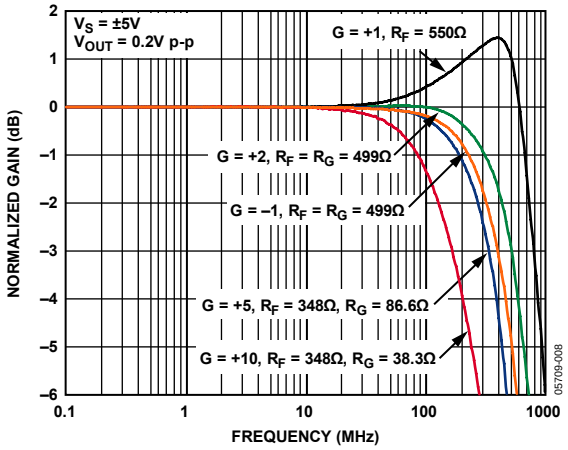


Figure 4. Small Signal Frequency Response for Various Gains

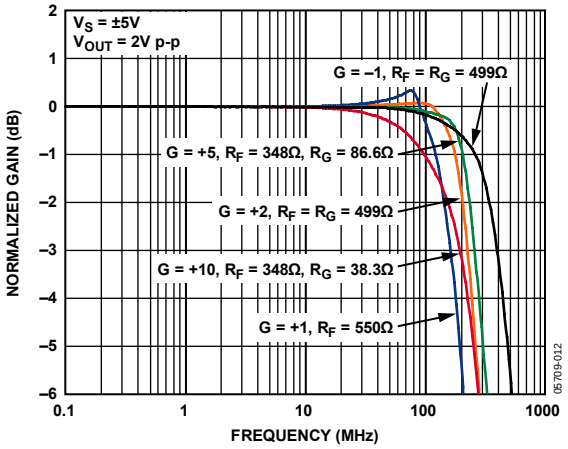


Figure 5. Large Signal Frequency Response for Various Gains

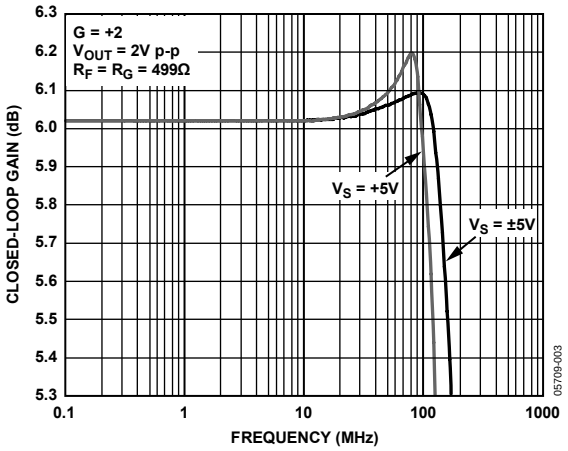


Figure 6. Large Signal 0.1 dB Flatness

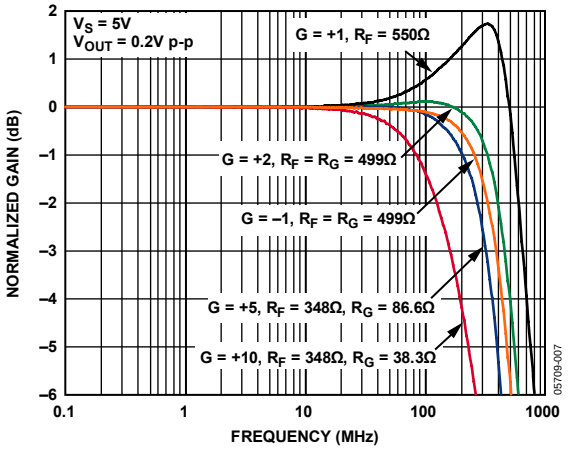


Figure 7. Small Signal Frequency Response for Various Gains

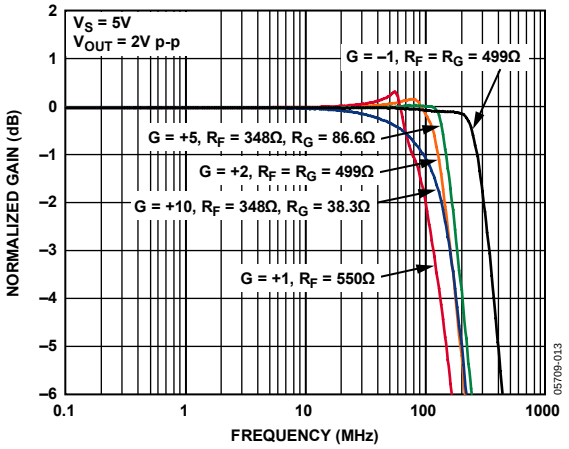


Figure 8. Large Signal Frequency Response for Various Supplies

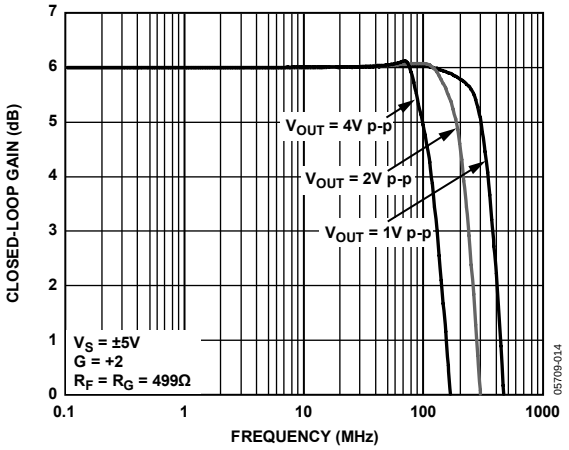


Figure 9. Large Signal Frequency Response for Various Output Levels

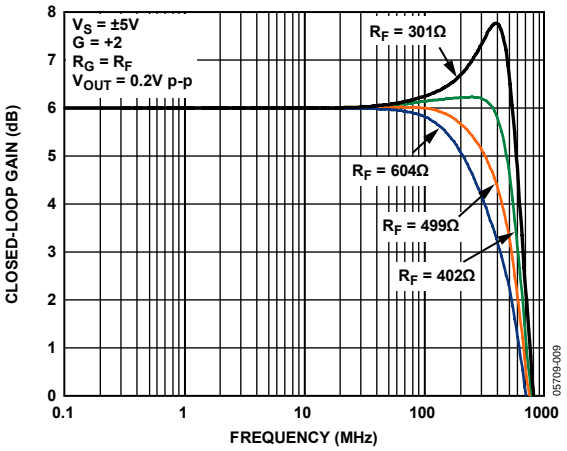


Figure 10. Small Signal Frequency Response vs. R_F

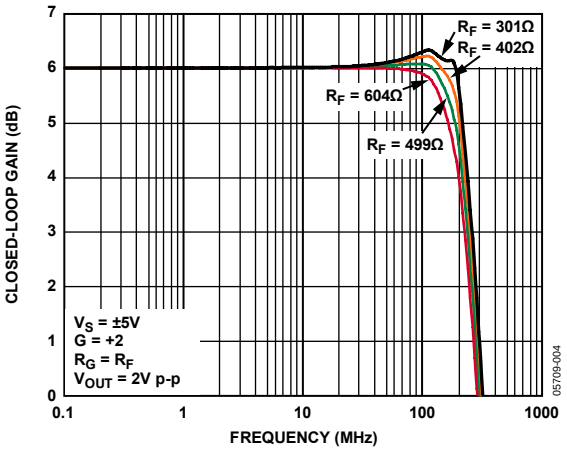


Figure 13. Large Signal Frequency Response vs. R_F

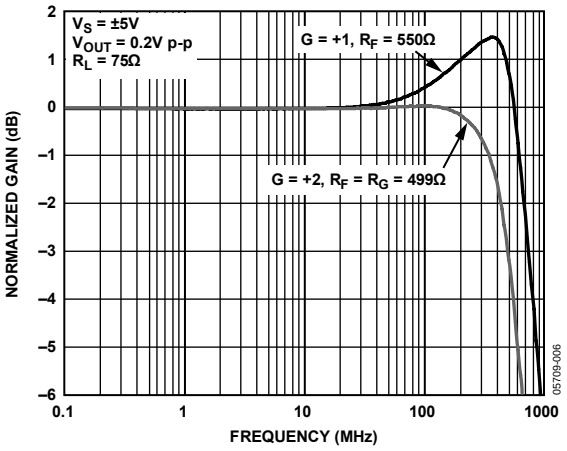


Figure 11. Small Signal Frequency Response for Various Gains

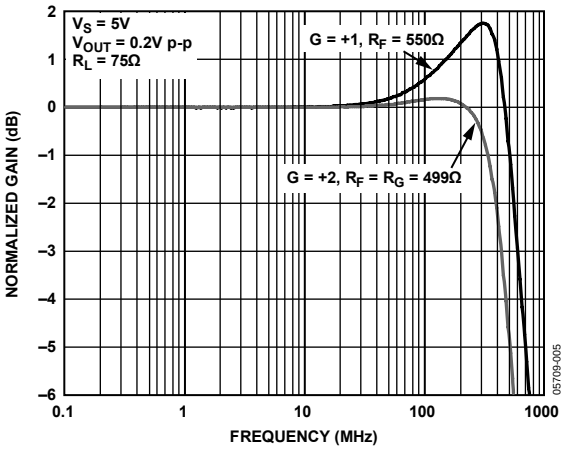


Figure 14. Small Signal Frequency Response for Various Gains

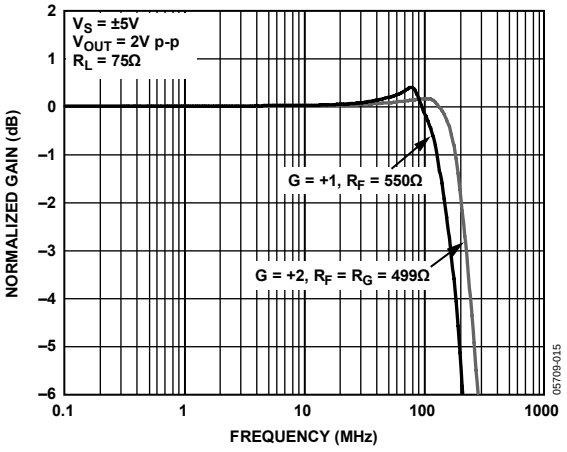


Figure 12. Large Signal Frequency Response for Various Gains

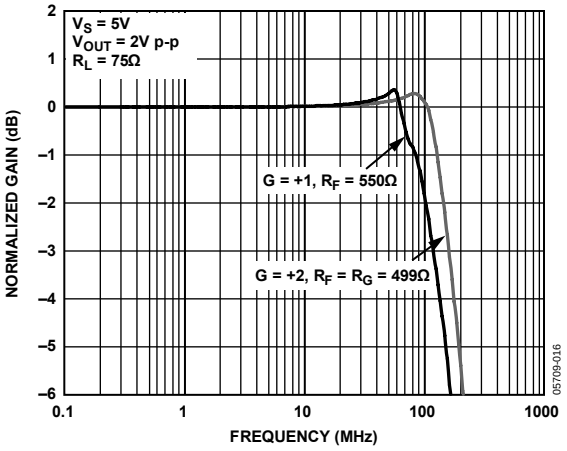


Figure 15. Large Signal Frequency Response for Various Gains

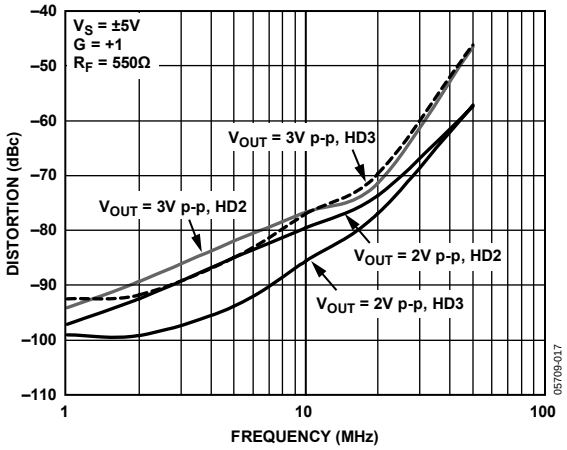


Figure 16. Harmonic Distortion vs. Frequency

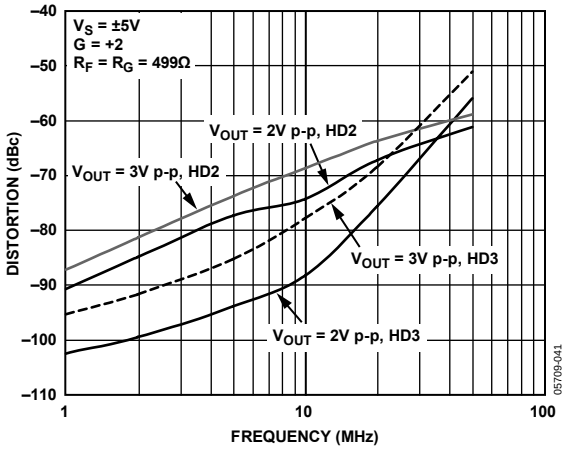


Figure 19. Harmonic Distortion vs. Frequency

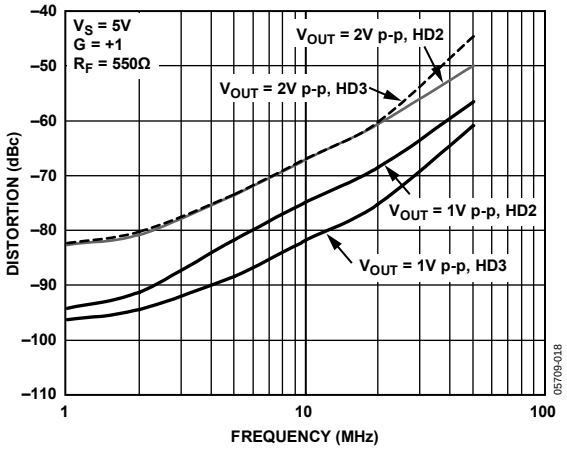


Figure 17. Harmonic Distortion vs. Frequency

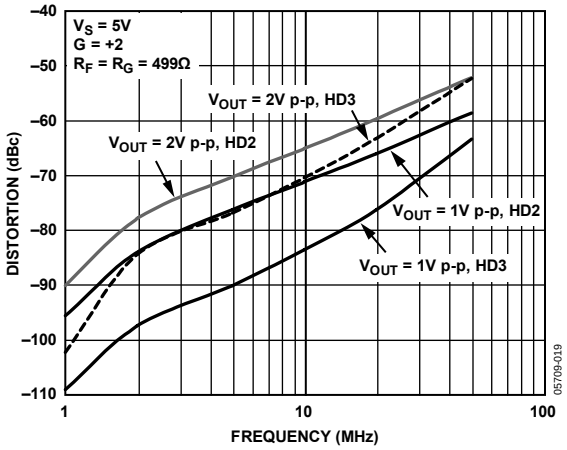


Figure 20. Harmonic Distortion vs. Frequency

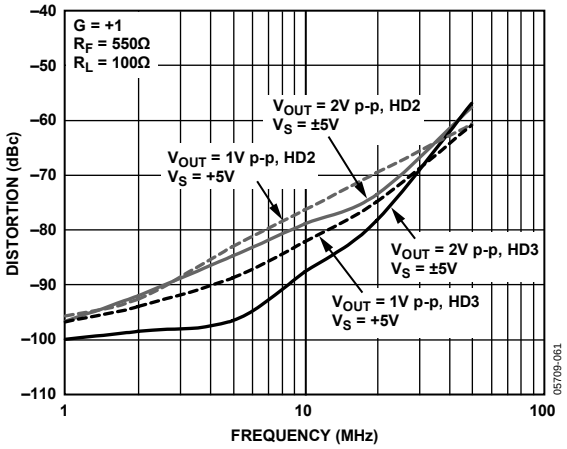


Figure 18. Harmonic Distortion vs. Frequency for Various Supplies

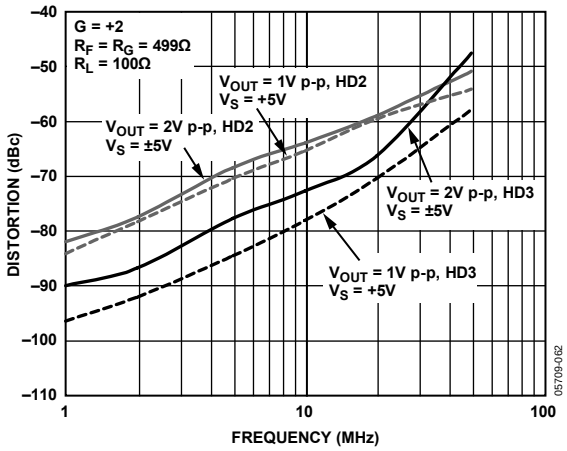


Figure 21. Harmonic Distortion vs. Frequency for Various Supplies

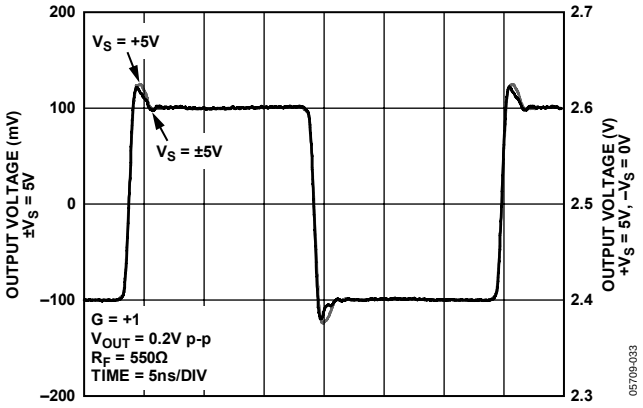


Figure 22. Small Signal Transient Response for Various Supplies

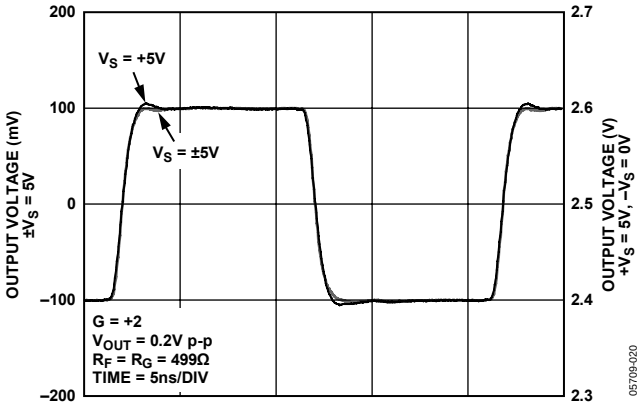


Figure 25. Small Signal Transient Response for Various Supplies

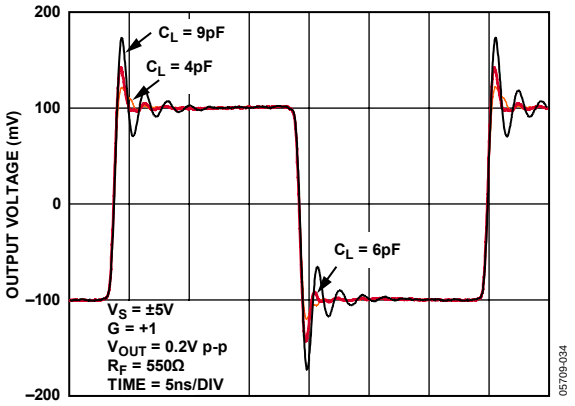


Figure 23. Small Signal Transient Response for Various Capacitor Loads

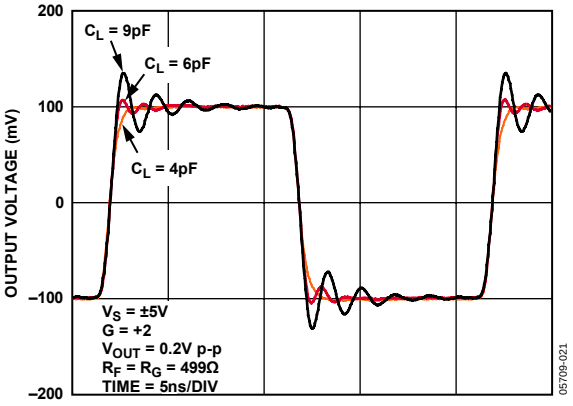


Figure 26. Small Signal Transient Response for Various Capacitor Loads

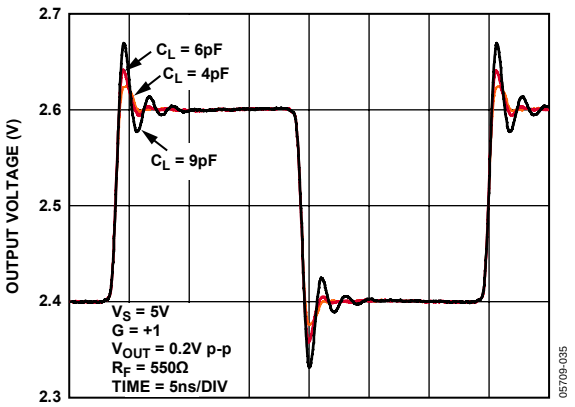


Figure 24. Small Signal Transient Response for Various Capacitor Loads

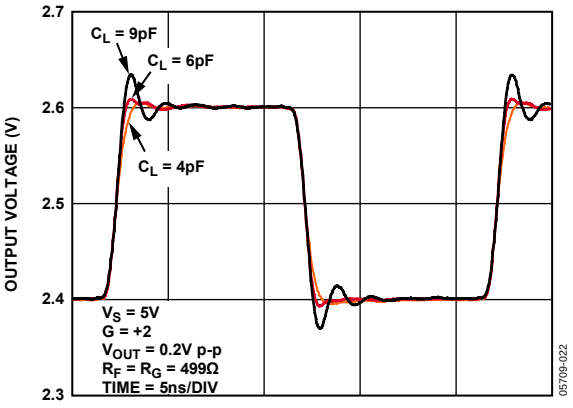


Figure 27. Small Signal Transient Response for Various Capacitor Loads

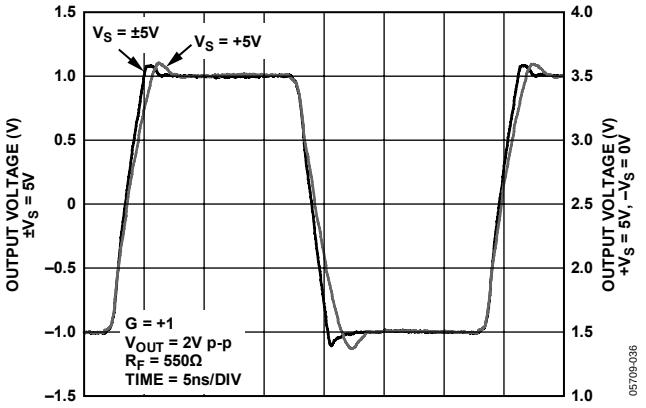


Figure 28. Large Signal Transient Response for Various Supplies

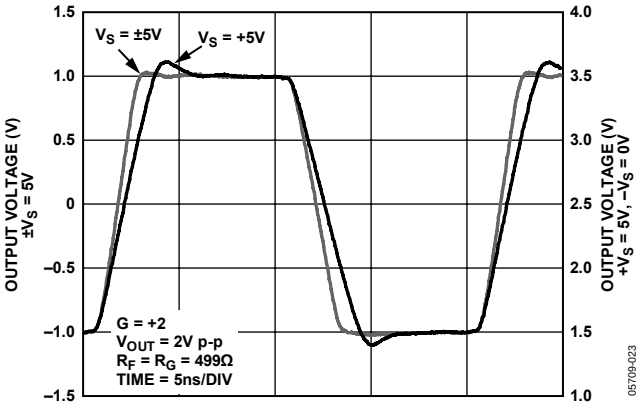


Figure 31. Large Signal Transient Response for Various Supplies

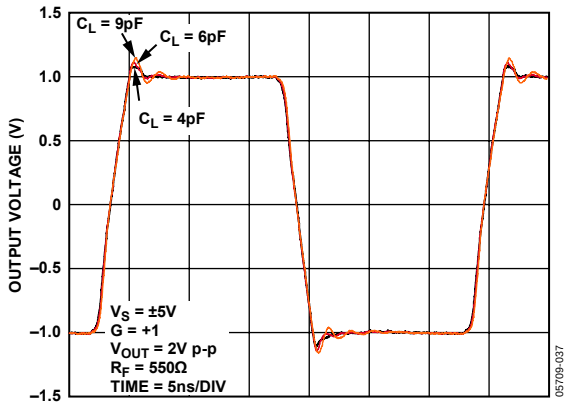


Figure 29. Large Signal Transient Response for Various Capacitor Loads

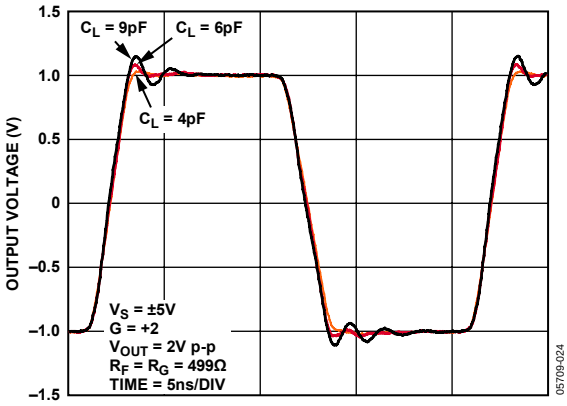


Figure 32. Large Signal Transient Response for Various Capacitor Loads

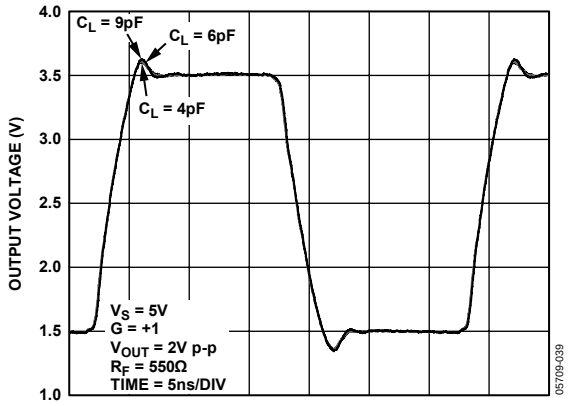


Figure 30. Large Signal Transient Response for Various Capacitor Loads

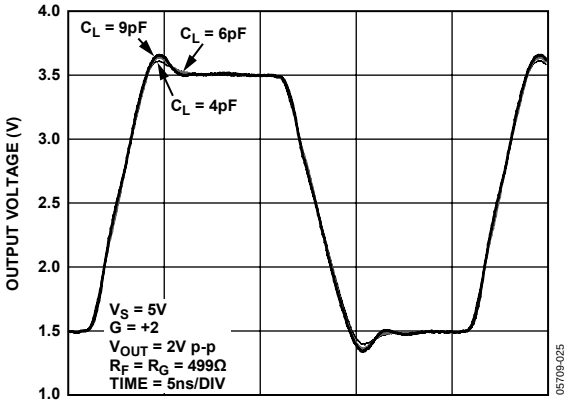


Figure 33. Large Signal Transient Response for Various Capacitor Loads

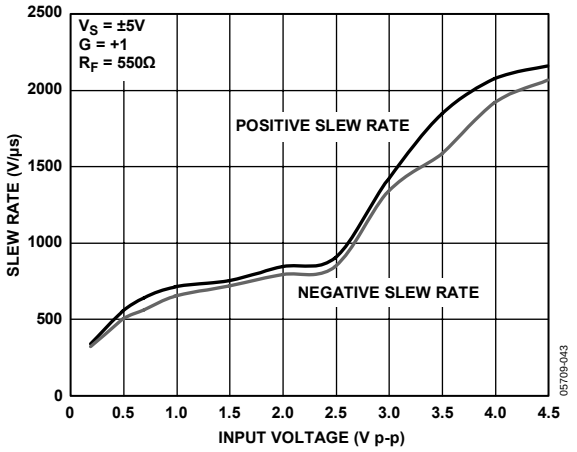


Figure 34. Slew Rate vs. Input Voltage

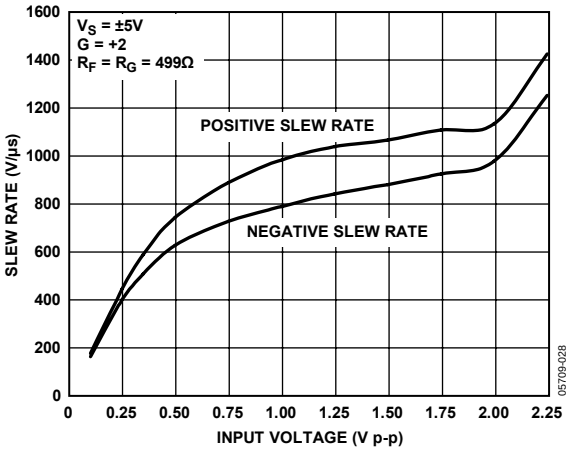


Figure 37. Slew Rate vs. Input Voltage

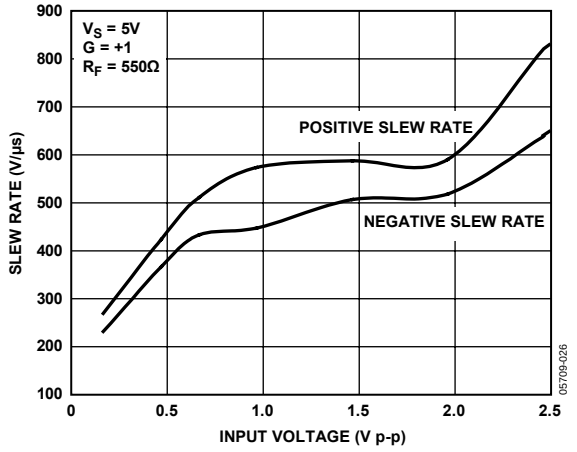


Figure 35. Slew Rate vs. Input Voltage

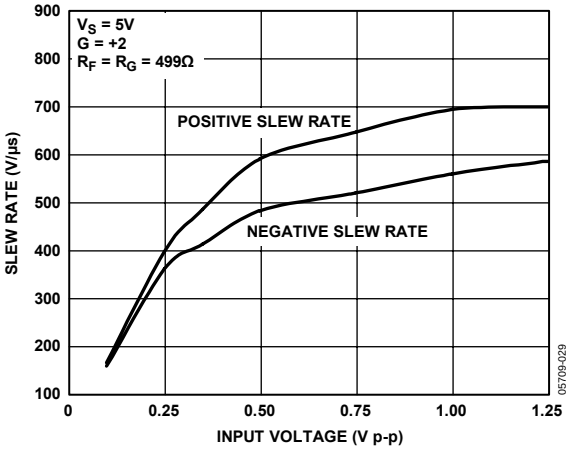


Figure 38. Slew Rate vs. Input Voltage

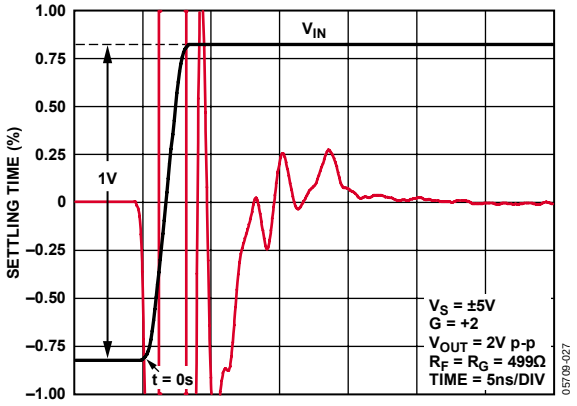


Figure 36. Settling Time Rising Edge

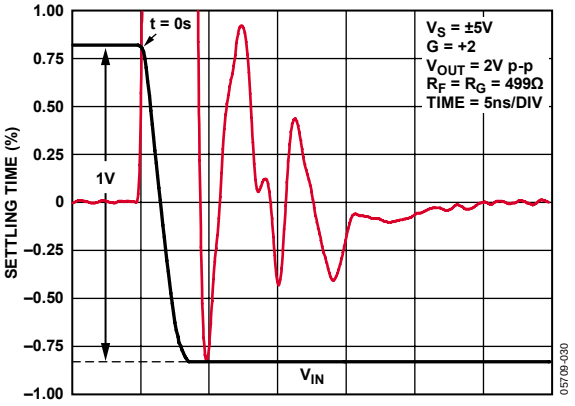


Figure 39. Settling Time Falling Edge

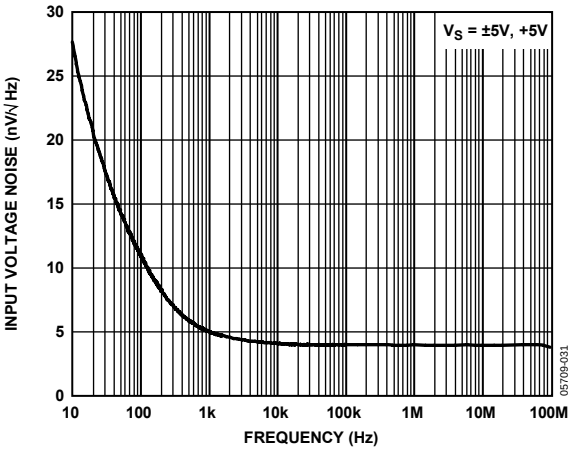


Figure 40. Input Voltage Noise vs. Frequency

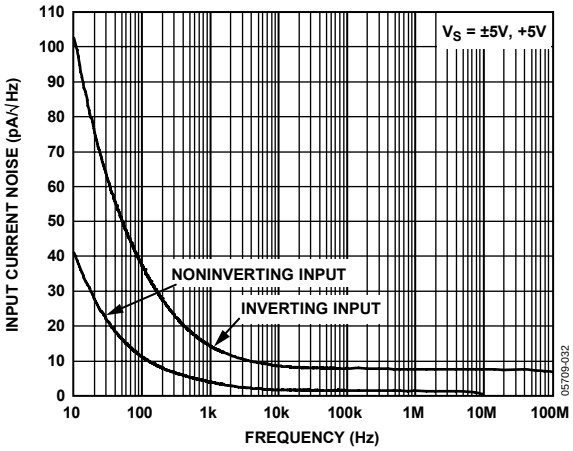


Figure 43. Input Current Noise vs. Frequency

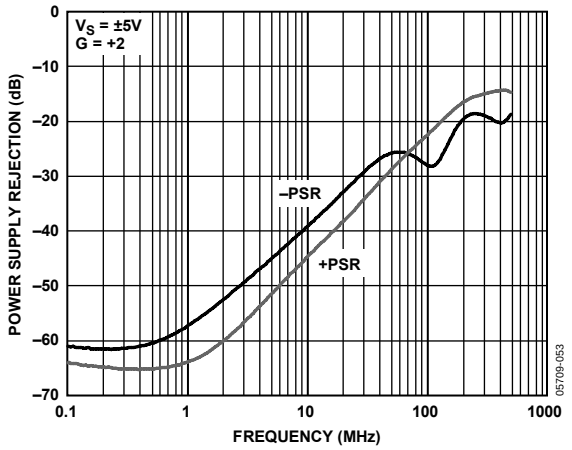


Figure 41. Power Supply Rejection vs. Frequency

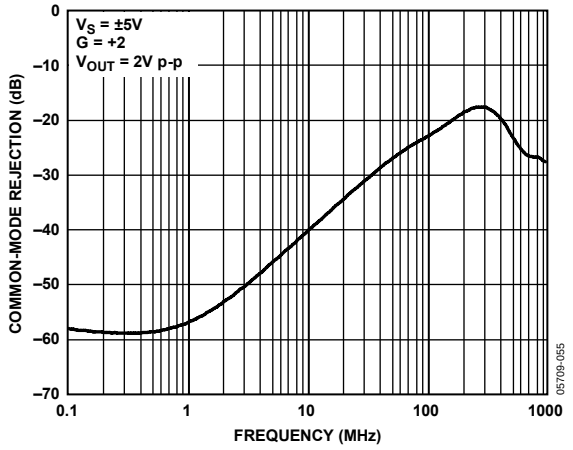


Figure 44. Common-Mode Rejection vs. Frequency

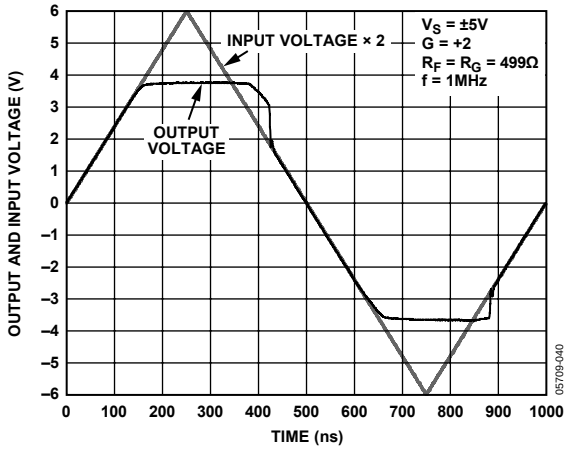


Figure 42. Output Overdrive Recovery

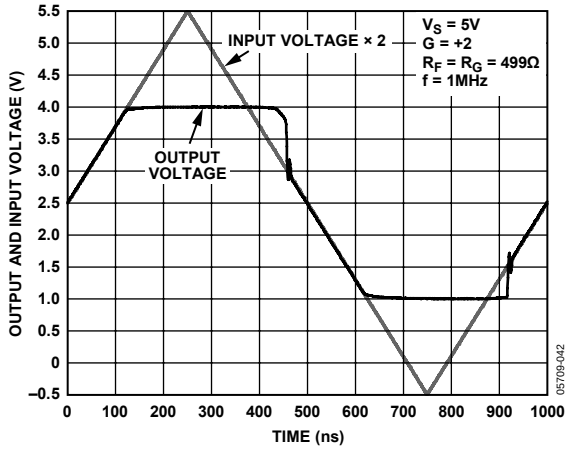


Figure 45. Output Overdrive Recovery

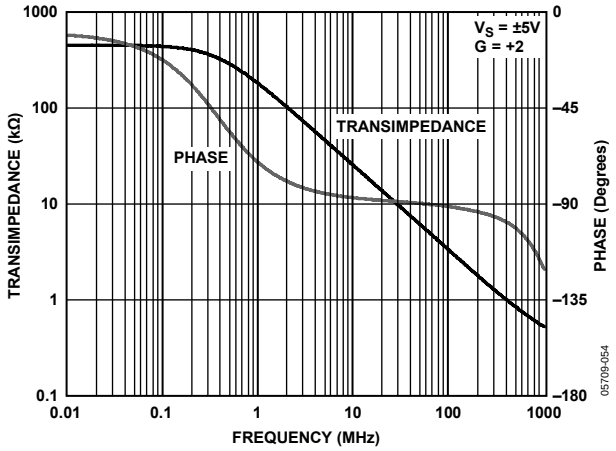


Figure 46. Transimpedance and Phase vs. Frequency

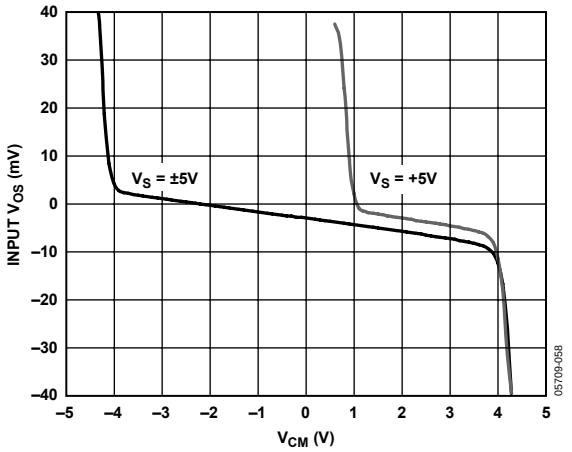


Figure 49. Input V_{OS} vs. Common-Mode Voltage

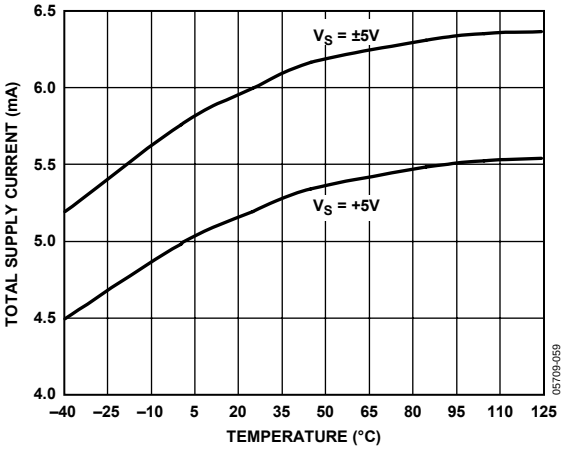


Figure 47. Supply Current at Various Supplies vs. Temperature

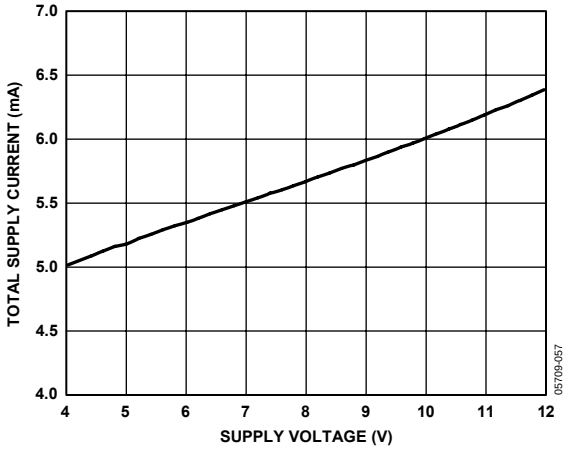


Figure 50. Supply Current vs. Supply Voltage

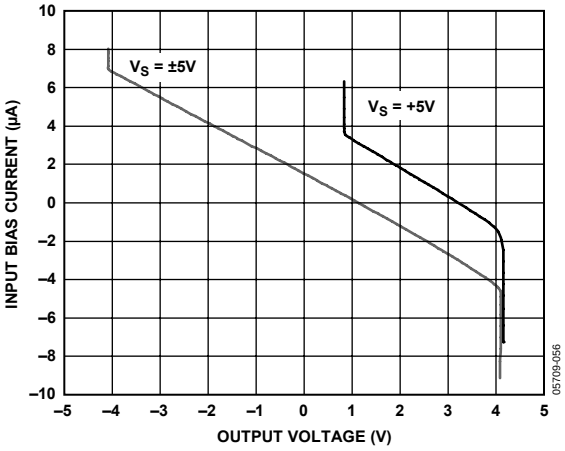


Figure 48. Inverting Input Bias Current vs. Output Voltage

APPLICATIONS

POWER SUPPLY BYPASSING

Attention must be paid to bypassing the power supply pins of the ADA4860-1. High quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), should be used to minimize supply voltage ripple and power dissipation. A large, usually tantalum, 2.2 µF to 47 µF capacitor located in proximity to the ADA4860-1 is required to provide good decoupling for lower frequency signals. The actual value is determined by the circuit transient and frequency requirements. In addition, 0.1 µF MLCC decoupling capacitors should be located as close to each of the power supply pins as is physically possible, no more than ⅛ inch away. The ground returns should terminate immediately into the ground plane. Locating the bypass capacitor return close to the load return minimizes ground loops and improves performance.

GAIN CONFIGURATIONS

The feedback resistor has a direct impact on the closed-loop bandwidth and stability of the current feedback op amp circuit. Reducing the resistance below the recommended value can make the amplifier response peak and even become unstable. Increasing the size of the feedback resistor reduces the closed-loop bandwidth. Table 5 provides a convenient reference for quickly determining the feedback and gain set resistor values and bandwidth for common gain configurations.

Table 5. Recommended Values and Frequency Performance[1]

Gain	R_F (Ω)	R_G (Ω)	−3 dB SS BW (MHz)	−3 dB LS BW (MHz)	Large Signal 0.1 dB Flatness
+1	550	N/A	800	165	40
−1	499	499	400	400	80
+2	499	499	520	230	125
+5	348	86.6	335	265	100
+10	348	38.3	165	195	28

[1] Conditions: V_S = ±5 V, T_A = 25°C, R_L = 150 Ω.

Figure 51 and Figure 52 show the typical noninverting and inverting configurations and the recommended bypass capacitor values.

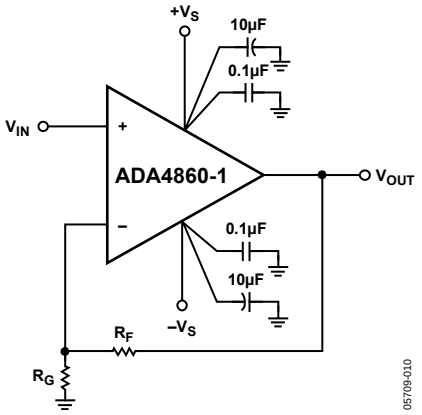


Figure 51. Noninverting Gain

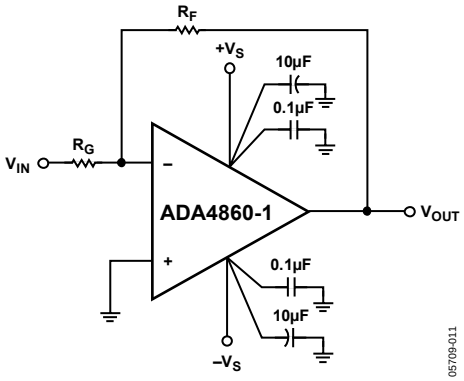


Figure 52. Inverting Gain

DRIVING CAPACITIVE LOADS

If driving loads with a capacitive component is desired, the best frequency response is obtained by the addition of a small series resistance, as shown in Figure 53. Figure 54 shows the optimum value for R_{SERIES} vs. capacitive load. The test was performed with a 50 MHz, 50% duty cycle pulse, with an amplitude of 200 mV p-p. The criteria for R_{SERIES} selection was based on maintaining approximately 1 dB of peaking in small signal frequency response. It is worth noting that the frequency response of the circuit can be dominated by the passive roll-off of R_{SERIES} and C_L.

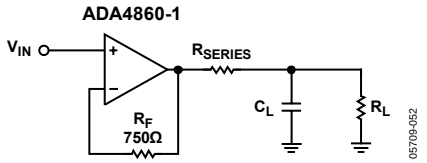


Figure 53. Driving Capacitive Loads

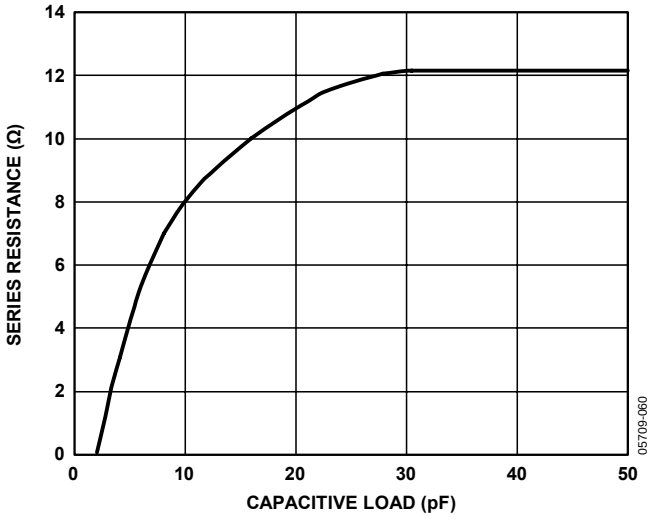


Figure 54. Recommended R_{SERIES} vs. Capacitive Load

POWER DOWN PIN

The ADA4860-1 is equipped with a power-down function. The POWER DOWN pin allows the user to reduce the quiescent supply current when the amplifier is not being used. The power-down threshold levels are derived from the voltage applied to the $-V_S$ pin. When used in single-supply applications, this is especially useful with conventional logic levels. The amplifier is powered down when the voltage applied to the POWER DOWN pin is greater than ($-V_S$ + 1 V). The amplifier is enabled whenever the POWER DOWN pin is left open, or the voltage on the POWER DOWN pin is less than ($-V_S$ + 1 V). If the POWER DOWN pin is not used, it should be connected to the negative supply.

VIDEO AMPLIFIER

With low differential gain and phase errors and wide 0.1 dB flatness, the ADA4860-1 is an ideal solution for consumer and professional video applications. Figure 55 shows a typical video driver set for a noninverting gain of +2, where $R_F = R_G = 499\ \Omega$. The video amplifier input is terminated into a shunt 75 Ω resistor. At the output, the amplifier has a series 75 Ω resistor for impedance matching to the video load.

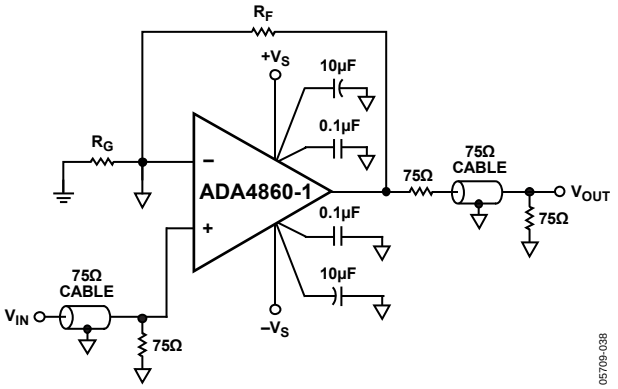


Figure 55. Video Driver Schematic

OPTIMIZING FLATNESS AND BANDWIDTH

When using the ADA4860-1, the variety of circuit conditions and parasitics can affect peaking, gain flatness, and −3 dB bandwidth. This section discusses how the ADA4860-1 small signal responses can be dramatically altered with basic circuit changes and added stray capacitances.

Particularly with low closed-loop gains, the feedback resistor (R_f) effects peaking and gain flatness. However, with gain = +1, −3 dB bandwidth varies slightly, while gain = +2 has a much larger variation. For gain = +1, Figure 56 shows the effect that various feedback resistors have on frequency response. In Figure 56, peaking is wide ranging yet −3 dB bandwidth vary by only 6%. In this case, the user must pick what is desired: more peaking or flatter bandwidth. Figure 57 shows gain = +2 bandwidth and peaking variations vs. R_F vs. R_L. Bandwidth delta vs. R_L increase was approximately 17%. Also for Figure 57, R_L = 100 Ω, the −3 dB bandwidth changed 49% as R_F was lowered with excessive compromises in peaking. For more gain = +2 bandwidth variations vs. R_F, see Figure 10 and Figure 13.

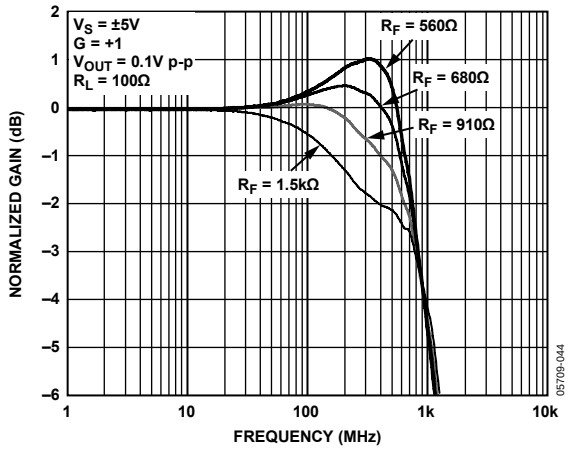


Figure 56. Small Signal Frequency Response vs. R_F

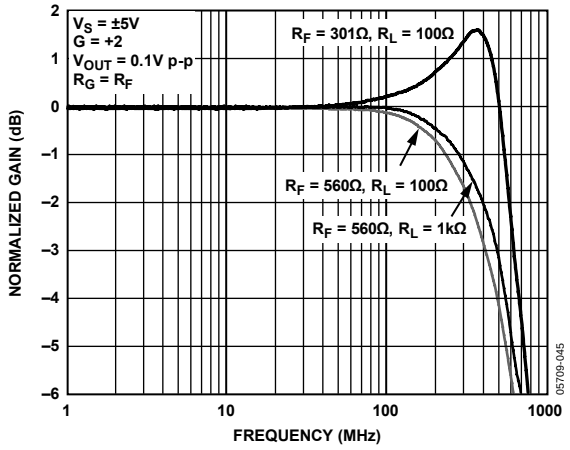


Figure 57. Small Signal Frequency Response vs. R_F vs. R_L

The impact of resistor case sizes was observed using the circuit drawn in Figure 58. The types and sizes chosen were 0402 case sized thin film and 1206 thick film. All other measurement conditions were kept constant except for the case size and resistor composition.

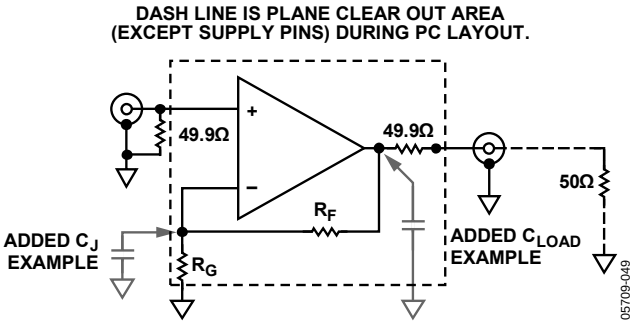


Figure 58. Noninverting Gain Setup for Illustration of Parasitic Effects, 50 Ω System, R_L = 100 Ω

In Figure 59, a slight −3 dB bandwidth delta of approximately 10% can be seen going from a small-to-large case size. The increase in bandwidth with the larger 1206 case size is caused by an increase in parasitic capacitance across the chip resistor. This extra capacitance is known to extend amplifier frequency response. Therefore, while a variation in chip resistor case size causes small bandwidth shifts, this should not stifle the user's case size selections.

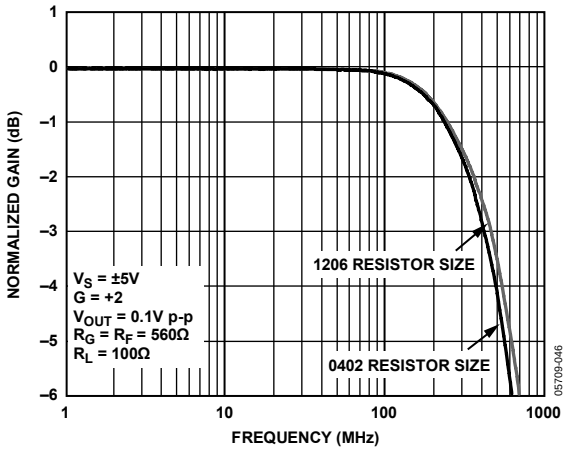


Figure 59. Small Signal Frequency Response vs. Resistor Size

Initially, a small capacitor of 0.4 pF was added to the amplifier summing junction of two boards with equal and opposite gains of +2 and −2. The results are shown in Figure 60. In a second test, 5.6 pF of capacitance was added directly at the output of the gain = +2 amplifier. The results are shown in Figure 61.

Figure 60 reveals extra summing junction capacitance, which affects noninverting gain circuits vs. inverting gain. With gain = +2, the additional 0.4 pF of added capacitance created an extra 43% −3 dB bandwidth extension, plus some extra peaking. For gain = −2, a 5% increase in −3 dB bandwidth was created with an extra 0.4 pF on summing junction.

Extra output capacitive loading on the ADA4860-1 also causes bandwidth extensions, as seen in Figure 61. The effect on the gain = +2 circuit is more pronounced with lighter resistive loading (1 kΩ). For pulse response behavior with added output capacitances, see Figure 23, Figure 24, Figure 26, Figure 27, Figure 29, Figure 30, Figure 32, and Figure 33.

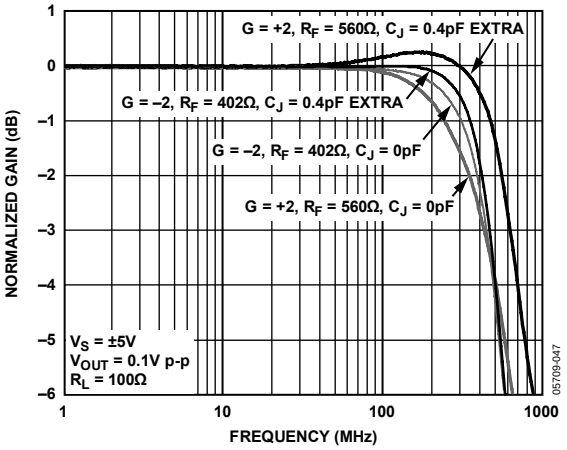


Figure 60. Small Signal Frequency Response vs. Added Summing Junction Capacitance

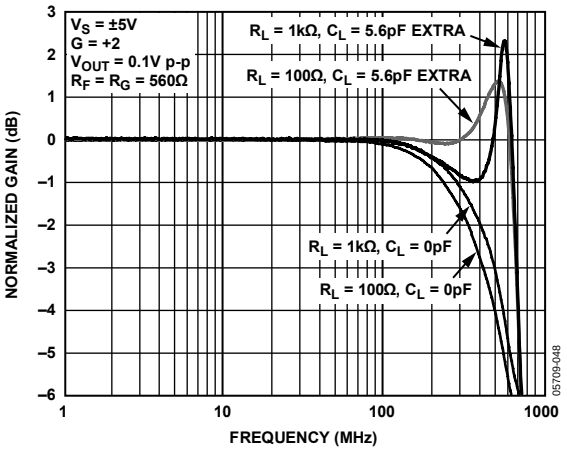


Figure 61. Small Signal Frequency Response vs. Output Capacitive Load

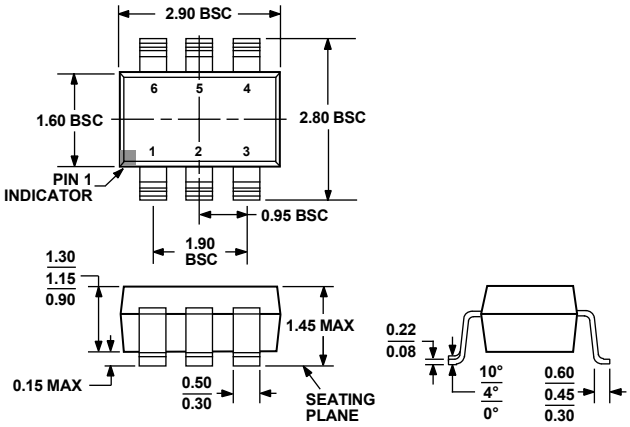
Optimization of circuit performance is accomplished with signal amplitudes that are relevant to a specific application. For example, in video applications, the gain = +2 circuit can be optimized for output signal amplitudes of 2 V p-p. Minimizing ac peaking and obtaining highest frequency flatband characteristics should result in the best overall circuit performance.

LAYOUT

Careful attention to printed circuit board (PCB) layout prevents associated board parasitics from becoming problematic and affecting gain flatness and −3 dB bandwidth. In the printed circuit environment, parasitics around summing junction (inverting input) or output pins can alter pulse and frequency response. Parasitic capacitance can be unintentionally created on a PC board via two parallel metal planes with a small vertical separation (in FR4). To avoid parasitic problems near the summing junction signal lines connections between the feedback and gain resistors should be kept as short as possible to minimize the inductance and stray capacitance. For similar reasons, termination and load resistors should be located as close as possible to the respective inputs. Lastly, removing the ground plane on all layers from the area near and under the input and output pins reduces stray capacitance.

It is important to realize the impact of printed circuit board parasitics. The best performing current feedback amplifier circuit layouts mitigate stray board capacitances around the summing junction and outputs by isolating capacitive loads using low value output series resistors. For more information on high speed board layout, go to: www.analog.com and www.analog.com/library/analogDialogue/archives/39-09/layout.html.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 62. 6-Lead Plastic Surface-Mount Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Ordering Quantity	Package Option	Branding
ADA4860-1YRJZ-RL[1]	–40°C to +105°C	6-Lead SOT-23	10,000	RJ-6	HKB
ADA4860-1YRJZ-RL7[1]	–40°C to +105°C	6-Lead SOT-23	3,000	RJ-6	HKB
ADA4860-1YRJZ-R2[1]	–40°C to +105°C	6-Lead SOT-23	250	RJ-6	HKB

[1] Z = Pb-free part.

NOTES

NOTES

PR05709-0-1/06(PrC)