Low-power dual 2-input NAND Schmitt trigger Rev. 4 — 4 November 2010

Product data sheet

General description 1.

The 74AUP2G132 provides the dual 2-input NAND Schmitt trigger function which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using IOFF. The IOFF circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

The inputs switch at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the input hysteresis voltage V_H.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- ESD protection:
 - HBM JESD22-A114F Class 3A exceeds 5000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; I_{CC} = 0.9 μA (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

- Wave and pulse shaper
- Astable multivibrator
- Monostable multivibrator



Low-power dual 2-input NAND Schmitt trigger

4. Ordering information

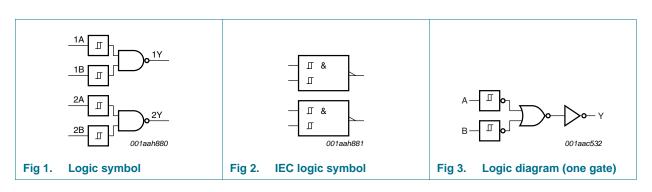
Table 1. Ordering	g information			
Type number	Package			
	Temperature range	Name	Description	Version
74AUP2G132DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AUP2G132GT	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 \times 1.95 \times 0.5 mm	SOT833-1
74AUP2G132GF	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 \times 1 \times 0.5 mm	SOT1089
74AUP2G132GD	–40 °C to +125 °C	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body $3 \times 2 \times 0.5$ mm	SOT996-2
74AUP2G132GM	–40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body $1.6 \times 1.6 \times 0.5$ mm	SOT902-1
74AUP2G132GN	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body $1.2 \times 1.0 \times 0.35$ mm	SOT1116
74AUP2G132GS	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body $1.35 \times 1.0 \times 0.35$ mm	SOT1203

5. Marking

Table 2. Marking codes	
Type number	Marking code ^[1]
74AUP2G132DC	aE2
74AUP2G132GT	aE2
74AUP2G132GF	aE
74AUP2G132GD	aE2
74AUP2G132GM	aE2
74AUP2G132GN	aE
74AUP2G132GS	aE

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram



 74AUP2G132
 All information provided in this document is subject to legal disclaimers.
 © NXP B.V. 2010. All rights reserved.

 Product data sheet
 Rev. 4 — 4 November 2010
 2 of 23

1A

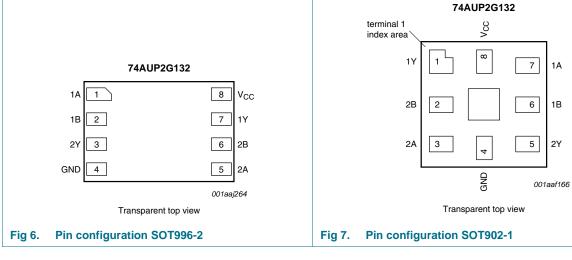
1B

2Y

Low-power dual 2-input NAND Schmitt trigger

7. Pinning information

74AUP2G132 1A 1 8 Vcc 1B 2 7 1Y 74AUP2G132 6 2B 2Y 3 8 V_{CC} 1A 1 7 1Y 1B 2 GND 2A 5 6 2B 4 2Y 3 5 2A GND 4 001aaf165 001aaf164 Transparent top view Pin configuration SOT765-1 Pin configuration SOT833-1, SOT1089, Fig 4. Fig 5. SOT1116 and SOT1203



7.2 Pin description

Symbol	Pin	Pin			
	SOT765-1, SOT833-1, SOT1089, SOT996-2, SOT1116 and SOT1203	SOT902-1			
1A, 2A	1, 5	7, 3	data input		
1B, 2B	2,6	6, 2	data input		
GND	4	4	ground (0 V)		
1Y, 2Y	7, 3	1, 5	data output		
V _{CC}	8	8	supply voltage		
74AUP2G132	All information provide	d in this document is subject to	o legal disclaimers.	© NXP B.V. 2010. All rights reserved.	
Product data	sheet Rev. 4	4 — 4 November 2	010	3 of 23	

7.1 Pinning

Low-power dual 2-input NAND Schmitt trigger

8. Functional description

Table 4.	Function table[1]		
Input			Output
nA		nB	nY
L		L	н
L		Н	Н
Н		L	Н
Н		Н	L

[1] H = HIGH voltage level; L = LOW voltage level.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
I _{IK}	input clamping current	V ₁ < 0 V	-50	-	mA
VI	input voltage		<u>[1]</u> –0.5	+4.6	V
Ι _{ΟΚ}	output clamping current	V _O < 0 V	-50	-	mA
Vo	output voltage	Active mode and Power-down mode	<u>[1]</u> –0.5	+4.6	V
lo	output current	$V_{O} = 0 V$ to V_{CC}	-	±20	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2] _	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
 For XSON8, XSON8U and XQFN8U packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

10. Recommended operating conditions

Table 6.	Operating conditions				
Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		0.8	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; $V_{CC} = 0 V$	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C

Low-power dual 2-input NAND Schmitt trigger

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Uni
T _{amb} = 2	5 °C					
√ _{ОН}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_{O} = –20 $\mu A;$ V_{CC} = 0.8 V to 3.6 V	$V_{CC}-0.1$	-	-	V
		$I_{O} = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.75 imes V_{CC}$	-	-	V
		$I_{O} = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	1.11	-	-	V
		$I_{O} = -1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.32	-	-	V
		$I_{O} = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	2.05	-	-	V
		$I_{O} = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.9	-	-	V
		$I_{O} = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.72	-	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.6	-	-	V
/ _{OL}	LOW-level output voltage	$V_{I} = V_{T+}$ or V_{T-}				
		I_{O} = 20 μ A; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	$0.3 imes V_{CC}$	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.31	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.31	V
		$I_0 = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
		$I_0 = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.44	V
I	input leakage current	$V_I = GND$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.1	μA
OFF	power-off leakage current	V_{I} or $V_{O} = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.2	μA
∆I _{OFF}	additional power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.2	μA
сс	supply current	$V_I = GND \text{ or } V_{CC}; I_O = 0 \text{ A};$ $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.5	μA
VI _{CC}	additional supply current	$V_1 = V_{CC} - 0.6 \text{ V}; \text{ I}_O = 0 \text{ A};$ $V_{CC} = 3.3 \text{ V}$	[1] -	-	40	μA
C _I	input capacitance	$V_I = GND \text{ or } V_{CC}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	1.1	-	pF
Co	output capacitance	$V_O = GND; V_{CC} = 0 V$	-	1.7	-	pF
amb = -4	40 °C to +85 °C					
/ _{ОН}	HIGH-level output voltage	$V_{I} = V_{T+}$ or V_{T-}				
		I_{O} = -20 μ A; V_{CC} = 0.8 V to 3.6 V	$V_{CC}-0.1$	-	-	V
		$I_0 = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.7 imes V_{CC}$	-	-	V
		$I_0 = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	1.03	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.30	-	-	V
		$I_{\rm O} = -2.3 \text{ mA}; V_{\rm CC} = 2.3 \text{ V}$	1.97	-	-	V
		$I_{\rm O} = -3.1 \text{ mA}; V_{\rm CC} = 2.3 \text{ V}$	1.85	-	-	V
		$I_{\rm O} = -2.7 \text{ mA}; V_{\rm CC} = 3.0 \text{ V}$	2.67	-	-	V
		$I_0 = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.55	-	-	V

NXP Semiconductors

74AUP2G132

Low-power dual 2-input NAND Schmitt trigger

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{OL}	LOW-level output voltage	$V_1 = V_{T+}$ or V_{T-}				
		I_{O} = 20 $\mu A; V_{CC}$ = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	$0.3\times V_{CC}$	V
		$I_0 = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.37	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.35	V
		$I_0 = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.33	V
		$I_0 = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_0 = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.33	V
		$I_0 = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.45	V
lı	input leakage current	V_1 = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	μA
I _{OFF}	power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.5	μΑ
ΔI_{OFF}	additional power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.6	μA
l _{cc}	supply current	$\label{eq:VI} \begin{array}{l} V_{I} = GND \text{ or } V_{CC}; \ I_{O} = 0 \ A; \\ V_{CC} = 0.8 \ V \ to \ 3.6 \ V \end{array}$	-	-	0.9	μA
Δl _{CC}	additional supply current		<u>[1]</u> _	-	50	μA
T _{amb} = –	40 °C to +125 °C					
V _{OH}	HIGH-level output voltage	$V_1 = V_{T+}$ or V_{T-}				
		I_{O} = –20 $\mu A;$ V_{CC} = 0.8 V to 3.6 V	$V_{CC}-0.11$	-	-	V
		$I_0 = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.6\times V_{CC}$	-	-	V
		$I_0 = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	0.93	-	-	V
		$I_{O} = -1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.17	-	-	V
		$I_{O} = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.77	-	-	V
		$I_{O} = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.67	-	-	V
		$I_{O} = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.40	-	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.30	-	-	V
V _{OL}	LOW-level output voltage	$V_1 = V_{T+}$ or V_{T-}				
		I_{O} = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	$0.33 \times V_{CC}$	V
		$I_0 = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		$I_0 = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		$I_0 = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	V
		$I_0 = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.50	V
I	input leakage current	$V_I = GND$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.75	μΑ
I _{OFF}	power-off leakage current	$V_{\rm I}~{\rm or}~V_{\rm O}$ = 0 V to 3.6 V; $V_{\rm CC}$ = 0 V	-	-	±0.75	μΑ

Table 7. Static characteristics ... continued

Low-power dual 2-input NAND Schmitt trigger

At recom	At recommended operating conditions; voltages are referenced to GND (ground = 0 V).										
Symbol	Parameter	Conditions	Min	Тур	Max	Unit					
ΔI_{OFF}	additional power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.75	μA					
I _{CC}	supply current	$\label{eq:VI} \begin{array}{l} V_{I} = GND \text{ or } V_{CC}; \ I_{O} = 0 \ A; \\ V_{CC} = 0.8 \ V \text{ to } 3.6 \ V \end{array}$	-	-	1.4	μA					
ΔI_{CC}	additional supply current	$\label{eq:VI} \begin{array}{l} V_{I} = V_{CC} - 0.6 \; V; \; I_{O} = 0 \; A; \\ V_{CC} = 3.3 \; V \end{array}$	<u>[1]</u> -	-	75	μA					

Table 7. Static characteristics ... continued

[1] One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.

12. Dynamic characteristics

Table 8. **Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V: for test circuit see Figure 9.

Symbol	Parameter	Conditions		Tai	mb = 25 °	°C	T _{amb} =	−40 °C t	o +125 °C	Unit
				Min	Typ <mark>[1]</mark>	Max	Min	Max (85 °C)	Max (125 °C)	
C _L = 5 pl	F									
t _{pd}	propagation delay	nA or nB to nY; see Figure 8	[2]							
		$V_{CC} = 0.8 V$		-	22.5	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		2.6	6.3	13.4	2.4	15.1	16.6	ns
		V_{CC} = 1.4 V to 1.6 V		2.2	4.6	8.2	1.9	9.7	10.7	ns
		V_{CC} = 1.65 V to 1.95 V		1.9	3.9	6.6	1.7	7.9	8.7	ns
		V_{CC} = 2.3 V to 2.7 V		1.7	3.2	5.3	1.5	6.2	6.8	ns
		V_{CC} = 3.0 V to 3.6 V		1.6	2.9	4.7	1.4	5.6	6.2	ns
C _L = 10	pF									
t _{pd}	propagation delay	nA or nB to nY; see Figure 8	[2]							
		$V_{CC} = 0.8 V$		-	26.1	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		3.0	7.2	15.4	2.7	17.3	19.0	ns
		V_{CC} = 1.4 V to 1.6 V		2.5	5.2	9.3	2.2	11.0	12.1	ns
		V_{CC} = 1.65 V to 1.95 V		2.3	4.5	7.5	2.0	9.0	9.9	ns
		V_{CC} = 2.3 V to 2.7 V		2.1	3.8	6.1	1.8	7.2	7.9	ns
		V_{CC} = 3.0 V to 3.6 V		2.0	3.5	5.5	1.8	6.5	7.2	ns
C _L = 15 p	pF									
t _{pd}	propagation delay	nA or nB to nY; see Figure 8	[2]							
		$V_{CC} = 0.8 V$		-	29.6	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		3.3	8.0	17.2	3.0	19.4	21.3	ns
		V_{CC} = 1.4 V to 1.6 V		2.8	5.8	10.4	2.5	12.3	13.5	ns
		V_{CC} = 1.65 V to 1.95 V		2.6	5.0	8.3	2.3	10.0	11.0	ns
		V_{CC} = 2.3 V to 2.7 V		2.3	4.2	6.7	2.1	7.9	8.7	ns
		$V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$		2.2	3.9	6.1	2.0	7.3	8.0	ns

Low-power dual 2-input NAND Schmitt trigger

Symbol	Parameter	Conditions	Ta	T _{amb} = 25 °C			T _{amb} = −40 °C to +125 °C		
				Typ <mark>[1]</mark>	Max	Min	Max (85 °C)	Max (125 °C)	
C _L = 30	pF								
t _{pd}	propagation delay	nA or nB to nY; see Figure 8							
		$V_{CC} = 0.8 V$	-	39.9	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$	4.3	10.2	22.6	3.8	25.4	27.9	ns
		$V_{CC} = 1.4 \text{ V} \text{ to } 1.6 \text{ V}$	3.6	7.3	13.3	3.2	15.8	17.4	ns
		V_{CC} = 1.65 V to 1.95 V	3.2	6.3	10.6	2.9	12.8	14.1	ns
		V_{CC} = 2.3 V to 2.7 V	3.0	5.3	8.5	2.7	10.1	11.1	ns
		V_{CC} = 3.0 V to 3.6 V	2.8	5.0	7.8	2.7	9.2	10.1	ns
C _L = 5 pl	F, 10 pF, 15 pF and	30 pF							
C _{PD}	power dissipation	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{\text{CC}}$							
	capacitance	$V_{CC} = 0.8 V$	-	2.6	-	-	-	-	pF
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$	-	2.9	-	-	-	-	pF
		$V_{CC} = 1.4 \text{ V} \text{ to } 1.6 \text{ V}$	-	3.0	-	-	-	-	pF
		V_{CC} = 1.65 V to 1.95 V	-	3.2	-	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	3.8	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	4.4	-	-	-	-	pF

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 9.

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

 $\mathsf{P}_{D}=C_{PD}\times V_{CC}{}^{2}\times f_{i}\times N$ + $\Sigma(C_{L}\times V_{CC}{}^{2}\times f_{o})$ where:

 $f_i = input frequency in MHz;$

f_o = output frequency in MHz;

 C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

$$\begin{split} N &= number \mbox{ of inputs switching;} \\ \Sigma(C_L \times V_{CC}{}^2 \times f_o) &= sum \mbox{ of the outputs.} \end{split}$$

Low-power dual 2-input NAND Schmitt trigger

13. Waveforms

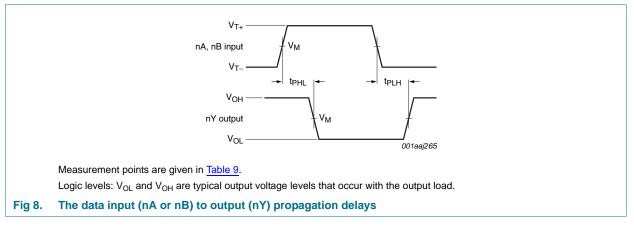


Table 9. Measurement points

Supply voltage	Output	Input					
V _{CC}	V _M	V _M	VI	t _r = t _f			
0.8 V to 3.6 V	$0.5 imes V_{CC}$	$0.5 imes V_{CC}$	V _{CC}	\leq 3.0 ns			

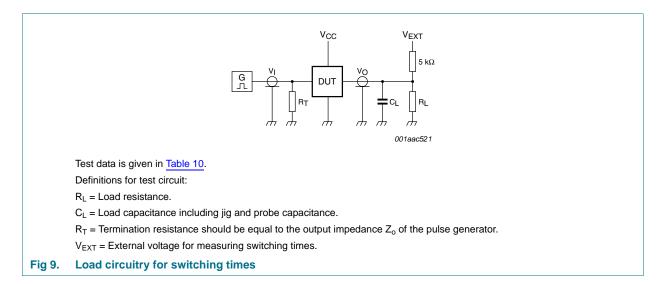


Table 10. T	est data
-------------	----------

Supply voltage	Load		V _{EXT}		
V _{CC}	CL	R _L [1]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k Ω or 1 M Ω	open	GND	$2\times V_{CC}$

[1] For measuring enable and disable times $R_L = 5 k\Omega$, for measuring propagation delays, setup and hold times and pulse width $R_L = 1 M\Omega$.

Low-power dual 2-input NAND Schmitt trigger

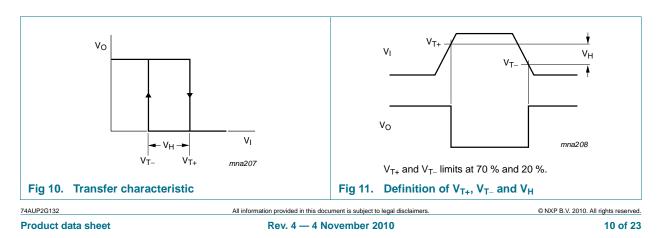
14. Transfer characteristics

Table 11. Transfer characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 9.

Symbol	Parameter	Conditions	Tai	T _{amb} = 25 °C		T _{amb} = -40 °C to +125 °C			Unit
		Min	Тур	Мах	Min	Max (85 °C)	Max (125 °C)		
V_{T+}	positive-going threshold voltage	see <u>Figure 10</u> and <u>Figure 11</u>							
		$V_{CC} = 0.8 V$	0.30	-	0.60	0.30	0.60	0.62	V
		$V_{CC} = 1.1 V$	0.53	-	0.90	0.53	0.90	0.92	V
		$V_{CC} = 1.4 V$	0.74	-	1.11	0.74	1.11	1.13	V
		V _{CC} = 1.65 V	0.91	-	1.29	0.91	1.29	1.31	V
		$V_{CC} = 2.3 V$	1.37	-	1.77	1.37	1.77	1.80	V
		$V_{CC} = 3.0 V$	1.88	-	2.29	1.88	2.29	2.32	V
V _T _ negative-going threshold voltage		see <u>Figure 10</u> and <u>Figure 11</u>							
		$V_{CC} = 0.8 V$	0.10	-	0.60	0.10	0.60	0.60	V
		V _{CC} = 1.1 V	0.26	-	0.65	0.26	0.65	0.65	V
		$V_{CC} = 1.4 V$	0.39	-	0.75	0.39	0.75	0.75	V
		V _{CC} = 1.65 V	0.47	-	0.84	0.47	0.84	0.84	V
		$V_{CC} = 2.3 V$	0.69	-	1.04	0.69	1.04	1.04	V
		$V_{CC} = 3.0 V$	0.88	-	1.24	0.88	1.24	1.24	V
V _H	hysteresis voltage	(V _{T+} – V _{T-}); see <u>Figure 10</u> , <u>Figure 11</u> , <u>Figure 12</u> and <u>Figure 13</u>							
		$V_{CC} = 0.8 V$	0.07	-	0.50	0.07	0.50	0.50	V
		V _{CC} = 1.1 V	0.08	-	0.46	0.08	0.46	0.46	V
		$V_{CC} = 1.4 V$	0.18	-	0.56	0.18	0.56	0.56	V
		V _{CC} = 1.65 V	0.27	-	0.66	0.27	0.66	0.66	V
		$V_{CC} = 2.3 V$	0.53	-	0.92	0.53	0.92	0.92	V
		$V_{CC} = 3.0 V$	0.79	-	1.31	0.79	1.31	1.31	V

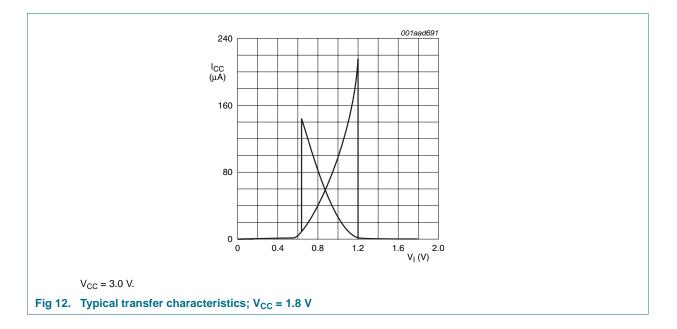
15. Waveforms transfer characteristics

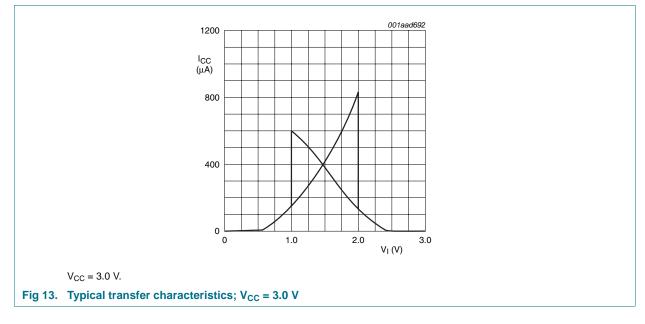


NXP Semiconductors

74AUP2G132

Low-power dual 2-input NAND Schmitt trigger





Low-power dual 2-input NAND Schmitt trigger

16. Application information

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

 $P_{add} = f_i \times (t_r \times \Delta I_{CC(AV)} + t_f \times \Delta I_{CC(AV)}) \times V_{CC} \text{ where:}$

 P_{add} = additional power dissipation (µW);

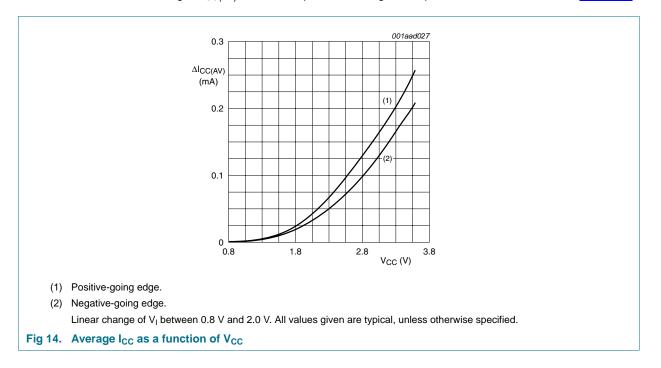
 $f_i = input frequency (MHz);$

 t_r = input rise time (ns); 10 % to 90 %;

 $t_f = input fall time (ns); 90 \% to 10 \%;$

 $\Delta I_{CC(AV)}$ = average additional supply current (µA).

Average $\Delta I_{CC(AV)}$ differs with positive or negative input transitions, as shown in Figure 14.



Low-power dual 2-input NAND Schmitt trigger

17. Package outline

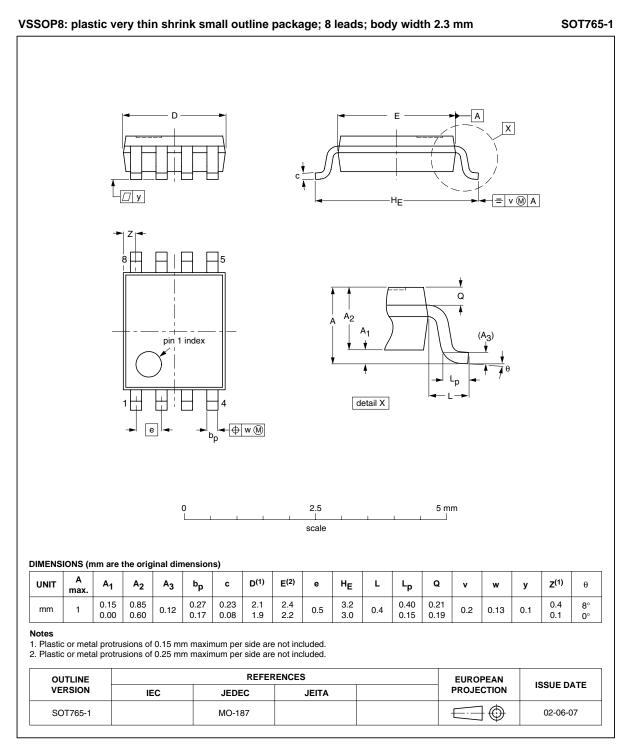


Fig 15. Package outline SOT765-1 (VSSOP8)

Low-power dual 2-input NAND Schmitt trigger

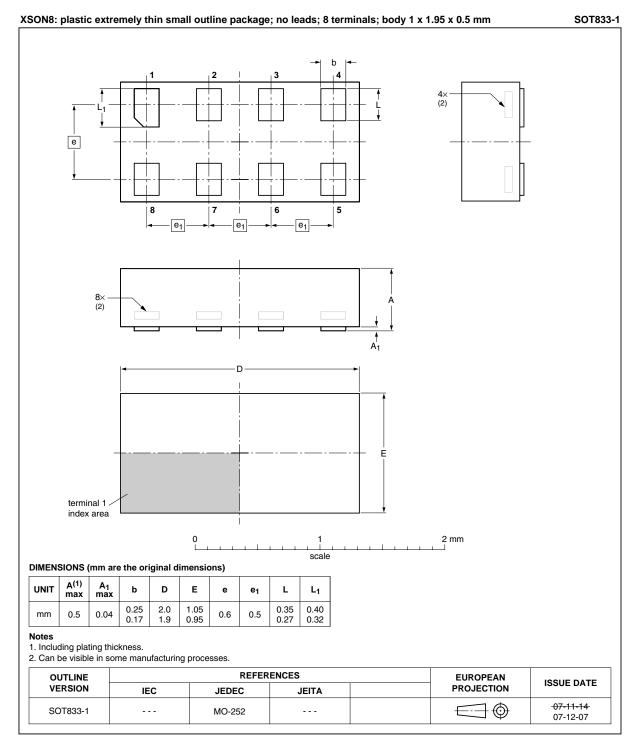
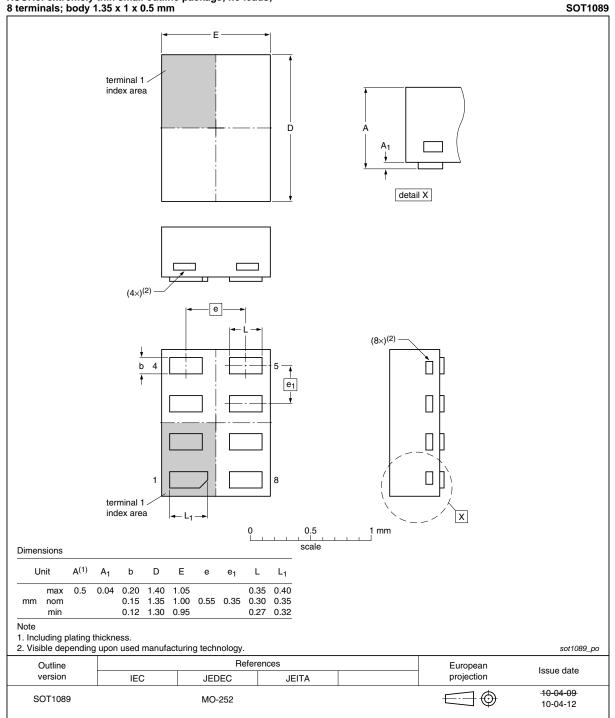


Fig 16. Package outline SOT833-1 (XSON8)

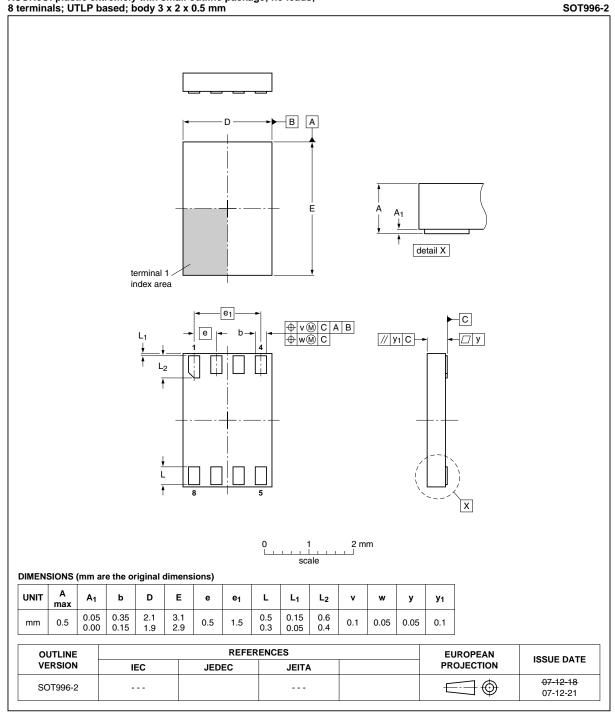
Low-power dual 2-input NAND Schmitt trigger



XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm

Fig 17. Package outline SOT1089 (XSON8)

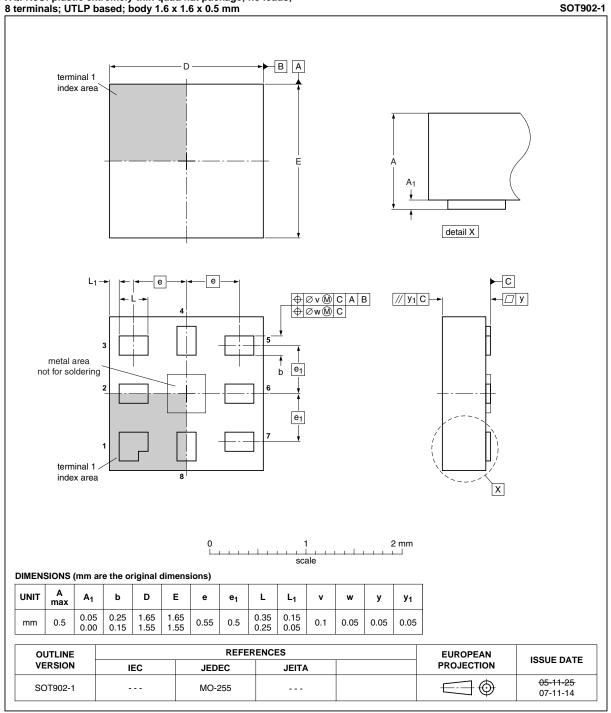
Low-power dual 2-input NAND Schmitt trigger



XSON8U: plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 x 2 x 0.5 mm

Fig 18. Package outline SOT996-2 (XSON8U)

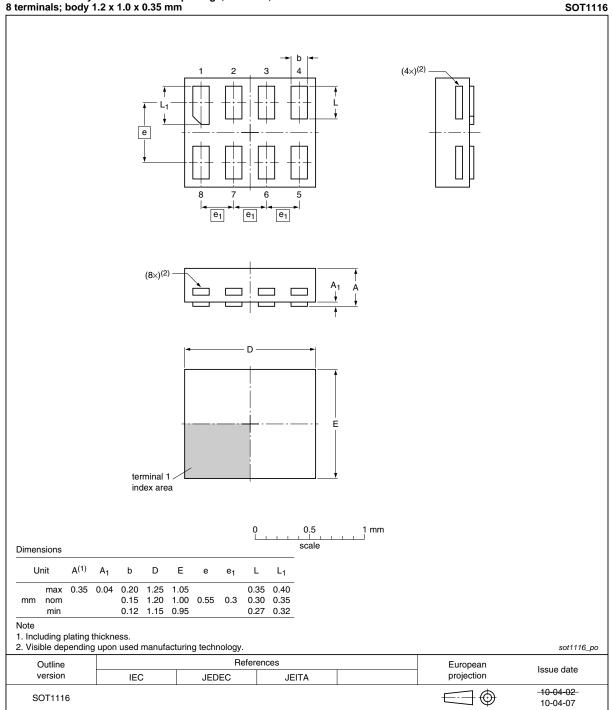
Low-power dual 2-input NAND Schmitt trigger



XQFN8U: plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm

Fig 19. Package outline SOT902-1 (XQFN8U)

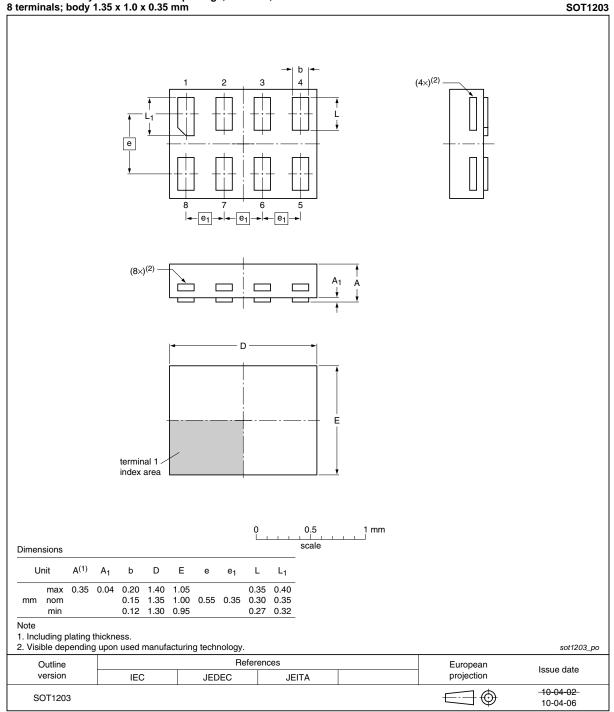
Low-power dual 2-input NAND Schmitt trigger



XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm $\,$

Fig 20. Package outline SOT1116 (XSON8)

Low-power dual 2-input NAND Schmitt trigger



XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm

Fig 21. Package outline SOT1203 (XSON8)

Low-power dual 2-input NAND Schmitt trigger

18. Abbreviations

AcronymDescriptionCDMCharged Device ModelDUTDevice Under TestESDElectroStatic DischargeHBMHuman Body ModelMMMachine Model	Table 12. Abbreviations			
DUTDevice Under TestESDElectroStatic DischargeHBMHuman Body Model	Acronym	Description		
ESD ElectroStatic Discharge HBM Human Body Model	CDM	Charged Device Model		
HBM Human Body Model	DUT	Device Under Test		
	ESD	ElectroStatic Discharge		
MM Machine Model	HBM	Human Body Model		
	MM	Machine Model		

19. Revision history

Table 13. Revision h	nistory			
Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G132 v.4	20101104	Product data sheet	-	74AUP2G132 v.3
Modifications:	 Added typ 	e number 74AUP2G132GF	(SOT1089/XSON8 pack	kage).
	 Added type 	e number 74AUP2G132GN	(SOT1116/XSON8 pack	kage).
	 Added type 	e number 74AUP2G132GS	(SOT1203/XSON8 pack	kage).
74AUP2G132 v.3	20081215	Product data sheet	-	74AUP2G132 v.2
74AUP2G132 v.2	20080314	Product data sheet	-	74AUP2G132 v.1
74AUP2G132 v.1	20061018	Product data sheet	-	-

74AUP2G132

Low-power dual 2-input NAND Schmitt trigger

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. The product is not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Product data sheet

74AUP2G132

All information provided in this document is subject to legal disclaimers. Rev. 4 — 4 November 2010

NXP Semiconductors

74AUP2G132

Low-power dual 2-input NAND Schmitt trigger

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

21. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

74AUP2G132

Low-power dual 2-input NAND Schmitt trigger

22. Contents

1	General description 1
2	Features and benefits 1
3	Applications 1
4	Ordering information 2
5	Marking 2
6	Functional diagram 2
7	Pinning information 3
7.1	Pinning 3
7.2	Pin description 3
8	Functional description 4
9	Limiting values 4
10	Recommended operating conditions 4
11	Static characteristics 5
12	Dynamic characteristics 7
13	Waveforms
14	Transfer characteristics 10
15	Waveforms transfer characteristics 10
16	Application information
17	Package outline 13
18	Abbreviations 20
19	Revision history 20
20	Legal information 21
20.1	Data sheet status 21
20.2	Definitions 21
20.3	Disclaimers
20.4	Trademarks 22
21	Contact information 22
22	Contents 23

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2010.

All rights reserved.

For more information, please visit: http://www.nxp.com For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 November 2010 Document identifier: 74AUP2G132