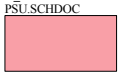
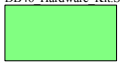
U_DB_Common
DB_Common

U_PSU
PSU.SCHDOC



U_Bypass_Board
DB_Bypass

U_DB46_Hardware_Kit
DB46_Hardware_Kit.SchDoc



Sheet Title	***DB46 Top Level***		
Project Title	***DB46 - Virtex4 SX35***		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:03 PM	Sheet 1 of 23	
File: DB46_Top.SchDoc			

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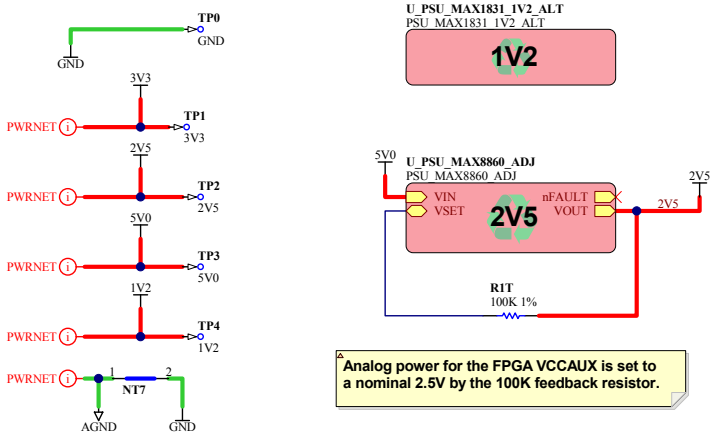

Sheet Title	*Power Supply Top Level*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:03 PM	Sheet 2 of 23	
File: PSU.SCHDOC			

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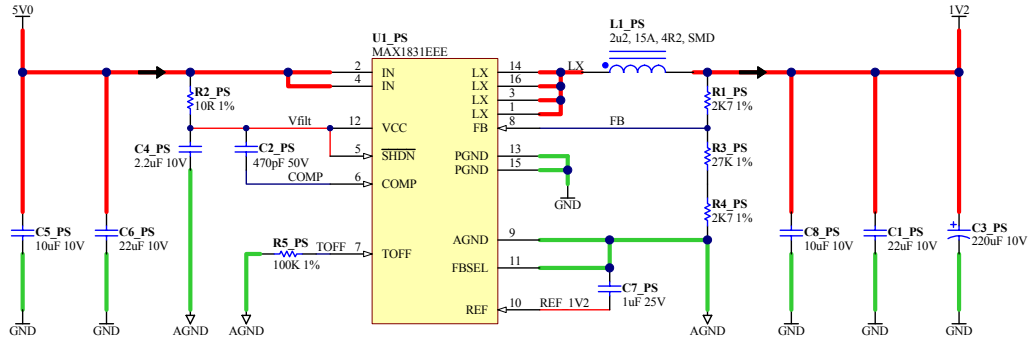

Sheet Title	***Power Supply MAX1831 (1V2)***	
Project Title	***DB46 - Virtex4 SX35***	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 3 of 23
File: PSU_MAX1831_1V2_ALT.SchDoc		

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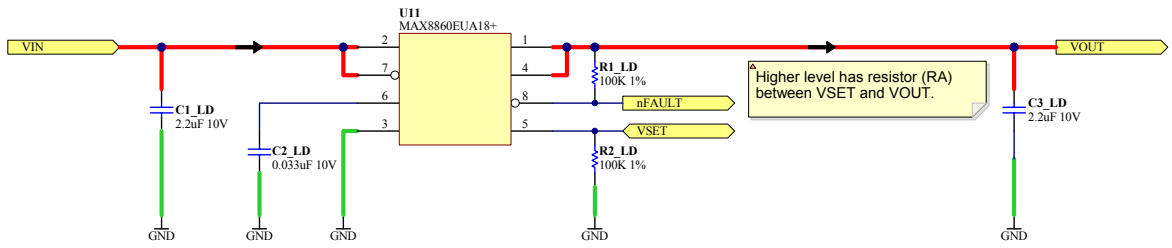

The voltage provided by the MAX8860 linear regulator is determined by the addition of a resistor between VOUT and VSET.

This additional resistor (RA) is located on the higher-level schematic.

The voltage produced by the MAX8860 is calculated as follows:
VOUT = 1.25 * (1 + RA / 100k)

If RA = 20k, VOUT = 1.25 * (1 + 20k/100k) = 1.50 Volts
If RA = 100k, VOUT = 1.25 * (1 + 100k/100k) = 2.50 Volts
If RA = 164k, VOUT = 1.25 * (1 + 164k/100k) = 3.30 Volts

Note that if VSET is grounded (on the higher-level schematic), VOUT=1.8 Volts

Note also that VIN must be a minimum of 0.18 Volts above VOUT.

Sheet Title	*Power Supply MAX8860 (2V5)*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 4 of 23	
File: PSU_MAX8860_ADJ.SchDoc			

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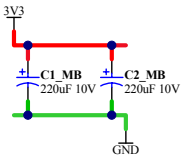

These decoupling capacitors are intended to assist the voltage rails on the PCB - where the decoupling capacitors for the FPGA are not close.

Sheet Title	*Board Bypass Capacitors*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 5 of 23	
File: DB_Bypass.SchDoc			

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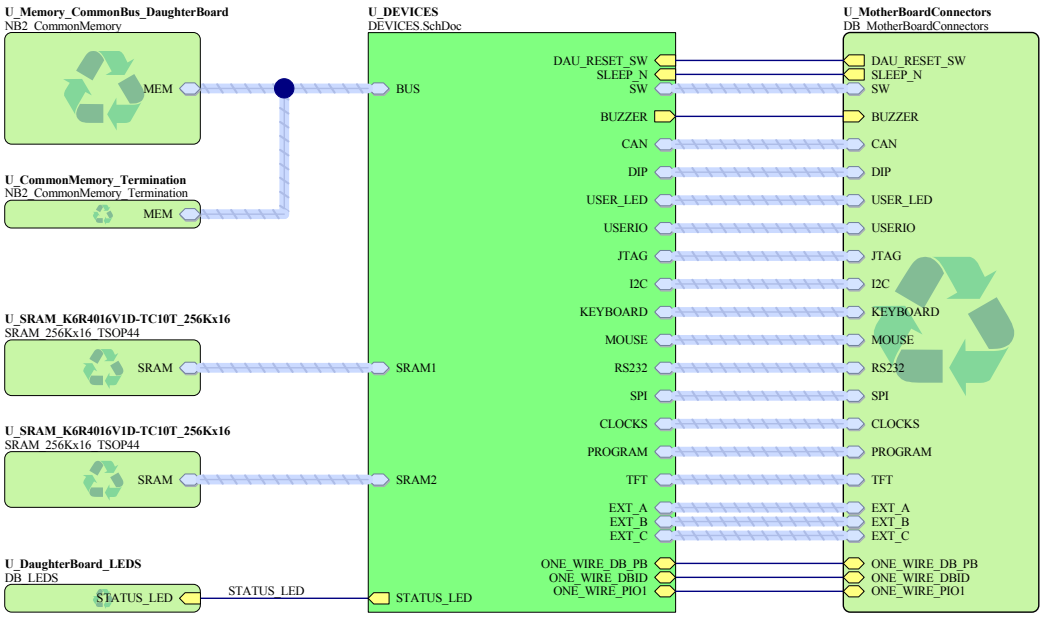
Top Level Schematic For Daughter Board Design
Both FPGA-Only and FPGA + MCU

This Device Sheet is the same for all designs.
It relies on being instantiated in a project that contains a device-specific sheet named DEVICES.SchDoc .



Sheet Title	*Daughter Board Top Level*	
Project Title	*DB46 - Virtex4 SX35*	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008 Time: 4:51:04 PM	Sheet 6 of 23	
File: DB_Common.SchDoc		

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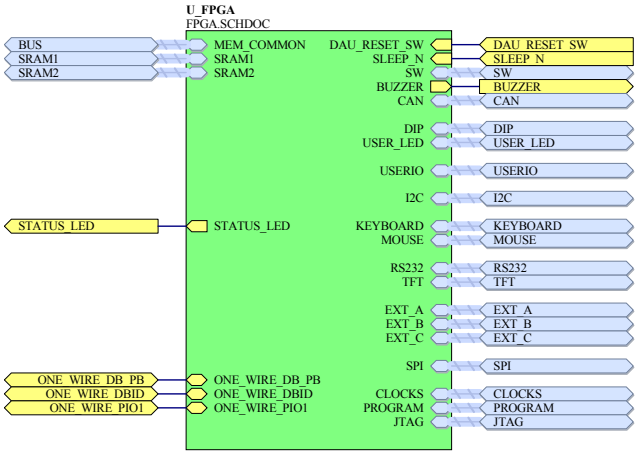

Device Specific Section of Daughter Board Design

This schematic sheet (plus any child sheets) will contain the device specific parts of any daughter board designs.

This will include any FPGA or MCU devices as well as dedicated power supplies, connectors etc.

Sheet Title	*FPGA, LEDs and SRAM Memory*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 7 of 23	
File: DEVICES.SchDoc			

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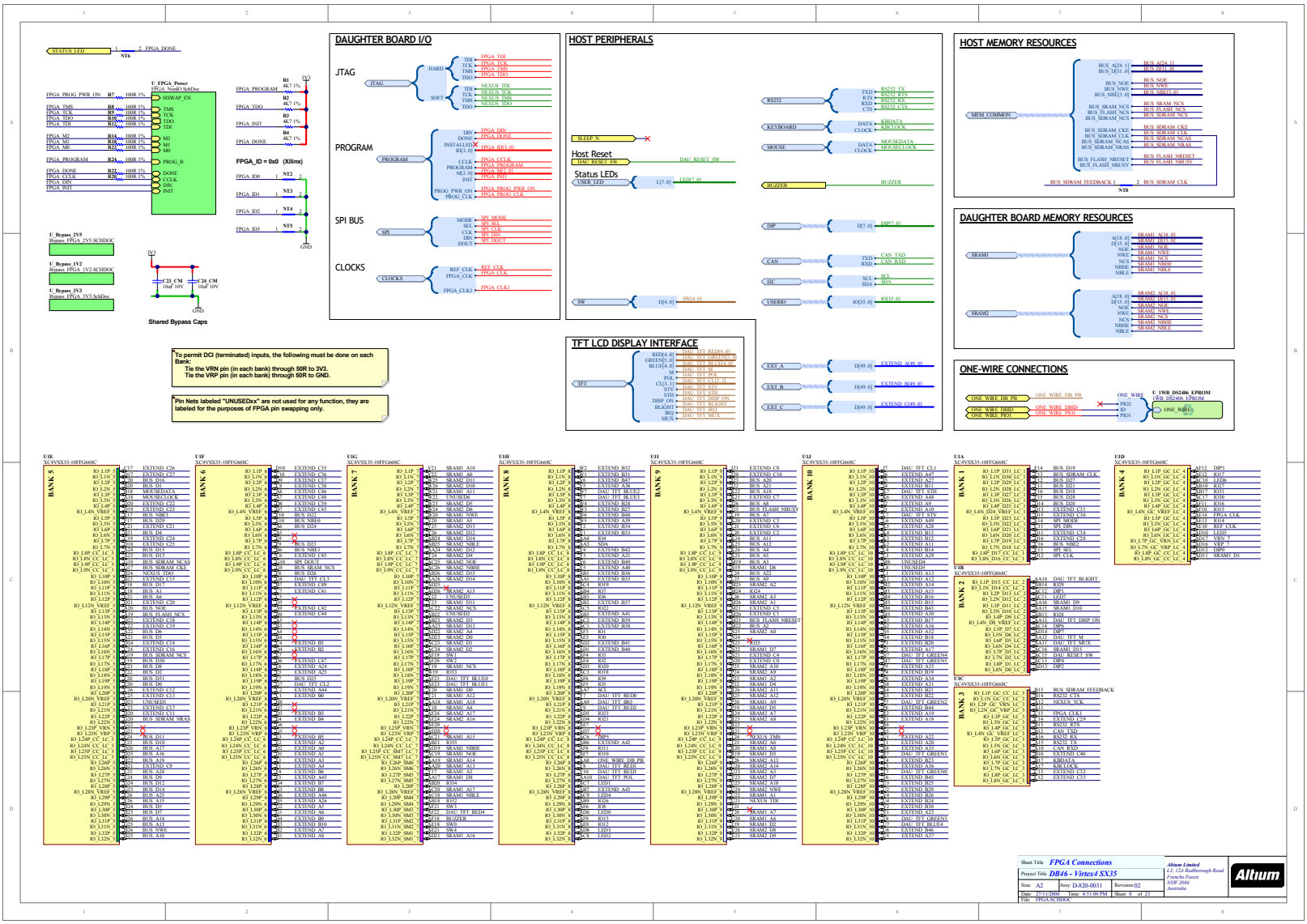

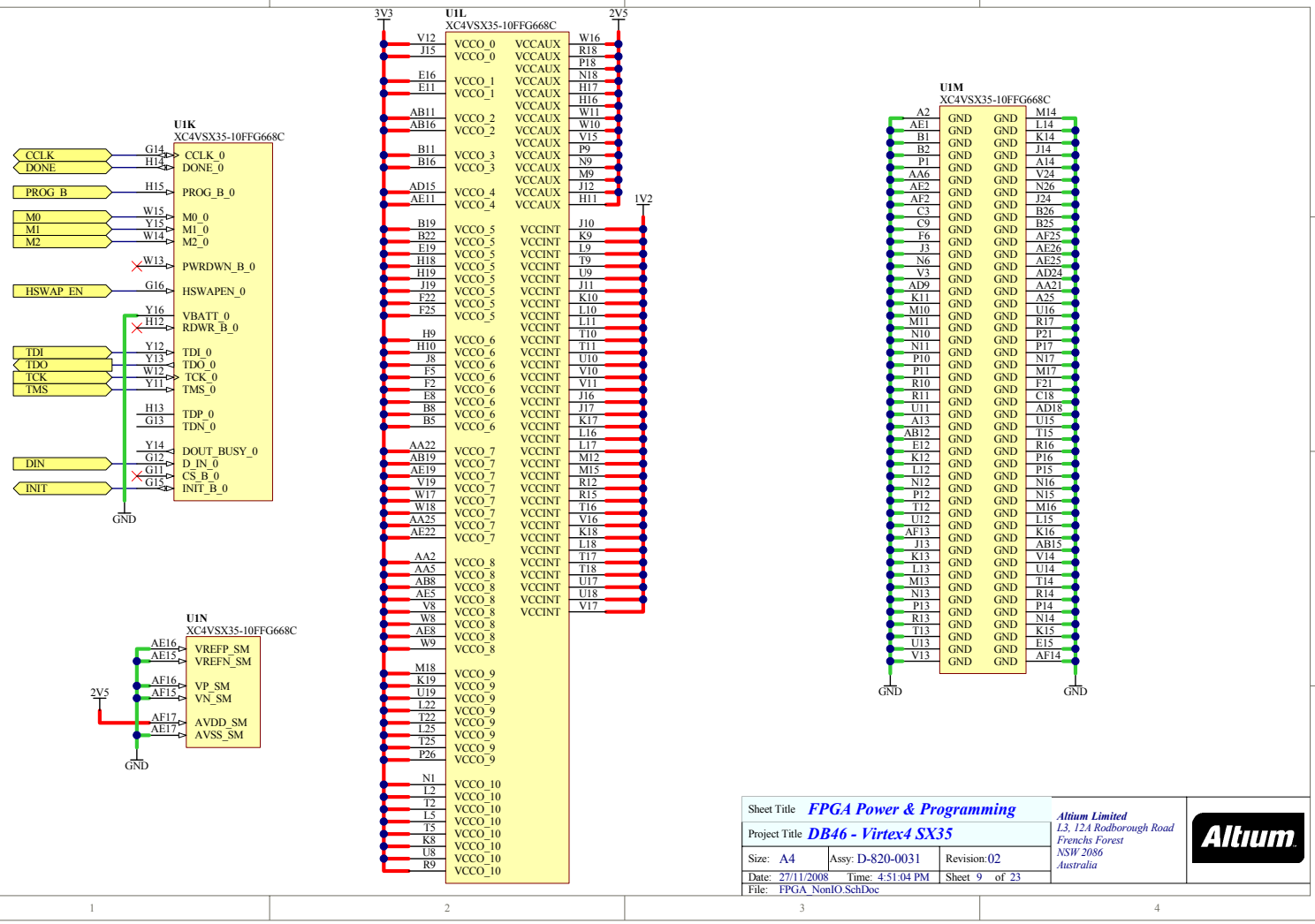

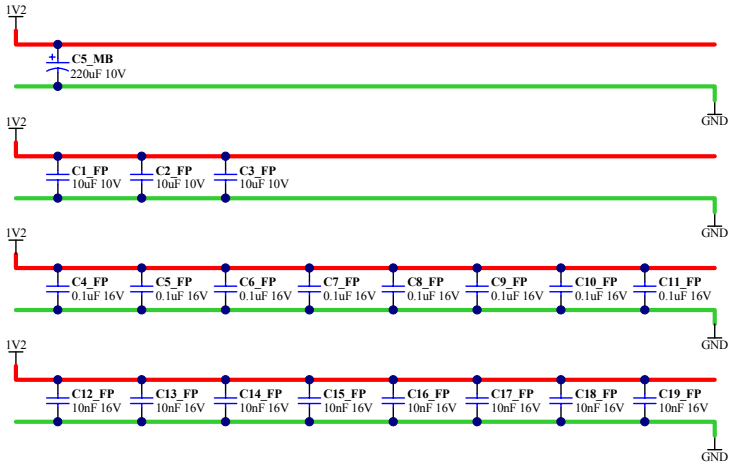

Sheet Title	*FPGA Bypass Capacitors for 1V2*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 10 of 23	
File: Bypass_FPGA_1V2.SCHDOC			

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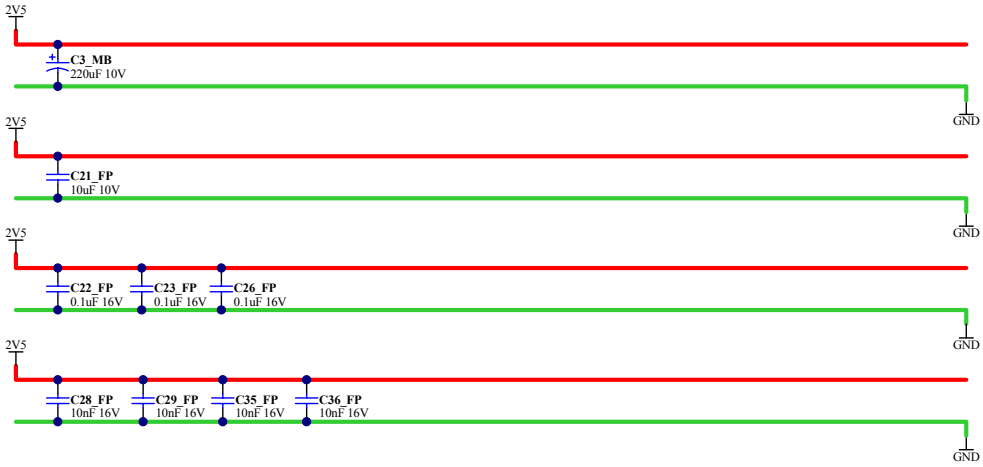

Sheet Title	*FPGA Bypass Capacitors for 2V5*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 11 of 23	
File: Bypass_FPGA_2V5.SCHDOC			

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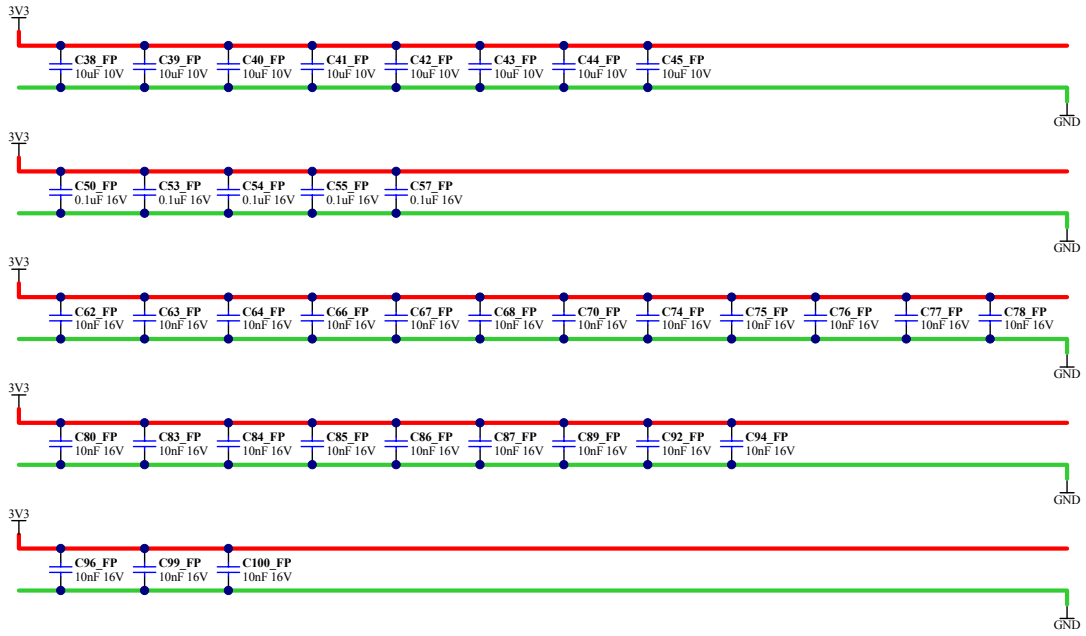

Sheet Title	*FPGA Bypass Capacitors for 3V3*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 12 of 23	
File: Bypass_FPGA_3V3.SchDoc			

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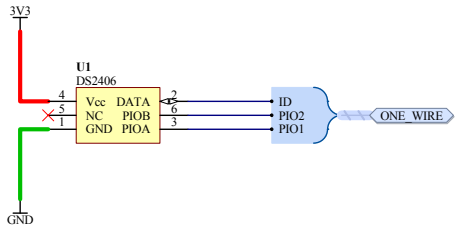

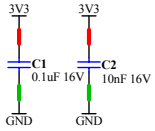

Sheet Title	*1-Wire Bus ID*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 13 of 23	
File: 1WB_DS2406_EPROM.SchDoc			

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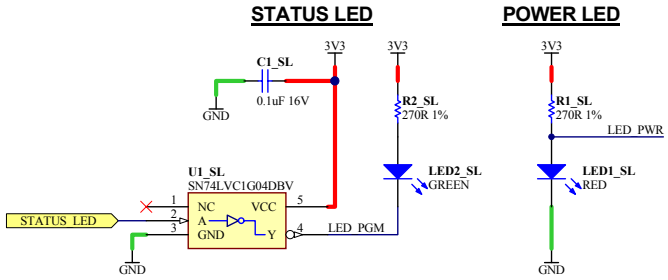

Sheet Title	*Daughter Board LEDs*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 14 of 23	
File: DB_LEDS.SchDoc			

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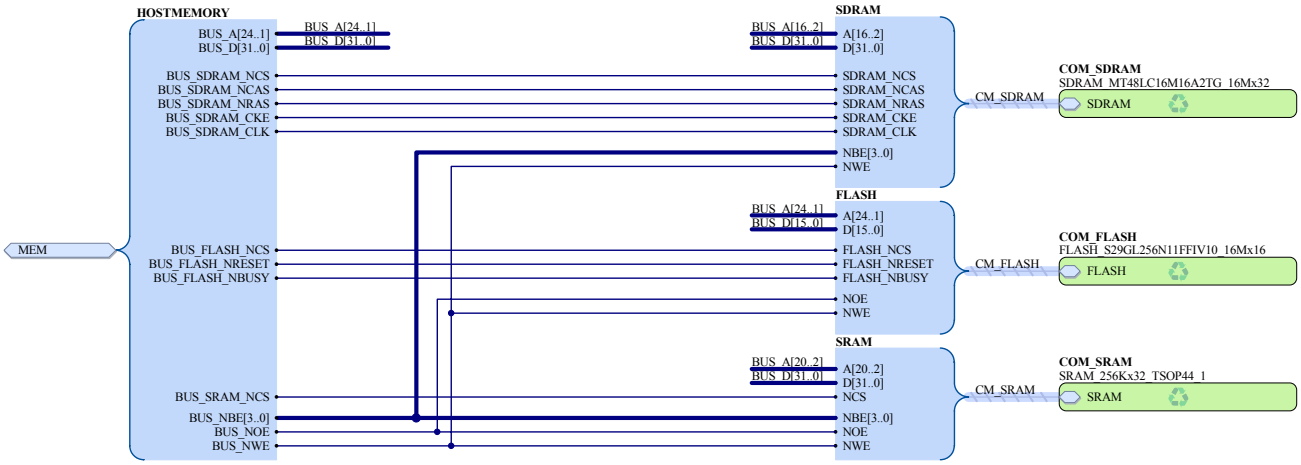

Sheet Title	*Common-Bus Memory Block*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 15 of 23	
File: NB2_CommonMemory.SchDoc			

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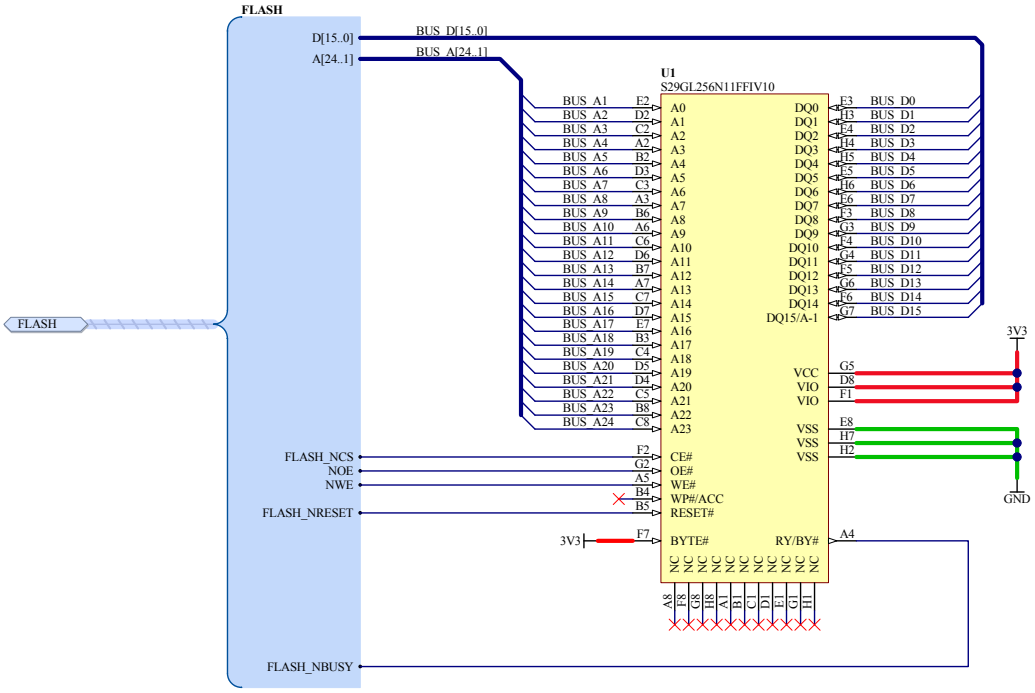

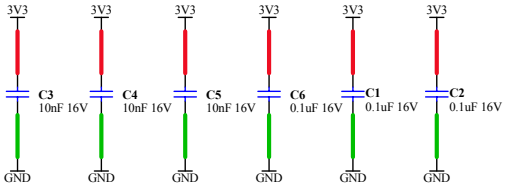

Sheet Title	*16M x 16 Flash Memory (BGA)*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 16 of 23	
File: FLASH_S29GL256N11FFIV10_16Mx16.SchDoc			

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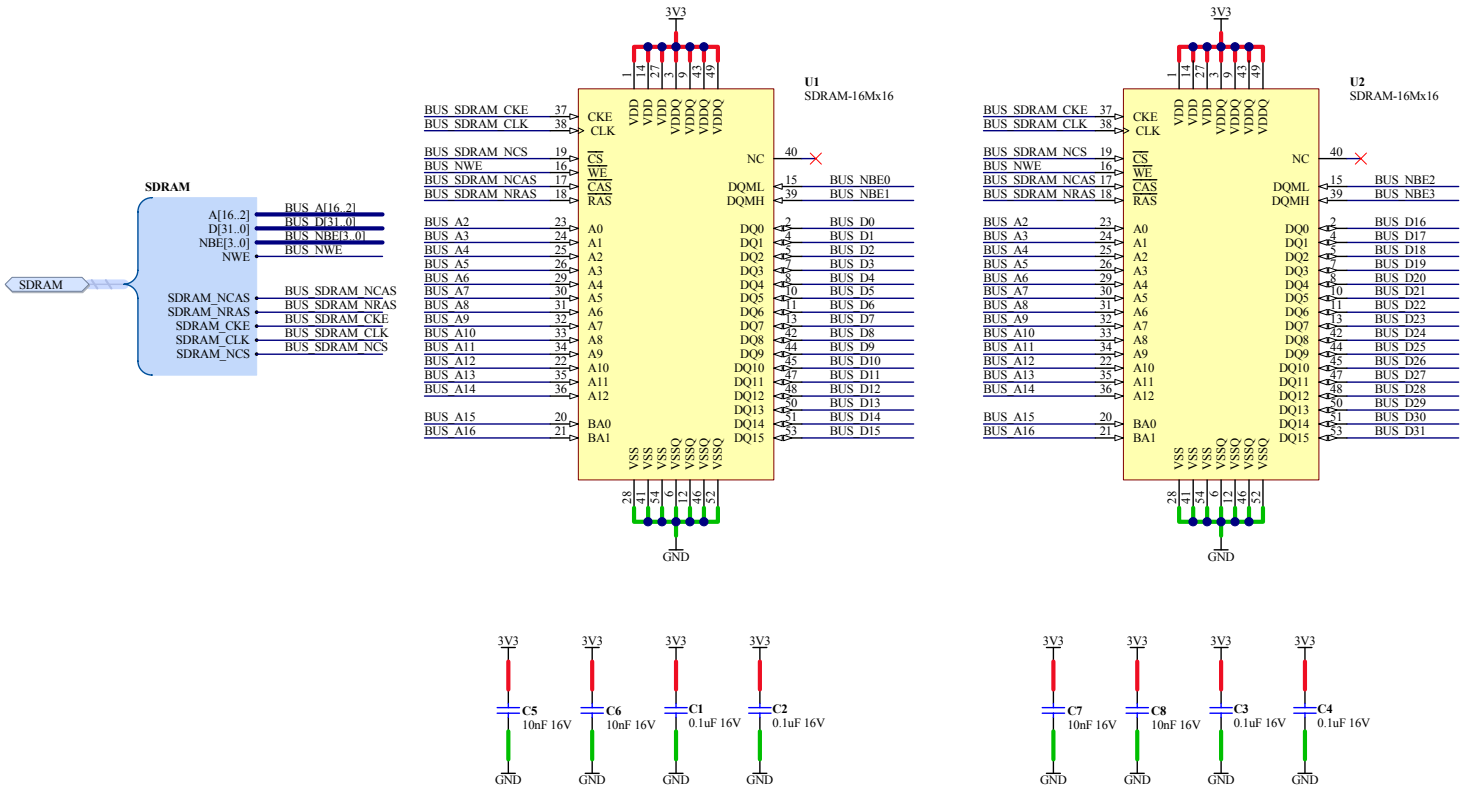

Sheet Title	*16M x 32 SDRAM TSOP54 x 2*	
Project Title	*DB46 - Virtex4 SX35*	
Size: A4	Assy: D-820-0031	Revision:02
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 17 of 23
File: SDRAM_MT48LC16M16A2TG_16Mx32.SchDoc		

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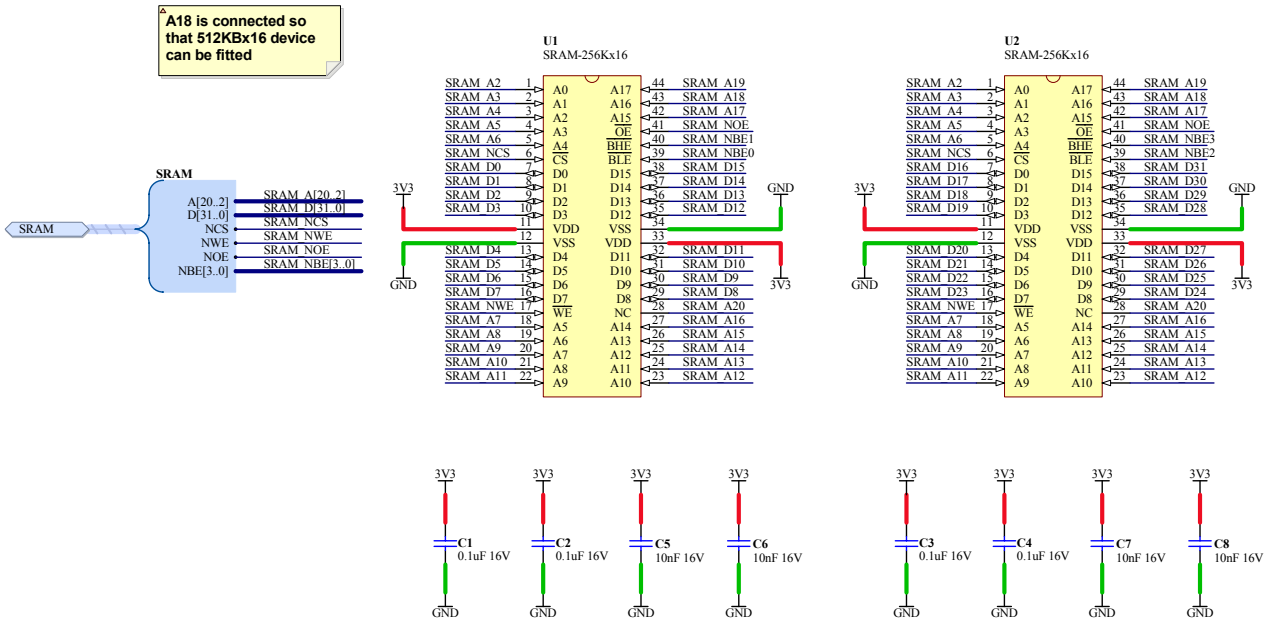

Sheet Title	*256K x 32 SRAM - TSOP44 x 2*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 18 of 23	
File: SRAM_256Kx32_TSOP44_1.SchDoc			

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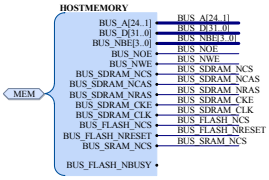
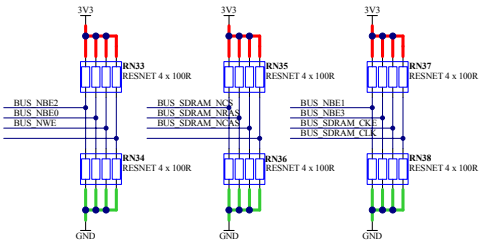


THESE SIGNALS TERMINATE AT THE SDRAM DEVICE



All devices using controlled impedance outputs from the source (ie. FPGA) should use 50 ohm (2 parallel 100 ohm resistors) termination.

The Flash should be located closest to the source (FPGA).
The SRAM should be located next furthest from the source (FPGA).
The SDRAM should be located next furthest from the source (FPGA).
Terminations are to be located at the furthest distance from the source (FPGA).

Note that pins 5,6,7 and 8 of the following resnet "groups" are pin-swappable within that "group":
- all "power" resnets that terminate the FLASH-only signals (ie. RN1 and RN3).
- all "ground" resnets that terminate the FLASH-only signals (ie. RN2 and RN4).
- all "power" resnets that terminate the FLASH-SRAM-only signals (ie. RN5 and RN7).
- all "ground" resnets that terminate the FLASH-SRAM-only signals (ie. RN6 and RN8).
- all "power" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN9, RN11, RN13, RN15, RN17, RN19, RN21, RN23, RN25, RN27, RN29, RN31, RN33, RN35).
- all "ground" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN10, RN12, RN14, RN16, RN18, RN20, RN22, RN24, RN26, RN28, RN30, RN32, RN34, RN36).

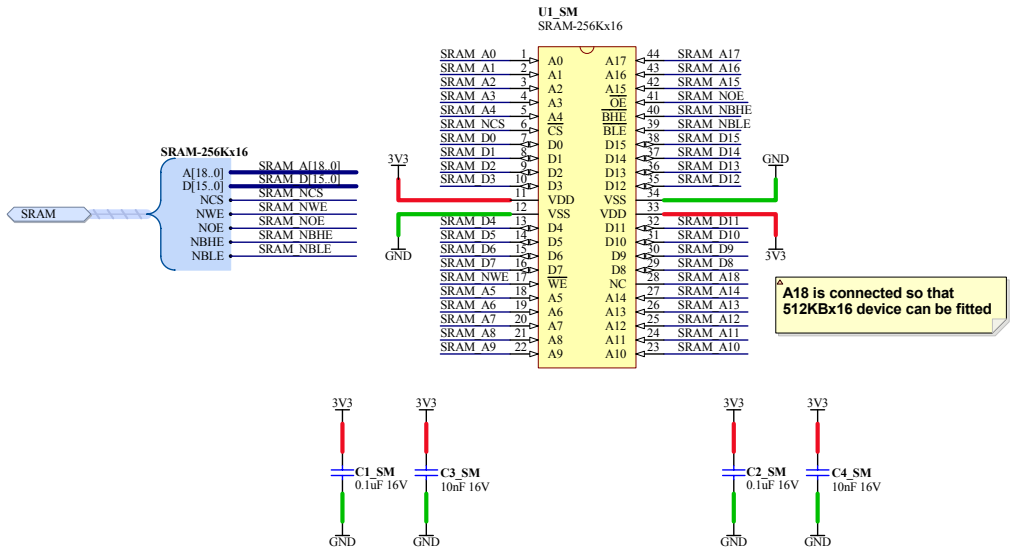
To remove any confusion by the PCB assembler, the following devices have been deleted entirely from the design: RN1 to RN16, and RN17 to RN32.

Note that high current (up to 1.25 Amps) is drawn from the 3V3 rail when all 19 pairs of resnets are loaded. The addition of up to 4.1 watts of heat was significantly warming the PCB.

Testing has confirmed that the loading of only 3 pairs of resnets (RN33/34, RN35/36 and RN37/38) provides good operation at speeds up to 96MHz. This consumes up to 0.20 amps, ie. up to 0.65 watts of heat.

The loading of the 3 pairs of resnets terminates only the output control signals from the FPGA to the SDRAM. The bidirectional data bus and address bus is not terminated. Signals that do not connect to the SDRAM (ie. signals to the slower flash and SRAM devices only) are also not terminated.

Sheet Title: *Memory CommonBus Terminations*			*Altium Limited* *L3, 12A Rodborough Road* *Frenchs Forest* *NSW 2086* *Australia*
Project Title: *DB46 - Virtex4 SX35*			
Size: A3	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 19 of 23	
File: NB2_CommonMemory_Termination.SchDoc			



Sheet Title	*256K x 16-Bit SRAM*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 20 of 23	
File: SRAM_256Kx16_TSOP44.SchDoc			

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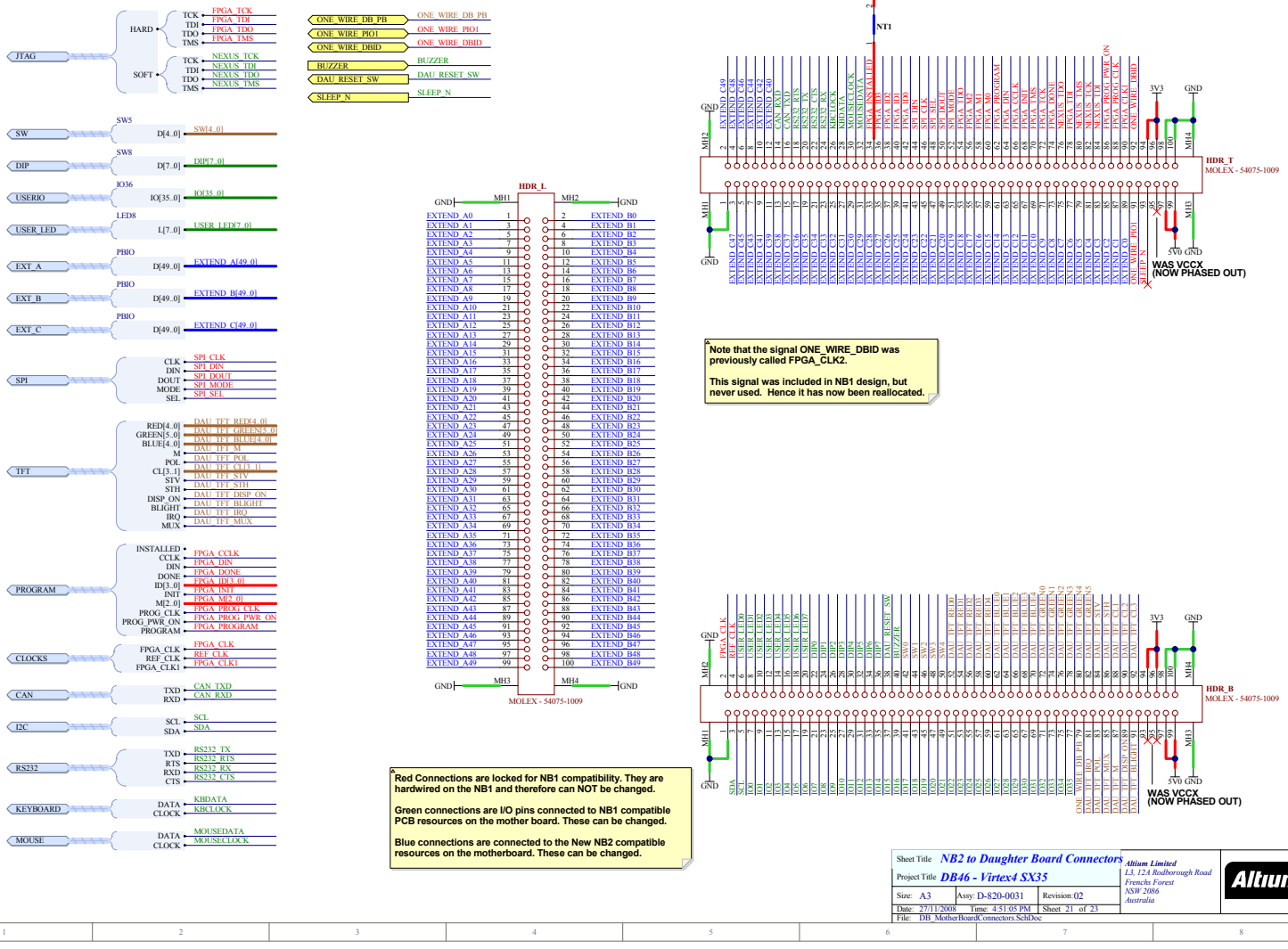

Sheet Title	NB2 to Daughter Board Connectors
Project Title	DB46 - Virtex4 SX35
Size: A3	Assy: D-820-0031 Revision: 02
Date: 27/11/2008	Time: 4:51:05 PM Sheet 21 of 23
File: DB_MotherBoardConnectors.SchDoc	

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U_MOUNTS
DB_MOUNTS

PCB1
DB46 Blank PCB
Printed Circuit Board (Bare)

Fiducial Alignment Components

FD1
Fiducial - Round

FD2
Fiducial - Round

Sheet Title	*DB46 Hardware Kit*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:05 PM	Sheet 22 of 23	
File: DB46_Hardware_Kit.SchDoc			

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MH1
MOUNTING HOLE 3MM

MH2
MOUNTING HOLE 3MM

MH3
MOUNTING HOLE 3MM

Altium Logo Top1

Altium Logo Bot1

Sheet Title	*Mounts, Logo & Label*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:05 PM	Sheet 23 of 23	
File: DB_MOUNTS.SchDoc			

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